Title of Paper: **Eradicating Processor Obsolescence in Telematics Systems**

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The new challenges facing automotive designers today can be likened more to that of those facing consumer electronics designers. Not only do they need to consider safety, space constraints and tough temperature ranges but are also faced with ever changing standards and protocols and time to market pressures.

Reconfigurable logic design techniques utilizing the latest Field Programmable Gate Array (FPGA) hardware and embedded soft-core microprocessors can mean the designer can create one multimedia platform for many applications/products thus reducing inventory and overall costs.

The multimedia platform concept means that one Printed Circuit Board (PCB) can be designed for many applications and given its 'personality' late in the production flow or even in the field thus extending time in market. The platform can be modified or evolved to cope with any standard or protocol around today or in the future using any wired or wireless network.

Obsolescence is a concern of most design engineers and none more so than with automotive telematics equipment designers. Even though automotive electronics equipment design and development time scales have shrunk recently from 5 to 2 years the products themselves will still need to be produced for many years and be active in the field for even longer.

The biggest obsolescence concern is that of out of date microprocessors and microcontrollers. This paper will also explore the possibility of utilising FPGA fabric combined with soft embedded processors to eradicate obsolescence with the added benefit of field upgrades. It will detail both FPGA and the MicroBlaze™ microprocessor architecture and development tool flow. FPGAs can thus offer the flexibility to get to market quicker and can also extend product time in market.

Main Points of the paper:

- Reconfigurable logic enables automotive telematics design to be brought to market quickly and risk free
- The multimedia platform concept allows for one platform for many telematics designs and multiple end customers with the added benefit of being able to be reconfigured in the field to cater for emerging standards and protocols
- The use of FPGA based hardware and embedded soft core processors can eradicate processor obsolescence
- Xilinx's experience in both the telecommunications and consumer equipment can help to bridge the technology and knowledge gaps that exist in automotive telematics design teams
- Exploration of multimedia platform design concept and applications examples

Vehicle and Telematics System Time in Market Mismatch

One of the automotive industries major concerns about Telematics systems is the potential for these units to become obsolete quickly. They exhibit characteristics of consumer products i.e. rapidly changing standards and protocols. In the consumer market space products become obsolete or out of date in 18 months to two years and are simply replaced by the newest model with extra features, functions and bandwidth. For example upgrading mobile phones from simple voice communications via GSM to data communications via GPRS which give the user extra bandwidth and new services such as mobile internet and video phone capability. If a telematics unit fitted into a car exhibits consumer like trends and has this fast a turn around of functionality, suffering from obsolete functions it could be a major headache. The trend is for telematics units not to conform to the standard DIN out line so an out of date system cannot simply be replaced with an after market unit. The standard life time of a vehicle is ten years so the challenge is to make the telematics time in market match that of the life time of the car.

Scalable and Reconfigurable Telematics Platforms

One solution is to design scalable and field upgradeable systems that can be upgraded in the future to cater for changing standards and protocols or have extra functions added long after the car has left the show room.

The ultimate in customer personalisation can be achieved at the dealership by configuring the multi-media platform exactly to the customers specification. So not only can the customer choose the car colour, engine size and upholstery type he could also choose what type of information and entertainment system he requires. For example GPRS instead of GSM, full tracking GPS instead of assisted GPS, DAB radio instead of standard FM and so on. This Reconfigurable solution can also be changed again later on if the customer wishes some other extra function in the future.

Functions stored in low cost memory

FPGA devices are configured on power up from a standard memory device (such as a PROM, Flash or even Compact Flash devices). This enables many different functions to be stored in low cost memory and selectively loaded into the FPGA. As the FPGA configuration process takes only microseconds the discrete functions can be loaded in at the touch of a button imperceptible to the user. This theoretically means that the system can be given enough head room for future features by simply adding larger memory devices.

Partial Reconfiguration

An important feature in FPGAs is the ability to reconfigure a portion of the device while the remainder of the design is still operational. Partial reconfiguration is useful for applications that require the loading of different designs into the same area of the device or the flexibility to change portions of a design without having to either reset or completely reconfigure the entire device. With this capability, entirely new application areas become possible:

• In-the-field hardware upgrades and updates to remote sites
• Runtime reconfiguration
• Adaptive hardware algorithms
• Continuous service applications

Other benefits include:

• Reduced device count
• Reduced power consumption
• More efficient use of available board space

Obsolescence

Obsolescence is a concern of most design engineers and none more so than with automotive telematics equipment designers. Even though automotive electronics equipment design and development time scales have shrunk recently from 5 to 2 years the products themselves will still need to be produced for many years and be active in the field for even longer.

The biggest obsolescence headache is that of out of date microprocessors and microcontrollers. Processors have shorter life spans than ever and are discontinued at short notice driven by the consumer market trends and the ever present need for speed enhancements. Consumer products such as games consoles and mobile phones have built in obsolescence to stimulate sales of the latest and greatest products. This built in obsolescence leads microprocessor manufacturers chasing the planned new platform introductions and high volume sales almost guaranteed and thus propagating the obsolescence ripple effect.

Even if the design has been coded in 'C' (which is always touted as being 'portable code') there are always architecture specific instructions and features which hamper the change over between and obsolete processor to the next generation device. The change over process is further exasperated by difference package options and I/O configurations necessitating the need for a complete board re-spin. If we imagine the scenario where every Electronic Control Unit (ECU) in a car contains at least one processor and that every car contains up to 60 ECUs this leads to a major headache every time a processor is obsoleted at relatively short notice.

There are several solutions to the problem of processor obsolescence. The applicability of any given solution depends upon a number of variables, including the value of the application software, the projected life of the system and the amount of time and money available to solve the problem. The most radical and most expensive solution is to redesign the system around a new processor. Depending upon the volume of the code, a redesign can cost hundreds of man-years of time, much of it devoted to validation and testing. Not only is the huge investment in debugging and refining the existing software lost, a clear case of throwing the baby out with the bath water, but the solution is temporary at best. If the system has a long projected life, the same problem will recur every few years, as each new design in turn becomes obsolete. Another solution is the last time buy (LTB), which, on the surface, appears to be the most cost-effective option. The problem is that the automotive designer must guess at how much product to buy for the life of his program. If he guesses wrong, he is faced with an even more difficult problem; a larger legacy investment that must somehow be upgraded.

Inserting a new processor along with software written to emulate the old one is presently more good in theory than a reality. The concept is appealing and in fact does have some operational history. The legacy software is preserved, and the process is therefore relatively cheap and fast. Once again, the solution is not permanent and, if the system has a long projected life, might have to be repeated every few years. More important, software emulation is inherently a serial process and therefore relatively slow. That means that the new processor must consume much of its performance running the emulation rather than the application. It has been shown empirically that emulation requires, on the average, about twenty clock cycles of the new processor for every legacy instruction it executes. In addition, emulation breeds further obsolescence since the processor used as the emulation engine itself will become obsolete and may force an entire rewrite of the emulator.

Soft Processor Solution

A radical but robust new solution is emerging to eradicate processor obsolescence and preserve many years of legacy code and development. The new way is to **own** the soft processor core and embed it in FPGA fabric. Not only can you port the core to multiple FPGA platforms but you can 'design' the peripheral set to meet the exact design requirements thus eradicating architecture compromises and wasted peripherals.

For example, the designer may desire a processor with perhaps 10 UARTs, an interrupt controller and access to a block of external FLASH. Whilst many off-the-shelf processors exist that would offer multiple UARTs and the other desired peripherals, they would typically be of sufficient complexity to have numerous other peripherals that would be unused in this system. Not only is the designer paying for the additional peripherals, it is often necessary that unused peripherals in this type of processor have to be placed into a safe mode or otherwise disabled via software. This places an additional burden on the software design team, who not only have to make the used processor peripherals operate correctly, but now have to write code for the parts of the processor which are not used. It is clear that purchasing an off the shelf solution for this scenario would be highly wasteful not only in terms of initial cost, but also in wasted engineering time during the design process.

With the Xilinx® MicroBlaze™ soft processor, the designer has the luxury of a different approach. They can now start with a processor core and build the peripheral set to meet their exact requirements. Silicon wastage is reduced to zero since the designer will only ever implement what they need. Software design complexity is reduced because no code need ever be written to disable unwanted processor functionality. The creation of unusual processor configurations, which can be changed at any time to suit changes in the specification, is reduced to a simple task.

Even if after five or six years of field use when the FPGA hardware may itself be nearing the end of its life then the soft processor core can simply be dropped into its new FPGA *host* utilising the same C code. The hardware platform may need some PCB modifications but the legacy code remains usable and intact.

Xilinx MicroBlaze™ and PicoBlaze™ Soft Processors

Xilinx offers both a 32-bit soft processor core called MicroBlaze and an 8-bit solution called PicoBlaze™. The PicoBlaze processor runs at speeds of 116 MHz, yet occupies a tiny footprint of just 35 Configurable Logic Blocks (CLBs). (See Figure 1).

The MicroBlaze™ 32-bit soft processor core is the industry's fastest soft processing solution and runs at 150 MHz and delivers 100 D-MIPS. It features a RISC architecture with Harvard-style separate 32-bit instruction and data busses running at full speed to execute programs and access data from both on-chip and external memory. A standard set of peripherals are also CoreConnect™ enabled to offer MicroBlaze designers compatibility and reuse. Table 1 shows the details of the two soft core processors.

The MicroBlaze Embedded Development Kit, including the soft processor core and a standard set of peripherals, will be available from Xilinx and its distribution partners. The kit includes a complete set of GNU-based software tools including the compiler, assembler, debugger, and linker. MicroBlaze Kits that are bought from Xilinx Distribution Partners will also include development boards that support the Virtex-E, Virtex-II, Spartan-II and Spartan-IIE series of FPGAs. The table below summarises the two processor cores. Selected Xilinx FPGAs in the new IQ Solutions range have been qualified to operate over the -40ºC to +125ºC temperature range and are targeted for use in automotive applications such as telematics systems.

Soft Processor	Architecture	Bus	MIPS/ Speed	Size	FPGA Support	Support
MicroBlaze	32-bit RISC	Harvard style buses 32-bit instruction and data buses	100 D-MIPs 150MHz	225 CLBs	Virtex Virtex-E Virtex-II Virtex-IIPro Spartan-II Spartan-IIE	Embedded Development Kit (EDK) – soft processor core, peripherals, GNU-based software tools (Compiler, assembler, debugger, and linker)
PicoBlaze	8-bit	8-bit address and data busses	35 MIPS 116MHz	35 CLBs	Virtex Spartan II	Free of charge reference design and application note, assembler

Table 1 Xilinx Soft Processors

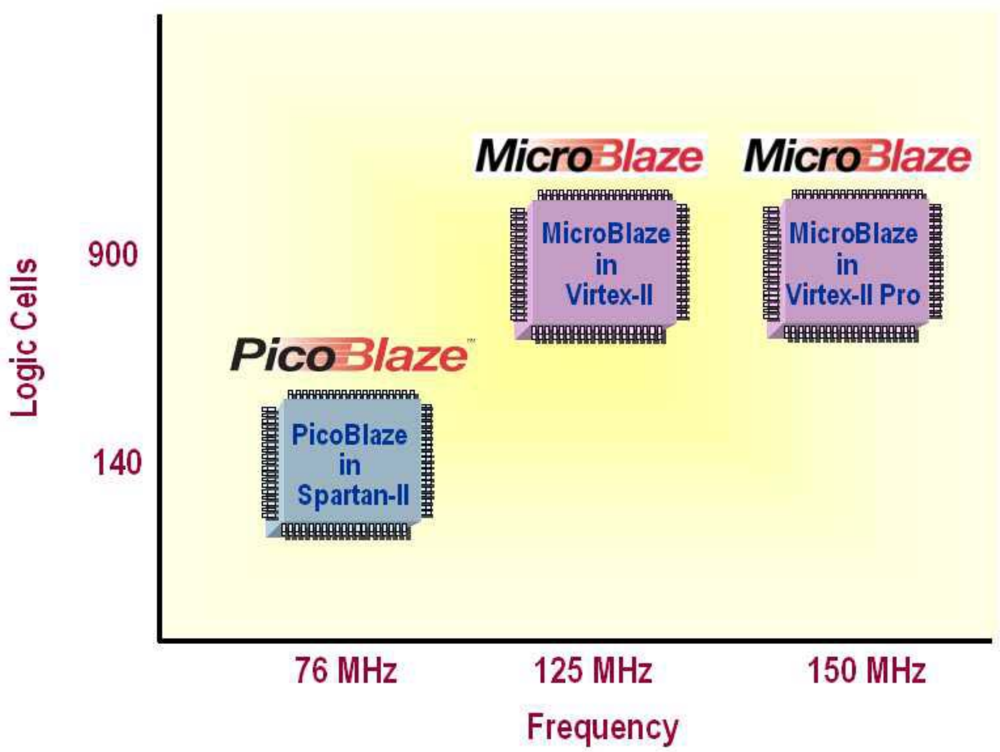

Figure 1 Xilinx PicoBlaze and MicroBlaze Soft Processors showing size in logic cells and speed in MHz

DSP Functions in Hardware

Safety is the number one concern of vehicle customers. Figure 2 shows the result of a study carried out by Visteon, mapping the requirements of its customers and showing vehicle safety at the heart of the hierarchy. This concern is not only for the driver and occupants but for other road users as well. Safety equipment has evolved from the physical to the electronic domain starting with advancements in tyre and braking technology, through side impact protection and airbags, and on to today's 'driver assistance systems'. The latest vehicles are electronics-rich and sensor-based to continuously evaluate the surroundings, display relevant information to the driver and, in some instances, even take control of the vehicle. They hold great promise in increasing the safety, convenience and efficiency of driving.

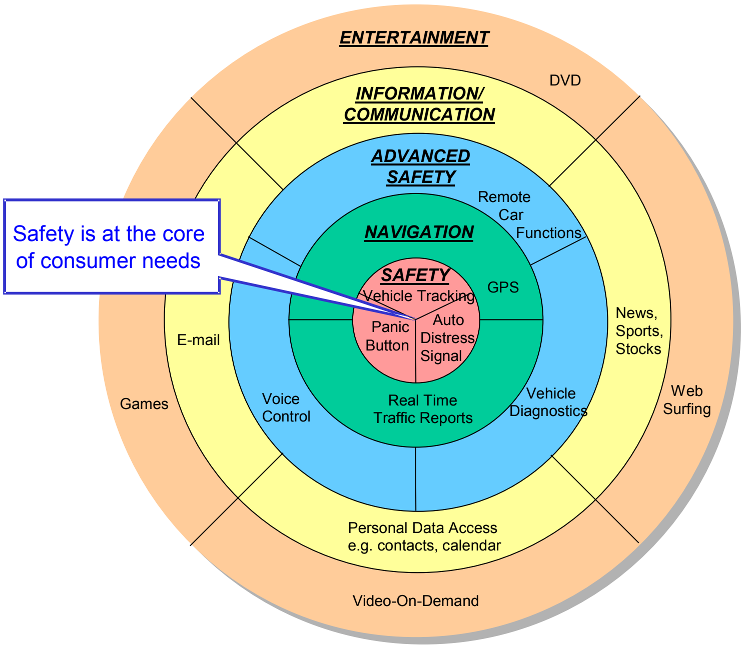

Figure 2 – Hierarchy of Consumer Needs (Courtesy Visteon Corporation)

Driver assistance systems can offer basic safety features, such as adding infrared (IR) cameras for improved visibility. More advanced equipment warns of potentially dangerous situations using a wider array of sensors, enabling the vehicle to be aware of surrounding traffic, lane direction and possible collision objects. The ultimate aim is for the vehicle to be able to react to this information automatically so that its occupants are kept safe, assisting the driver with information and car control. For example, video cameras have been installed in some of the latest trucks to capture images of the lane ahead. If the vehicle changes lanes without using indicators, maybe because the driver is suffering from tiredness, an alert is sounded through the cabin loudspeakers.

Driver assistance can also offer better levels of comfort by removing mundane driving actions. For example, conventional cruise control allows the driver to set a constant travel speed that can be overridden manually when needed. This has now evolved into Adaptive Cruise Control (ACC) which automatically controls the throttle and brakes to match the speed of the vehicle in front and keep a safe distance from it. If the vehicle ahead accelerates away or changes lane, ACC returns to the pre-set speed of the conventional cruise control.

Driver assistance systems also hold the promise of increased traffic efficiency, by using so-called "electronic tow bars". For example, the lead truck in a convoy is driven manually, but the following trucks are driven automatically. As well as taking some of the burden from drivers, the distance between trucks can be greatly reduced because of the faster electronic reaction time. Not only does this save valuable road space, but by travelling in the slipstream of the vehicle in front, fuel savings can be made too.

Xilinx® FPGAs in Driver Assistance Systems

Figure 3 shows a conceptual diagram of a Xilinx Field Programmable Gate Array (FPGA) in an ACC Driver Assistance System.

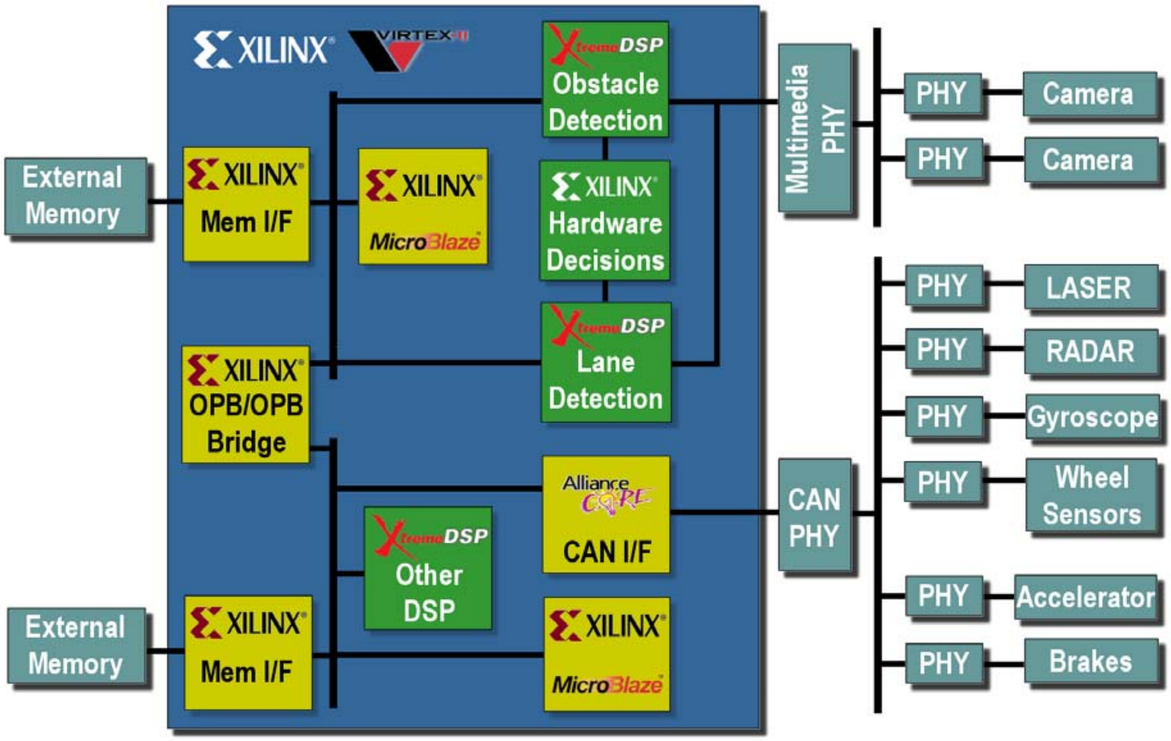

Figure 3 - Concept of FPGA in ACC Driver Assistance System

The system is partitioned into very high-speed input processing and relatively low speed sensor inputs and output control signals, each under the control of its own processor (e.g. a Xilinx MicroBlaze™ 32-bit soft processor or even an embedded IBM PowerPC™ in Virtex-II Pro™ FPGAs). The high-speed section is dedicated to the real-time processing of video coming from the cameras mounted at the front of the vehicle. Real-time processing is absolutely critical due to the nature of the application - crash avoidance, emergency procedures and alerts. Usually two or more cameras will be used to allow the capture of a stereo image, thus enabling calculation of image depth (directly related to real distances from objects) in the FPGA. When combined with radar and laser measurements, plus the information collected from gyros and wheel sensors to detect motion, a very accurate map of the vehicle's surroundings and its path through it can be calculated. Using fully flexible FPGAs, as opposed to off-the-shelf video components, equipment manufacturers can easily develop unique, optimised edge detection, image depth and enhancement algorithms that will differentiate the system performance from that of competitors. Capturing and processing this information in real-time requires the use of maths intensive Digital Signal Processing (DSP) algorithms. However, software processing can't meet the performance requirements and although conventional DSP processors are an alternative, it often needs multiple devices to perform such high-speed tasks. Even ASSP video processors often cannot compare to the extremely high-speed DSP performance of Xilinx FPGAs, also known as XtremeDSP™ processing. After processing the video, the decision tree mechanisms can be partitioned between hardware, for speed-critical algorithms like sudden object avoidance, and processor software, for sounding alerts such as lane drift warnings. Partitioning speed-critical processes into FPGA hardware also enables testing at real-time rates which is impossible in software.

XtremeDSP™ Real-Time Image Processing

So why do Xilinx FPGAs offer faster video processing than conventional DSPs? The fundamental reason is because of the inherent ability to process data in parallel in the FPGA architecture. The latest Virtex-II Pro family of devices from Xilinx also has an array of embedded, high-performance multiplier blocks to increase image-processing power even further. In contrast, a DSP processor takes in successive instructions and data and processes these in a serial fashion. This enables the FPGA to be configured as a large array of Multiply Accumulate (MAC) engines performing multiple operations concurrently (in a single clock cycle) as opposed to multiple cycles required through the one or few MAC engines available in conventional DSPs, as shown in Figure 4.

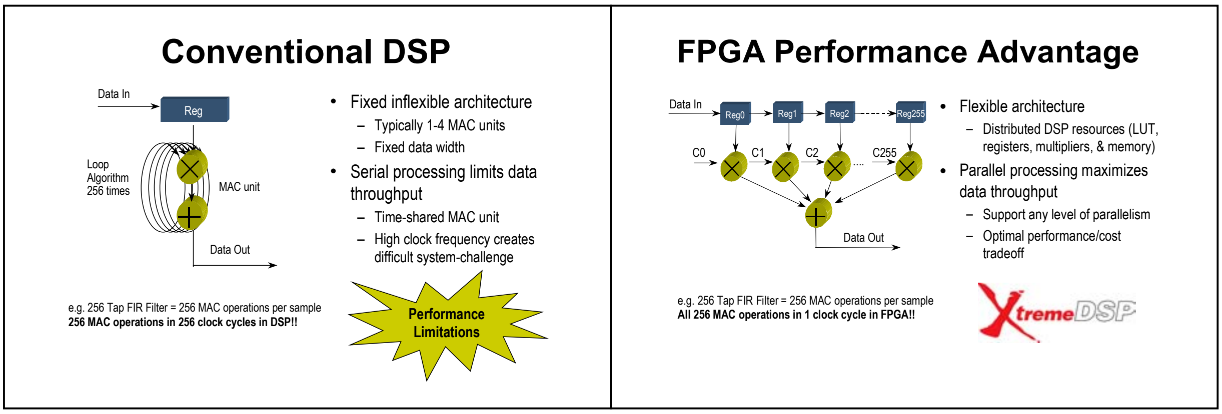

Figure 4 – Conventional DSP versus DSP Functions in FPGAs

Xilinx FPGAs also have the added advantage of enabling the use of an exact size of array to suit the calculation requirements. Such features are ideal for performing calculations on images. Clusters of pixels, such as Discrete Cosine Transform (DCT) macroblocks, can now have calculations performed on them concurrently with other blocks in the picture, rather than having to scan the entire picture sequentially. FPGA performance improvements also lead to the extra benefit that less memory is needed for buffering pixel values, as processing can now be done real-time.

As well as real-time performance, the reprogrammability of Xilinx FPGAs also offers superb system flexibility, enabling algorithm upgrades to be made even after deployment. This is important, as current driver support systems are still in the early days of research and development. As edge and object detection algorithms are improved over time, hardware upgrades can be done in a matter of minutes and no board redesign is required.

Bridging Automotive Networks with Programmable Peripherals

As the vehicle evolves into a truly networked area, the equipment manufacturer somehow needs to determine which standard will be the most successful or offer them the greatest advantage over other network protocols. Various network technologies have emerged that cover different requirements in the car, ranging from multimedia networks in the cockpit such as Media Oriented Systems Transport (MOST) to car control networks like FlexRay. In Figure 3, a pre-verified Controller Area Network (CAN) interface core was chosen as an example.

One of the real benefits of using an FPGA rather than an ASSP is that it allows engineers to produce designs that precisely match the interfaces and peripherals to the system requirements. This is particularly useful when trying to interface to various automotive networks that are in the early stages of development. When trying to get a product to market quickly, chipset or ASIC re-spins are costly and time consuming. If the specification of a network protocol changes during a standard's early days, all it takes to support the latest revision in an FPGA is a relatively simple redesign in software and a new download of the hardware configuration. This can even be done over a wide area network using Xilinx IRL™ (Internet Reconfigurable Logic) so the hardware can be revised during maintenance without costly truck rolls or extra manpower.

Xilinx IQ Solutions for Automotive Applications

To address the needs of automotive electronics equipment designers Xilinx has created a new range of devices with an extended industrial temperature range option. Called the “IQ” range, it comprises of current Xilinx industrial grade (I) FPGAs and CPLDs qualified to a new extended temperature grade (Q) as shown in Table 2. The first products qualified to operate at the new temperature grade are Spartan-XL™ 3.3V FPGAs ranging from 5K gates to 30K gates, and the 36 and 72 macrocell XC9500XL™ 3.3V CPLDs. Over the coming months the IQ range will be expanded to include FPGA devices up to 300K gates and CPLDs up to 512 macrocells in density, as shown in Table 3.

	Temperature Grade/Range °C		
Product	**C**	**I**	**Q**
FPGA	T_J = 0 to +85	T_J = -40 to +100	T_J = -40 to +125
CPLD	T_A = 0 to +70	T_A = -40 to +85	T_A = -40 to +125

Table 2 - Temperatures supported by Xilinx Products

	Xilinx IQ Solutions Silicon Selector		
Product Family	**Packages**	**Voltage**	**Density Range**
XC9500XL CPLDs	VQ44, VQ64, TQ100	3.3V	36 - 72 Macrocells
CoolRunner XPLA3 CPLD	VQ44, VQ100, TQ144, PQ208	3.3V	32 - 512 Macrocells
CoolRunner II CPLD	VQ44, VQ100, TQ144, PQ208	1.8V	32- 512 Macrocells
Spartan XL FPGA	VQ100, TQ144, PQ208, BG256	3.3V	5K - 40K Gates
Spartan II FPGA	TQ144, PQ208, FG256,	2.5V	15K - 200K Gates
Spartan IIE FGPA	TQ144, PQ208, FT256, FG456	1.8V	50K - 600K Gates

Table 3 – Xilinx IQ Solutions Silicon for Automotive Applications

Conclusion

Xilinx soft processor cores such as MicroBlaze and PicoBlaze when embedded in FPGA fabric can eradicate processor obsolescence issues by providing a stable platform owned and configured by the automotive designer. In combination with the new IQ Solutions range of FPGAs, qualified to extended temperature, they are ideal for automotive applications. Not only can you benefit from the flexibility, integration and upgradeablilty offered by programmable logic but you can take advantage of a processor tailored to your design needs that will not go obsolete.

The new wave of driver assistance systems requires high performance image processing, but without sacrificing the flexibility required during early stages of research and development of object detection and automotive network technologies. The use of Xilinx FPGAs at the heart of such systems offers the industry's best DSP performance and unrivalled support for network connectivity standards and gives system architects a fully flexible design platform to work on. By enabling these systems to work in real-time, it is now possible to provide emergency driver alerts or assisted car control and significantly increase safety.

Further Information

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www.xilinx.com/microblaze	MicroBlaze Information
www.xilinx.com/picoblaze	PicoBlaze Information

Glossary

ACC – Automatic Cruise Control
ASIC – Application-Specific Integrated Circuit
ASSP – Application Specific Standard Product
CAN – Controller Area Network
CLB – Configurable Logic Block
CPLD – Complex Programmable Logic Device
DAB – Digital Audio Broadcast
DIN - Deutsches Institut für Normung e.V. (German Institute for Standardization; similar to US ANSI)
DCT - Discrete Cosine Transform
DSP – Digital Signal Processor
FM – Frequency Modulation
FPGA – Field Programmable Gate Array
GSM - Global System for Mobile Communication
GPRS – General Packet Radio Service
IR – Infra Red
IRL – Internet Reconfigurable Logic
LTB – Last Time Buy
MOST – Media Oriented Systems Transport
PROM - Programmable Read-Only Memory
PCB – Printed Circuit Board
UART - Universal Asynchronous Receiver-Transmitter