XILINX®

Xilinx IQ Solutions for Automotive Intelligence

Xilinx IQ Products for Automotive Applications

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Overview

- PLDs in the Automotive sector
- How PLDs fits in Telematics & Infotainment
- Multimedia Platforms
- Applications Overview
- Reliability Verification
- Summary

Telematics - A New Platform for Service Delivery

- **Perfect application for programmable logic solutions**
- **Benefits from re-programmable platform**
  - **New applications/services, user interface, look & feel, etc.**

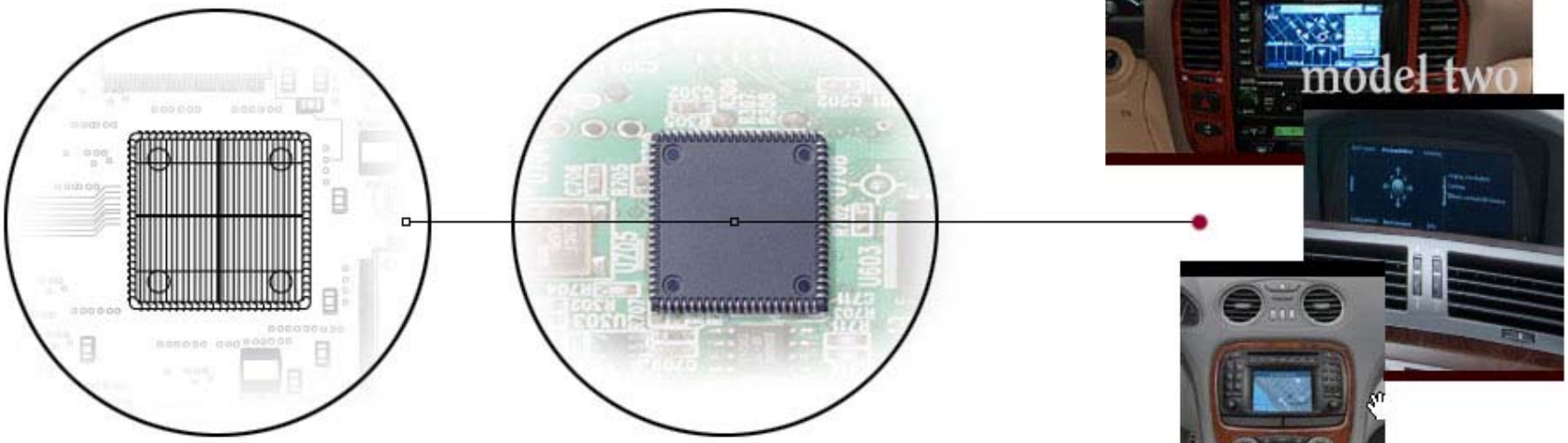
- **System Technology:** 2G or 3G mobile, satellites, RDS, Bluetooth, WAP, DAB, DVD, etc.
- **Mobile Multimedia:** traffic information, internet access, electronic games, pay-TV, advertising, MPEG music downloads, digital radio broadcasting and mobile commerce services

MultiMedia Products

From the Lab to the Road - Multimedia Platform Design

Prototype

Production



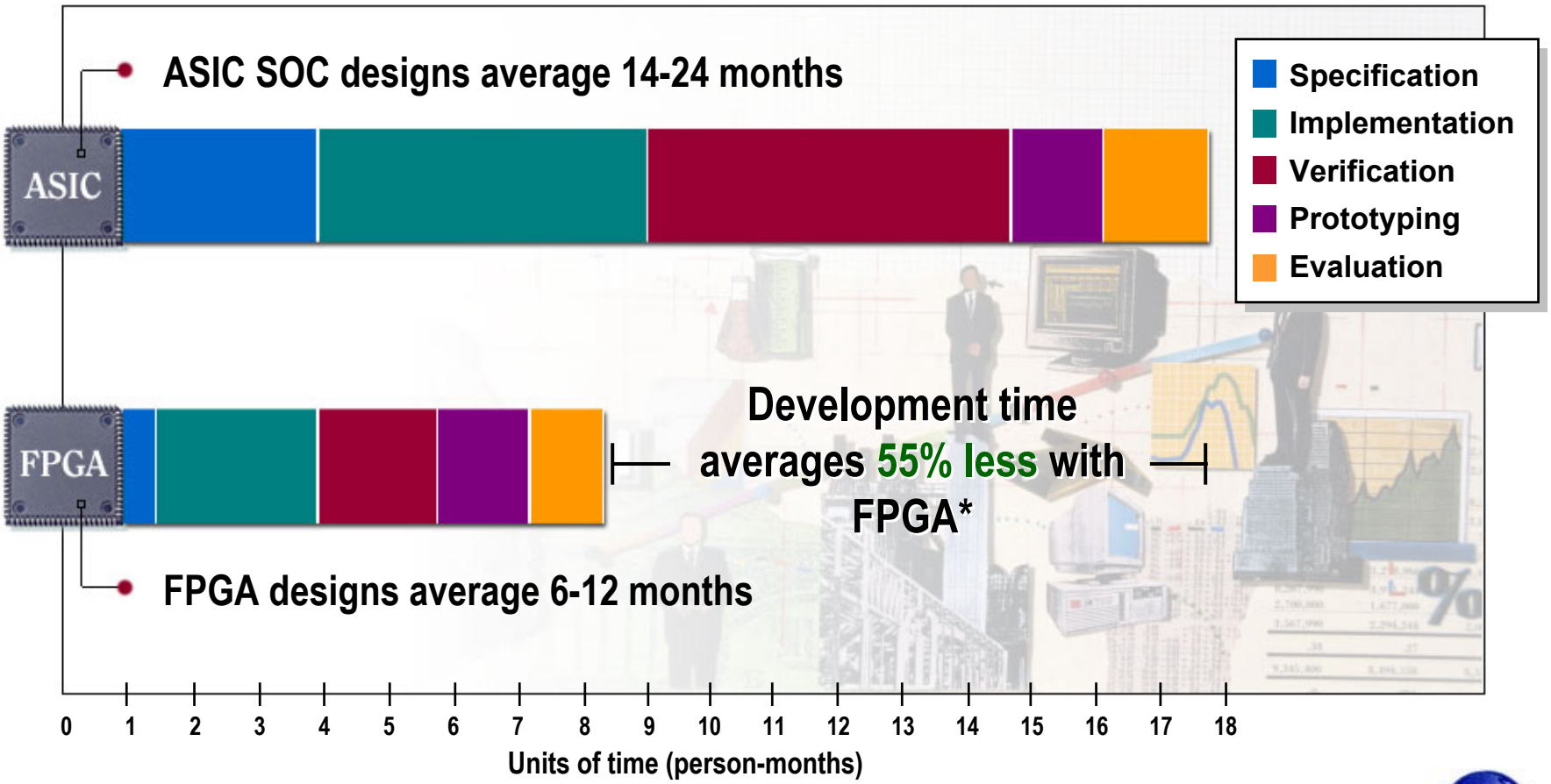
- Develop system
- Integrate functionality / new standards
- Evaluate operation

Large FPGAs

- Flexible and field upgradeable
- Single platform, multiple manufacturing variations
- Customized look & feel
- New features, functions
- Requires extended temperature operation

Smaller Low Cost FPGAs for Production

Shorter Development Cycles Increase Revenue Potential



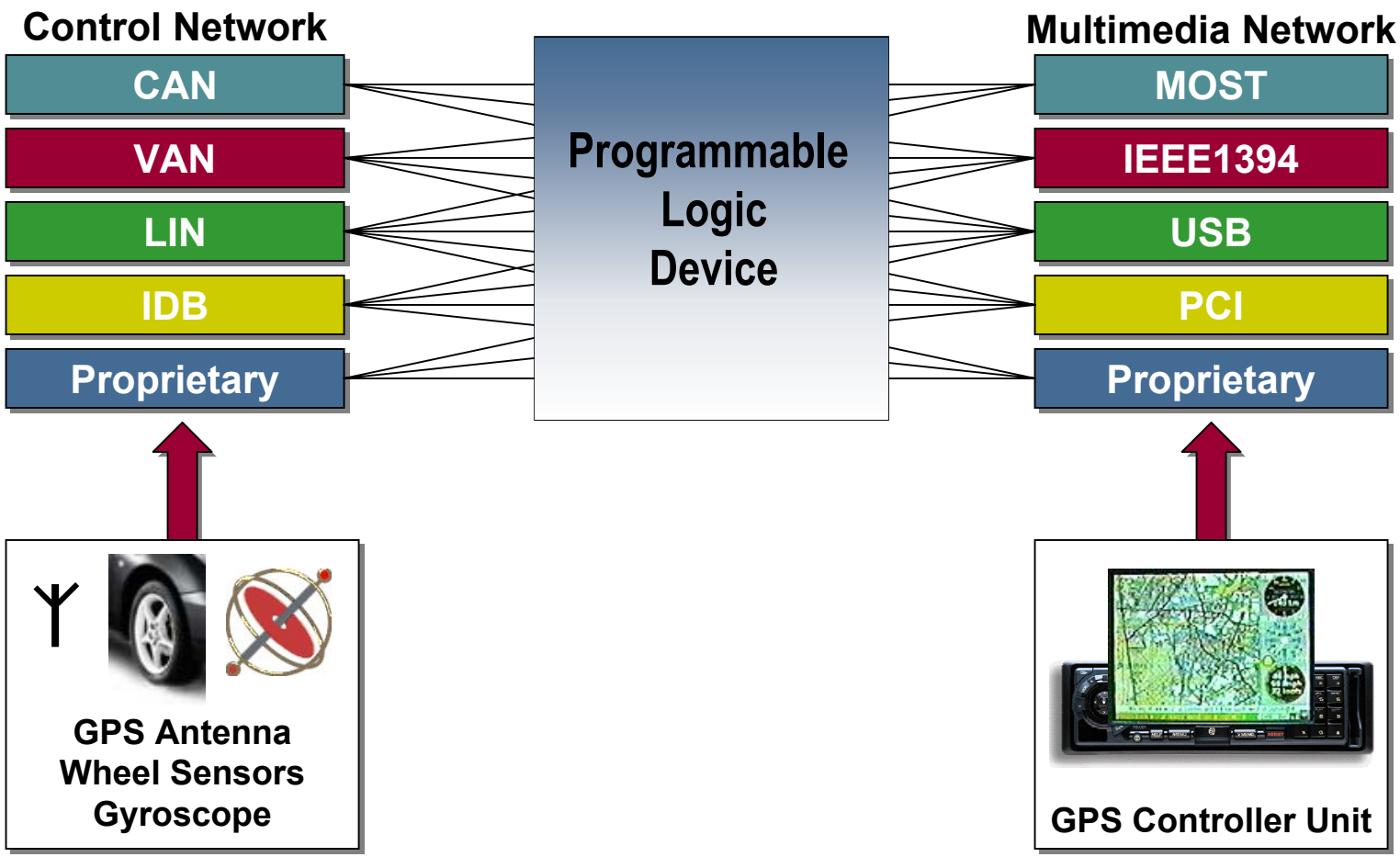
Source: Harvard Study

* Based on an average of 391 different sized designs

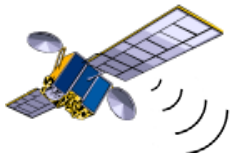
In-Car Digital Convergence

- Technologies are based on multiple, new and changing standards
  - Bluetooth, WAP, GPS, MOST, CAN, etc.
- Integration of multiple complex technologies in auto environment
  - Display, computing, audio, RF, etc.
- Requires flexible solution
- Time-to-market pressures as automotive is shrinking from 6 to 2 years
- Traditional solution challenges
  - Microcontroller - insufficient compute capability
  - ASIC - design cycle flexibility, upgradeability

Bridging Automotive Networks



In-Car GPS Receiver



RF In

Clock Gen and DLLs

Drive Interface

Drive Unit

CD/DVD

RF Tuner

Filtering and Formatting

Graphics Controller

LCD Screen

Wheel Sensors

ADC

CPU

PCI Bridge

PCI Plug-In Modules

Gyros

ADC

CAN Interface

Control Area Network

Microphones

ADC

DSP Noise Cancellation

HCI Bridge

Bluetooth Module

Audio DAC

Speakers

User Interface

Front Panel

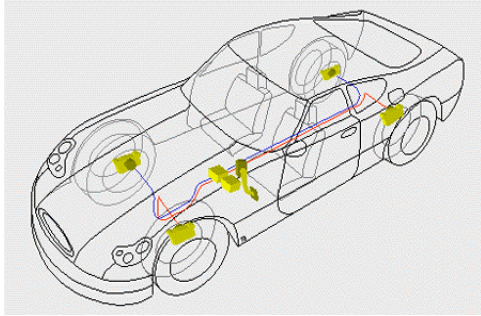
Memory Controller

FLASH

SDRAM

Xilinx | Memory | CPU | Non-Xilinx | Mixed Signal

X-by-Wire



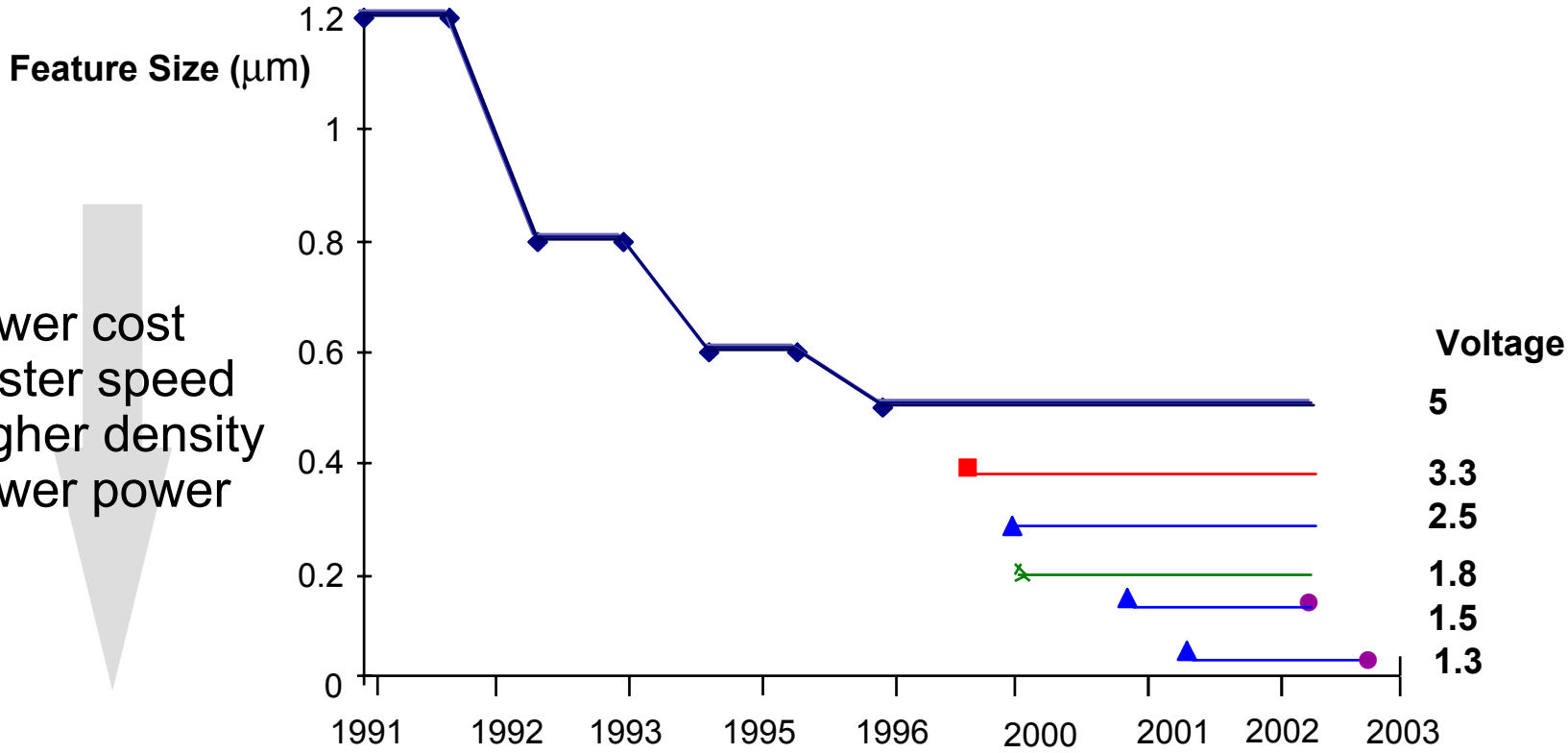
- Replacing mechanical and hydraulic systems with communications busses to control:
  - Throttle, Steering, Braking, traction control etc
- Real-time response needed (paralleling the CPU? DSP Co-processing?)
- Special interrupt/safety/task structure needed
- Hardware based designs are less prone to software based `bugs`
- New way of designing with FPGA based reconfigurable hardware:
  - Prototype and testing with FPGAs - concept proving/quick changes
  - Pre-production with low cost FPGAs (shrink/optimise designs)
  - Production move to ASIC? (Depending on NRE charges and risk)
- Field/customer feedback on additional functionalities required can be added during development and/or production

Safety and Security

- Utilizing the power of IRL units that are stolen can be de-activated remotely over any network
- Functions implemented in Hardware (programmable logic) can be fully tested vs. software in embedded microprocessors
  - 200MHz + in PLDs vs. 20MHz in Microcontrollers
  - PLDs can be used as a system co-processors for fast operations and interfaces
  - Coding in hours vs. days
  - Functions can be re-used and created as a ‘standard’ application ‘core’ or ‘macro’ to be shared by engineers

Process Technology and Supply
Voltage Roadmap

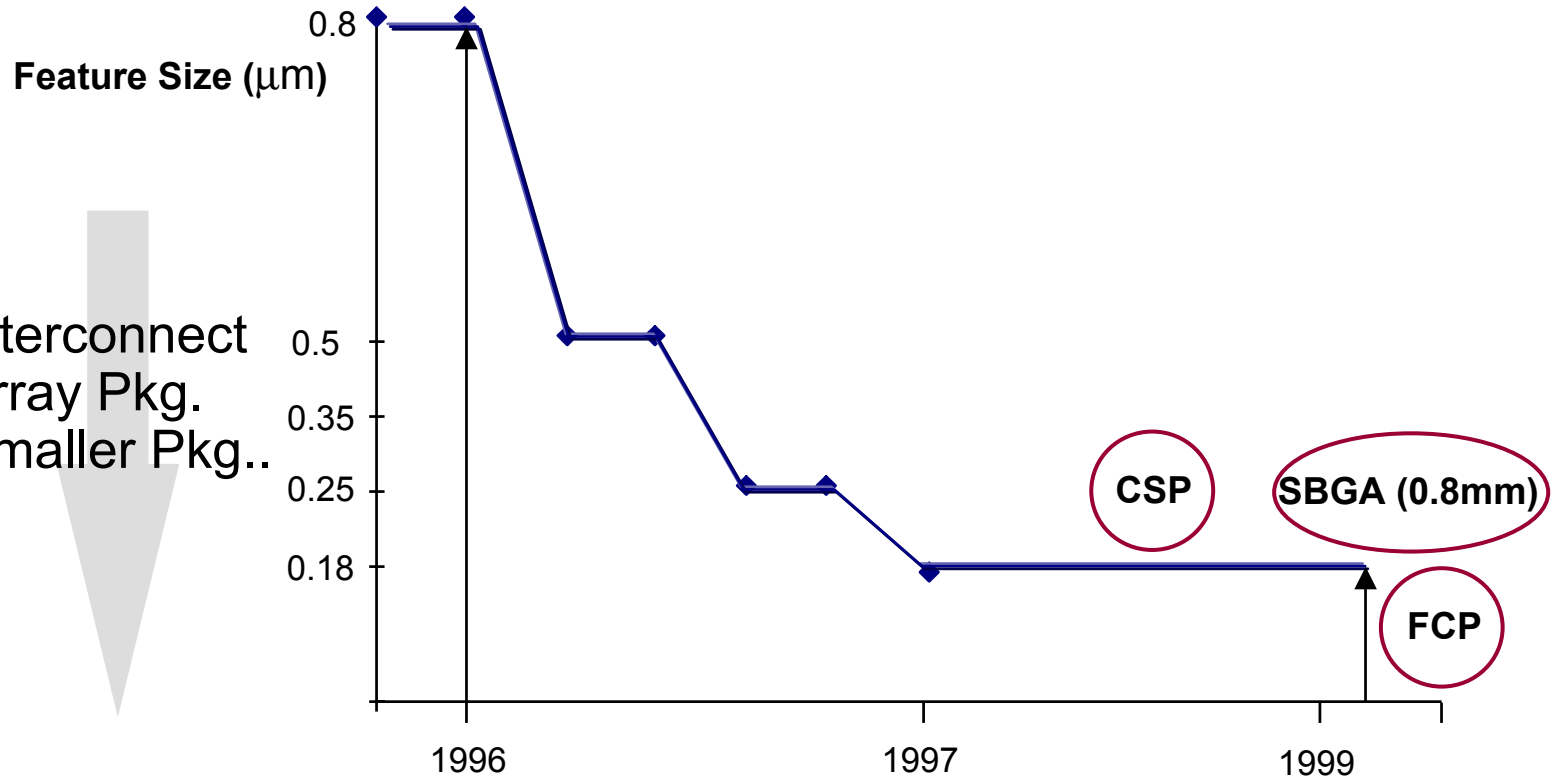
- Lower cost
- Faster speed
- Higher density
- Lower power



Xilinx fab partners use FPGAs to drive their process

Package Density Drivers (Lead Pitch)

- Interconnect
- Array Pkg.
- Smaller Pkg..



- Package Interconnect must shrink with die-size resulting to Array Packaging instead of Perimeter
- Aimed at smaller size packages
- High Performance / Frequency / Density Designs
- Efficient Cost

Xilinx Quality Standard Roadmap

Industry Quality Standards…
A Journey to Quality Excellence

former

ISO9000/QML/PURE

- ISO-9000:1994 meet minimum requirements
- QML, PURE Certified
- ISO-14000 (Q4CY2001)
- Quality systems
  - focus on re-establization
  - Meet customer rqts.
- Wim's Quality Initiatives
  - Internalize worldwide
  - WW training
  - Continuous drive needed as part of our "values"

TODAY

ISO9000/QML/PURE

ISO-9000:2000

- Emphasis on continuous improvement
- Customer input is significant
- Top management quality review
- Analysis & Use of Data (FOL --> EOL, SPC, Metrics)

■ **Completed in July 02**

Q4' CY03

ISO9000/QML/PURE/TL9000

TL9000 (Telec. Stds.)

- Telecom Industry Standards
- Design Control, NPI, Traceability/ Prod. I.D., Product Lifecycle, PCN/PDN)
- Significant Involvement and Participation of Top Mgmt (Software, Hardware)
- Emphasis on continuous improvement and customer satisfaction
- High on balanced metrics and communication systems, tracking results
  - ➢Supplier - customer relationship
  - ➢performance feedback
  - ➢problem escalation & resolution

Q1' CY05

ISO9000/QML/PURE/ TL9000/QS9000

QS9000 or TS16949

- Systems Expectations for Automotive Industry
- Customer and Supplier relationship
- Top Mgmt Involvement
- Design Process Control
  - ➢Design Control, NPI, Traceability/ Prod. I.D., Product Lifecycle, PCN/PDN)
- Specific Emphasis on statistical tools & techniques continuous improvement
  - ➢Gauge R&R; SPC Charts, FMEA

System Reliability

- For system failure rates, the relationship is quite simple (i.e the sum of the failure rates of all the individual components)

$$h_s(t) = \sum_{i=1}^{n} h_i(t)$$

- PLD's reduce the number of components in a system (fewer solder connections, fewer devices)
- Increasing levels of integration in automotive
  - e.g car radio is now integrated into dashboard system

Process Qualification Tests

TABLE I

2.1 New Wafer Process Qualification

Reliability Test	Condition	Duration	Lot Qty	SS/lot[A]	Acceptance
High Temperature Operating Life (HTOL)	Ta >=125°C, $V_{DD\ Max}$	1,000 hours	3	76	0 fail
Temperature Humidity Bias (THB)	85°C, 85% R.H., V_{DD}	1,000 hours	2	76	0 fail
Temperature Cycling (TC)	-65°C/+150°C or -55°C/+125°C[B]	500 cycles or 1,000 cycles	1	76	0 fail
High Temperature Storage (HTS)[C]	Ta = 150°C	1,000 hours	1	76	0 fail
Data Retention[D]	Ta = 150°C	1,000 hours	1	76	0 fail
Program Erase[C,D]	Ta = 75°C	10,000 cycles	1	76	0 fail

Note: A. The sample size listed is based on the die size </= 237 mm^2. For bigger die size, the sample size may be reduced.

B. For plastic flat pack packages use conditions of -65°C/+150°C, the duration is 500 cycles.
For ball grid array packages use conditions of -55°C/+125°C, the duration is 1000 cycles.

C. This is not a mandatory test.

D. For CPLD and Eprom products only

E. Package precondition is performed prior to THB & TC tests.

Package Qualification Tests

TABLE I Continued

2.2 New Non-Hermetic Package/Assembly Qualification:

Reliability Test	Condition	Duration	Lot Qty	SS/lot[A]	Acceptance
Temperature Humidity Bias (THB) or High Accelerated stress Test (HAST)	85°C, 85% R.H., V_{DD} or 130°C, 85% R.H., V_{DD}	1,000 hours	1	76	0 fail
Temperature Cycling (TC)[B]	-65°C/+150°C, -55°C/+125°C, -40°C/+125°C or -0°C/+100°C	500 cycles or 1,000 cycles	1	76	0 fail
Autoclave or Moisture Resistance	121°C, 100% R.H.or 85°C, 85% R.H	96 hours 1,000 hours	1	76	0 fail
Resistance to Solvent			1	3	0 fail
Solderability			1	3	0 fail
Lead Fatigue			1	3	0 fail
Ball Shear			1	5(40)[C]	0 fail
Bond Pull			1	5 (40)[C]	0 fail

Note:

A. The sample size listed is based on the die size </= 237 mm^2. For bigger die size, the sample size may be reduced.

B. For plastic flat pack packages use conditions -65°C/+150°C, the duration is 500 cycles.
For ball grid array packages use conditions -55°C/+125°C, the duration is 1,000 cycles.
For Flip chip packages use conditions -40°C/+125°C, the duration is 500 cycles and conditions -040°C/+100°C, the duration is 1,000 cycles.

C. Five units w/ a total of 40 balls or bonding wires.

Device Qualification & Rel Monitor

2.3 New Device Qualification:

For a new device from a previously qualified process, the requirements are as follows:

Reliability Test	Condition	Lot Qty	SS/lot[A]	Acceptance
ESD	HBM	1	3	>=2000V
Latch up	Current injection Ta =25°C	1	4	>=200mA

2.4 Hermetic Packages: The hermetic package qualification requires a full group D test per MIL-STD-883, Method 5005.

2.5 Reliability Monitor

2.5.1 Wafer Process

Reliability Test	Condition	Duration	Lot Qty	SS/ process family/quarter	Acceptance
High Temperature Operating Life (HTOL)	Ta >=125°C $V_{DD\ Max}$	1,000 hours	1	45	0 fail
Data Retention[A]	Ta=150C	1,000 hours	1	45	0 fail
Extended Static Life Test	Ta >=125°C $V_{DD\ Max}$	2,000 hours	1[B]	45	0 fail

A- For CPLD and Eprom products only.
B. 1 of the lot that is pulled per quarter is extended to 2,000 hours.

Package Rel Monitor

2.5 Reliability Monitor (cont'd)

2.5.2 Package/ Assembly (Monitor)

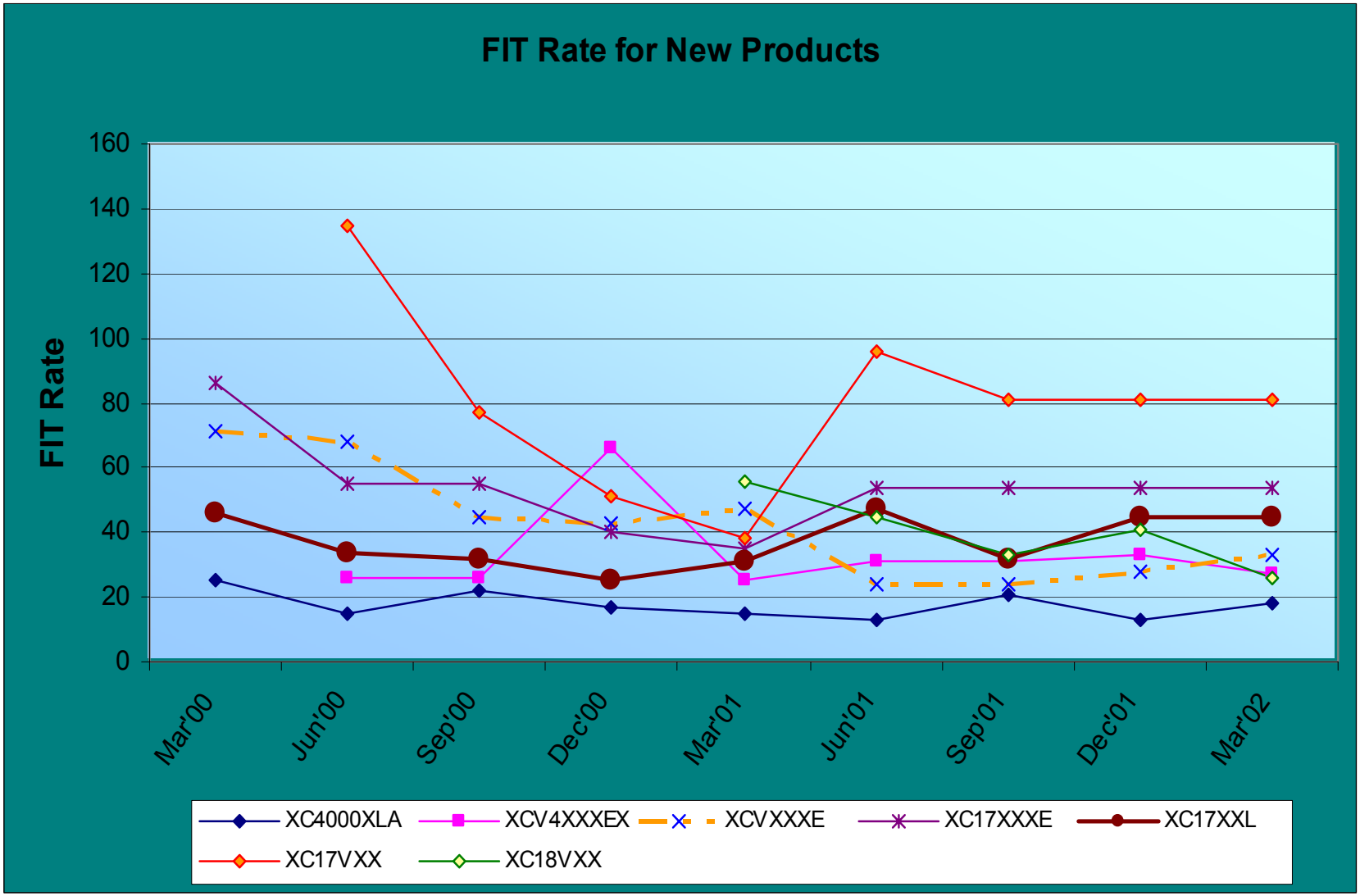
Reliability Test	Condition	Duration	Lot Qty	SS/ site /pkg family/quarter	Acceptance
Temperature Humidity Bias (THB) or	85°C, 85% R.H., V_{DD}	1,000 hours	1	45	0 fail
High Accelerated stress Test (HAST)	130°C, 85% R.H., V_{DD}	100 hours	1	22	0 fail
Temperature Cycling (TC) [B]	-65°C/+150°C , -55°C/+125°C, -40°C/+125°C or -0°C/+100°C	500 cycles or 1,000 cycles	1	45	0 fail
Autoclave or Moisture Resistance	121°C, 100% R.H. or	96 hours	1	45	0 fail
Solderability			1	3	0 fail
Mark Permanency			1	3	0 fail
Lead Fatigue			1	3	0 fail
Physical Dimension			1	5	0 fail

Note:

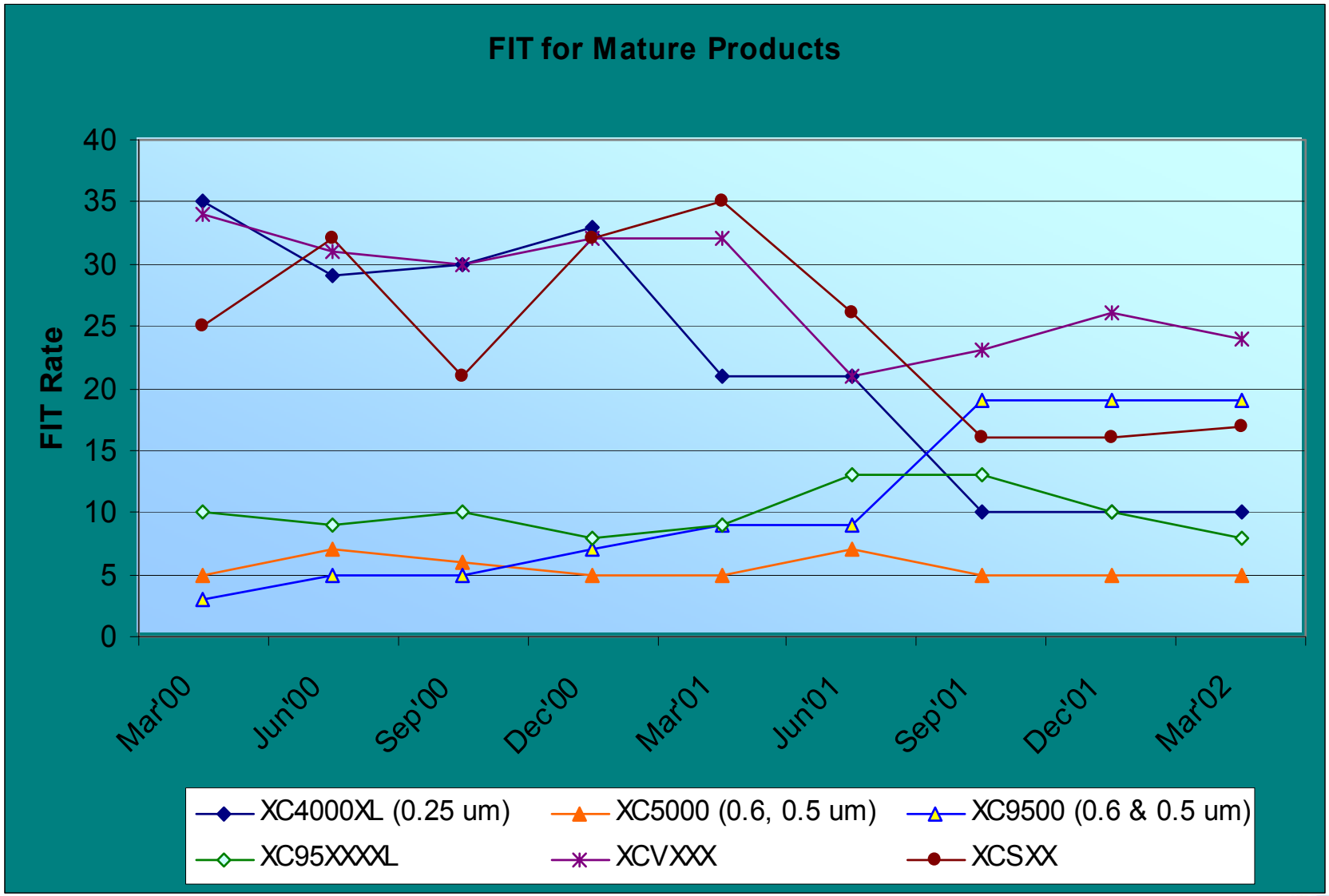
A. The sample size listed is based on the die size </= 237 mm^2. For bigger die size, the sample size may be reduced.

B. For plastic flat pack packages use conditions -65°C/+150°C, the duration is 500 cycles.
For ball grid array packages use conditions -55°C/+125°C, the duration is 1,000 cycles.
For Flip chip packages use conditions -40°C/+125°C, the duration is 500 cycles and conditions -040°C/+100°C, the duration is 1,000 cycles.

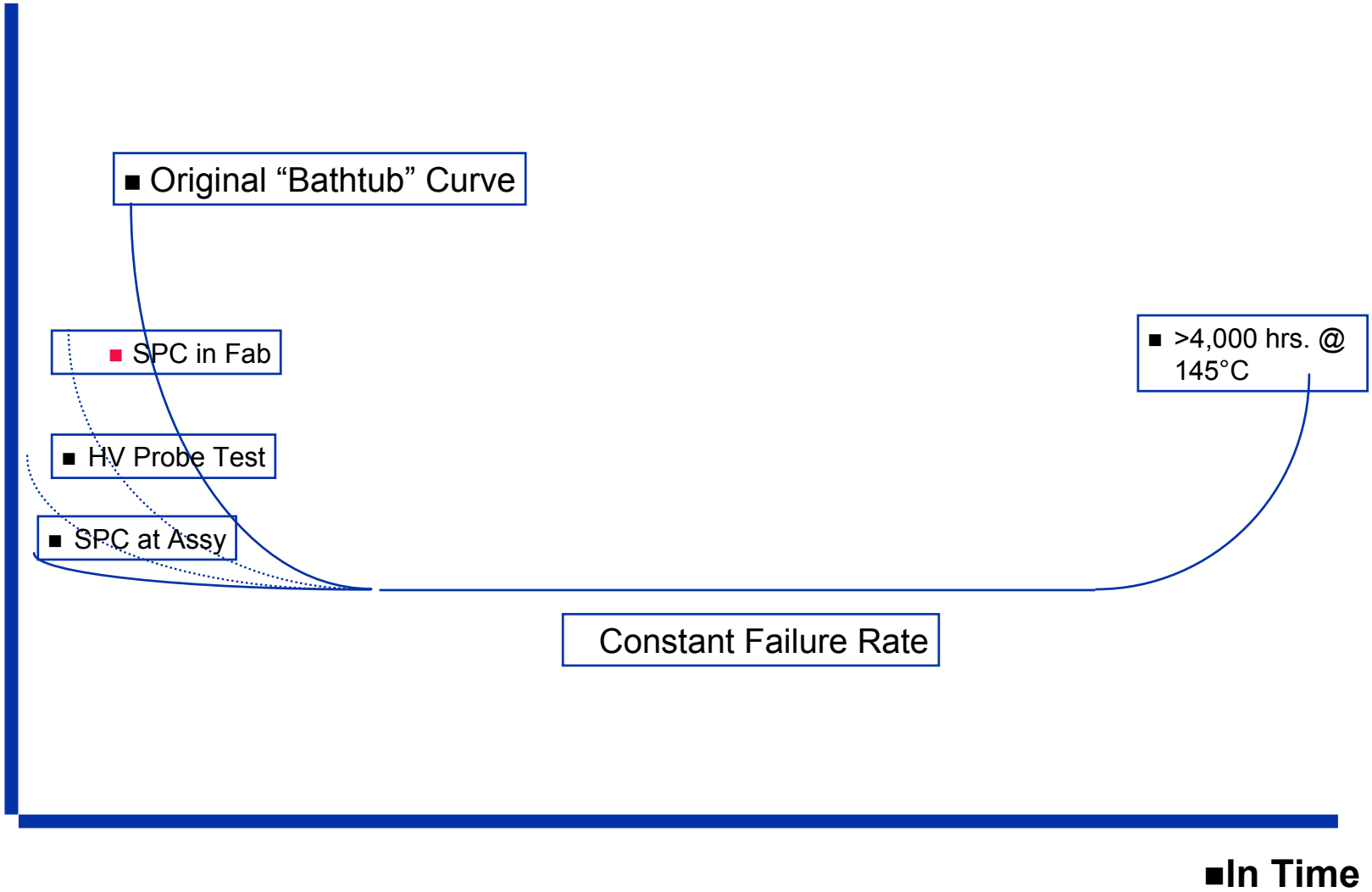
Reliability Fit Rate: 2 years Rolling



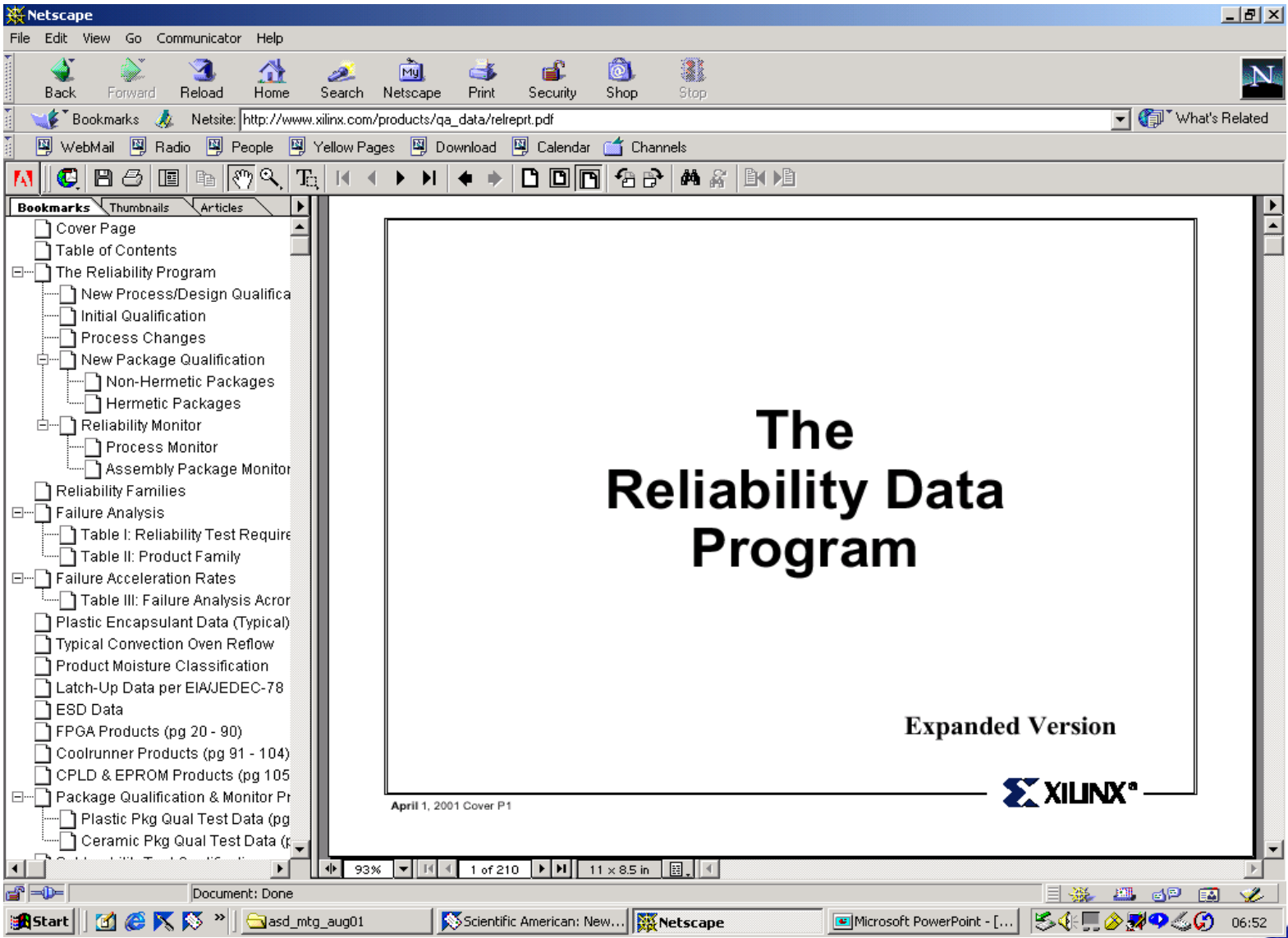
Reliability Fit Rate: 2 years Rolling



Failure Rate Curve



http://www.xilinx.com/products/qa_data/relreprt.pdf



Introducing IQ Products

- Why IQ?
  - New range of devices with an extended Industrial Temperature option
  - Consists of CPLD and FPGA families already available in I Grade - and the addition of selected devices with an extended temperature 'Q' grade option
  - *IQ - it's the intelligent choice for Automotive designers!!*
- For FPGAs Q grade means:
  - -40°C to +125°C Junction Temperature
- For CPLDs Q Grade means:
  - -40°C to +125°C Ambient Temperature

Ambient = the temperature of the air surrounding the device
Junction = is the temperature of the die in the package

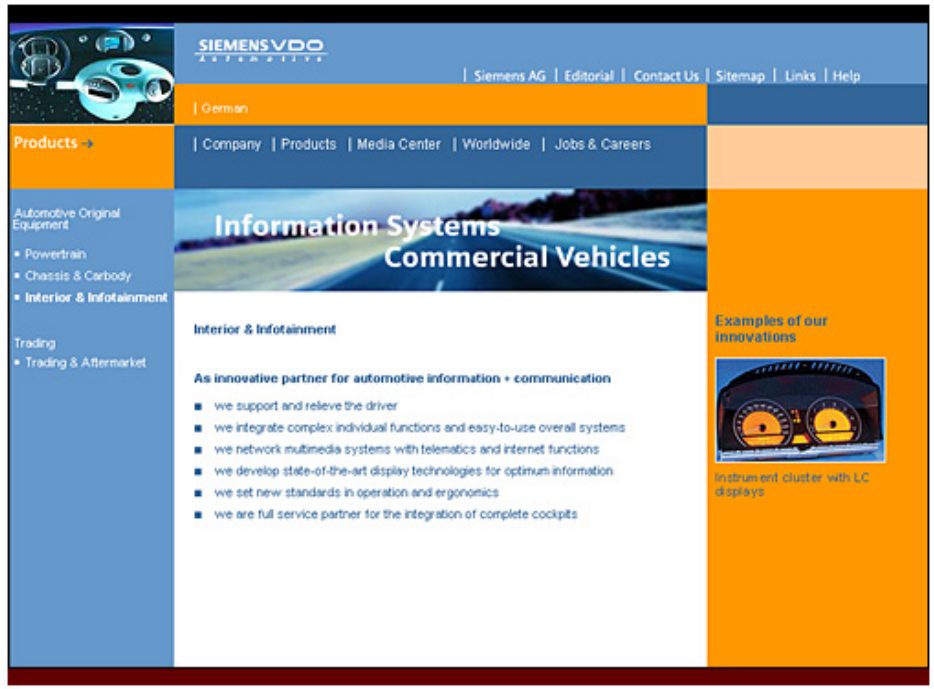
Automotive SSB Solutions

- Divio
  - Digital video decoder & CODEC
    - Based on Xilinx Spartan-II FPGA
    - Single chip DV codec
    - Separate 1394 link layer & PHY

- ACUNIA
  - CarCube™: prototype design for in-vehicle telematics terminal, based on XINGU® 8000 series processing platform, featuring:
    - Intel® Xscale™ micro-architecture
    - Xilinx Spartan-II FPGA companion chip

Xilinx in Infotainment Systems Today

- Siemens VDO Dayton MP3 car radio CD
  - Spartan-II FPGAs
    - Perform peripheral interfacing and audio control
  - Selected for
    - Ability to upgrade via reprogrammability to accomodate changing standards
    - Ease-of-use
    - Low cost



- Siemens VDO has been using Xilinx FPGAs for its advance in-car systems since 1997

Summary

- The fastest growing area for semiconductors in the automotive sector today is in-car applications
- Different mobile technologies are merging and will be combined in new car solutions - consumer product business models plus wireless communication challenges must be met
- Multimedia platforms are being developed to provide bespoke in-car infotainment using one common reconfigurable platform
- Reconfigurable logic devices
  - *shorten time to market*
  - *lengthen time in market*
  - *allow for for changing standards and protocols*
  - *provide lower total solution costs*