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XILINX FPGA PACKAGE OPTIONS AND USER I/O

			Virtex-II (1.5V)											Virtex-E (1.8V)												V-EM		Spartan-IIE (1.8V)						Spartan-II (2.5V)					
			XC2V40	XC2V80	XC2V250	XC2V500	XC2V1000	XC2V1500	XC2V2000	XC2V3000	XC2V4000	XC2V6000	XC2V8000	XCV50E	XCV100E	XCV200E	XCV300E	XCV400E	XCV600E	XCV1000E	XCV1600E	XCV2000E	XCV2600E	XCV3200E	XCV405E	XCV812E	XC2S50E	XC2S100E	XC2S150E	XC2S200E	XC2S300E	XC2S15	XC2S30	XC2S50	XC2S100	XC2S150	XC2S200
Pins	**Body Size**	**I/O's**	88	120	200	264	432	528	624	720	912	1104	1296	176	176	284	316	404	512	660	724	804	804	804	404	556	182	202	263	289	329	86	132	176	196	260	284
PQFP Packages (PQ)																																							
208	28 x 28 mm																										146	146	146	146	146		132	140	140	140	140
240	32 x 32 mm													158	158	158	158	158	158	158																		
HQFP Packages (HQ)																																							
240	32 x 32 mm														158				158																				
VQFP Packages (VQ)																																							
100	14 x 14 mm																															60	60					
TQFP Packages (TQ)																																							
144	20 x 20 mm																										102	102				86	92	92	92			
Chip Scale Packages — wire-bond chip-scale BGA (0.8 mm ball spacing)																																							
144	12 x 12 mm		88	92	92									94	94	94																86	92					
BGA Packages (BG) — wire-bond standard BGA (1.27 mm ball spacing)																																							
352	40 x 40 mm														196	260	260																						
432	40 x 40 mm																316	316	316																				
560	42.5 x 42.5 mm																	404	404	404	404	404			404	404													
575	31 x 31 mm						328	392	408																														
728	35 x 35 mm								456	516																													
FGA Packages (FT) — wire-bond fine-pitch thin BGA (1.0 mm ball spacing)																																							
256	17 x 17 mm																										182	182	182	182	182							
FGA Packages (FG) — wire-bond fine-pitch BGA (1.0 mm ball spacing)																																							
256	17 x 17 mm		88	120	172	172	172							176	176	176	176																	176	176	176	176
456	23 x 23 mm				200	264	324									284	312											202	263	289	329				196	260	284
676	27 x 27 mm							392	456	484								404	444						404													
680	40 x 40 mm																		512	512	512	512																
860	42.5 x 42.5 mm																			660	660	660																
900	31 x 31 mm																		512	660	700					556											
1156	35 x 35 mm																			660	724	804	804	804														
FFA Packages (FF) — flip-chip fine-pitch BGA (1.0 mm ball spacing)																																							
896	31 x 31 mm						432	528	624																														
1152	35 x 35 mm									720	824	824	824																										
1517	40 x 40 mm										912	1104	1108																										
BFA Packages (BF) — flip-chip fine-pitch BGA (1.27 mm ball spacing)																																							
957	40 x 40 mm								624	684	684	684	684																										

Note: Virtex-II packages FG456 and FG676 are footprint compatible.
Virtex-II packages FF896 and FF1152 are footprint compatible.
Important: Verify all Data with Device Data Sheet

Numbers indicated in the matrix are the maximum number of user I/O's for that package and device combination.

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XILINX FPGA PRODUCT SELECTION MATRIX

		CLB Resources					BLK RAM		CLK Resources					I/O Features				Speed				
	System Gates (see note 1)	CLB Array (Row X Col)	Number of Slices	Logic Cells (see note 2)	CLB Flip-Flops	Max. Distributed RAM Bits	# Block RAM Blocks	Block RAM Bits	# Dedicated Multipliers	DLL Frequency (min/max)	# DLL's	Frequency Synthesis	Phase Shift	Digitally Controlled Impedance	Number of Differential I/O Pairs	Max. I/O	I/O Standards	Commercial Speed Grades (slowest to fastest)	Industrial Speed Grades (slowest to fastest)	Serial PROM Family		Config. Memory (Bits)
Virtex-II Family — 1.5 Volt																						.15um Eight Layer Metal Process
XC2V40	40K	8 x 8	256	576	512	8K	4	72K	4	24/420	4	DCM	DCM	YES	44	88	LDT-25, LVPECL-33,	-4 -5 -6	-4 -5	ISP	OTP	0.4M
XC2V80	80K	16 x8	512	1,152	1,024	16K	8	144K	8	24/420	4	DCM	DCM	YES	60	120	LVDS-33, LVDS-25,	-4 -5 -6	-4 -5			0.6M
XC2V250	250K	24 x16	1,536	3,456	3,072	48K	24	432K	24	24/420	8	DCM	DCM	YES	100	200	LVDSEXT-33, LVDSEXT-25,	-4 -5 -6	-4 -5			1.7M
XC2V500	500K	32 x 24	3,072	6,912	6,144	96K	32	576K	32	24/420	8	DCM	DCM	YES	132	264	BLVDS-25, ULVDS-25,	-4 -5 -6	-4 -5			2.8M
XC2V1000	1M	40 x 32	5,120	11,520	10,240	160K	40	720K	40	24/420	8	DCM	DCM	YES	216	432	LVTTL, LVCMOS33,	-4 -5 -6	-4 -5			4.1M
XC2V1500	1.5M	48 x 40	7,680	17,280	15,360	240K	48	864K	48	24/420	8	DCM	DCM	YES	264	528	LVCMOS25, LVCMOS18,	-4 -5 -6	-4 -5			5.7M
XC2V2000	2M	56 x 48	10,752	24,192	21,504	336K	56	1008K	56	24/420	8	DCM	DCM	YES	312	624	LVCMOS15, PCI33, PCI66,	-4 -5 -6	-4 -5			7.5M
XC2V3000	3M	64 x 56	14,336	32,256	28,672	448K	96	1728K	96	24/420	12	DCM	DCM	YES	360	720	PCI-X, GTL, GTL+, HSTL I,	-4 -5 -6	-4 -5			10.5M
XC2V4000	4M	80 x 72	23,040	51,840	46,080	720K	120	2160K	120	24/420	12	DCM	DCM	YES	456	912	HSTL II, HSTL III, HSTL IV,	-4 -5 -6	-4 -5			15.7M
XC2V6000	6M	96 x 88	33,792	76,032	67,584	1056K	144	2592K	144	24/420	12	DCM	DCM	YES	552	1104	SSTL21, SSTL211,	-4 -5 -6	-4 -5			21.9M
XC2V8000	8M	112 x 104	46,592	104,832	93,184	1456K	168	3024K	168	24/420	12	DCM	DCM	YES	554	1108	SSTL3 I, SSTL3 II	-4 -5	-4			29.1M
Virtex-E Family — 1.8 Volt																						.18um Six Layer Metal Process
XCV50E	72K	16 x 24	768	1,728	1,536	24K	16	64K	NA	25/350	8	YES	YES	NA	88	176		-6 -7 -8	-6 -7	ISP	OTP	0.6M
XCV100E	128K	20 x 30	1,200	2,700	2,400	37.5K	20	80K	NA	25/350	8	YES	YES	NA	98	196		-6 -7 -8	-6 -7			0.9M
XCV200E	306K	28 x 42	2,352	5,292	4,704	73.5K	28	112K	NA	25/350	8	YES	YES	NA	142	284	LVTTL, LVCMOS2,	-6 -7 -8	-6 -7			1.45M
XCV300E	412K	32 x 48	3,072	6,912	6,144	96K	32	128K	NA	25/350	8	YES	YES	NA	158	316	LVCMOS18, PCI33,	-6 -7 -8	-6 -7			1.88M
XCV400E	570K	40 x 60	4,800	10,800	9,600	150K	40	160K	NA	25/350	8	YES	YES	NA	202	404	PCI66, GTL, GTL+,	-6 -7 -8	-6 -7			2.7M
XCV600E	986K	48 x 72	6,912	15,552	13,824	216K	72	288K	NA	25/350	8	YES	YES	NA	256	512	HSTL I, HSTL III, HSTL IV,	-6 -7 -8	-6 -7			3.97M
XCV1000E	1,569K	64 x 96	12,288	27,648	24,576	384K	96	384K	NA	25/350	8	YES	YES	NA	330	660	SSTL3 I, SSTL3 II,	-6 -7 -8	-6 -7			6.6M
XCV1600E	2,188K	72 x 180	25,920	34,992	51,840	486K	144	576K	NA	25/350	8	YES	YES	NA	362	724	SSTL21, SSTL211, BLVDS,	-6 -7 -8	-6 -7			8.4M
XCV2000E	2,542K	80 x 120	19,200	43,200	38,400	600K	160	640K	NA	25/350	8	YES	YES	NA	402	804	LVDS, LVPECL	-6 -7 -8	-6 -7			10.2M
XCV2600E	3,264K	92 x 138	25,392	57,132	50,784	793.5K	184	736K	NA	25/350	8	YES	YES	NA	402	804		-6 -7 -8	-6 -7			13M
XCV3200E	4,074K	104 x 156	32,448	73,008	64,896	1014K	208	832K	NA	25/350	8	YES	YES	NA	402	804		-6 -7 -8	-6 -7			16.3M
Virtex-EM Family — 1.8 Volt																						.18um Six Layer Metal Process
XCV405E	1.31M	40 x 60	4,800	10,800	9,600	150K	140	560K	NA	25/350	8	YES	YES	NA	202	404	Same As	-6 -7 -8	-6 -7	ISP	OTP	3.43M
XCV812E	2.54M	56 x 84	9,408	21,168	18,816	294K	280	1120K	NA	25/350	8	YES	YES	NA	278	556	Virtex-E	-6 -7 -8	-6 -7			6.52M
Spartan-IIE Family — 1.8 Volt																						.18um Six Layer Metal Process
XC2S50E	50K	16 x 24	768	1,728	1,536	24K	8	32K	NA	25/320	4	YES	YES	NA	84	182	LVTTL,LVCMOS2, LVCMOS18,	-6 -7	-6			0.6M
XC2S100E	100K	20 x 30	1,200	2,700	2,400	37.5K	10	40K	NA	25/320	4	YES	YES	NA	86	202	PCI33, PCI66, GTL, GTL+,	-6 -7	-6			0.9M
XC2S150E	150K	24 x 36	1,728	3,888	3,456	54K	12	48K	NA	25/320	4	YES	YES	NA	114	263	HSTL I, HSTL III, HSTL IV, SSTL3 I,	-6 -7	-6			1.1M
XC2S200E	200K	28 x 42	2,352	5,292	4,704	73.5K	14	56K	NA	25/320	4	YES	YES	NA	120	289	SSTL3 II, SSTL2 I, SSTL2 II, AGP-2X,	-6 -7	-6			1.4M
XC2S300E	300K	32 x 48	3,072	6,912	6,144	96K	16	64K	NA	25/320	4	YES	YES	NA	120	329	CTT, LVDS, BLVDS, LVPECL	-6 -7	-6			1.9M
Spartan-II Family — 2.5 Volt																						.22/.18um Six Layer Metal Process
XC2S15	15K	8 x 12	192	432	384	6K	4	16K	NA	25/200	4	YES	YES	NA	NA	86	LVTTL, LVCMOS2,	-5 -6	-5	ISP	OTP	0.2M
XC2S30	30K	12 x 18	432	972	864	13.5K	6	24K	NA	25/200	4	YES	YES	NA	NA	132	PCI33 (3.3V & 5V),	-5 -6	-5			0.4M
XC2S50	50K	16 x 24	768	1,728	1,536	24K	8	32K	NA	25/200	4	YES	YES	NA	NA	176	PCI66 (3.3V), GTL, GTL+,	-5 -6	-5			0.6M
XC2S100	100K	20 x 30	1,200	2,700	2,400	37.5K	10	40K	NA	25/200	4	YES	YES	NA	NA	196	HSTL I, HSTL III, HSTL IV,	-5 -6	-5			0.8M
XC2S150	150K	24 x 36	1,728	3,888	3,456	54K	12	48K	NA	25/200	4	YES	YES	NA	NA	260	SSTL3 I, SSTL3 II, SSTL2 I,	-5 -6	-5			1.1M
XC2S200	200K	28 x 42	2,352	5,292	4,704	73.5K	14	56K	NA	25/200	4	YES	YES	NA	NA	284	SSTL2 II, AGP-2X, CTT	-5 -6	-5			1.4M

Note: 1. System Gates include 20-30% of CLBs used as RAM
2. A Logic Cell is defined as a 4 input LUT and a register
DCM – Digital Clock Management

Important: Verify all Data with Device Data Sheet