XILINX IP REFERENCE GUIDE

Function	Vendor Name	IP Type	Virtex-II Pro	Virtex-II	Virtex-E	Virtex	Spartan-IIE	Spartan-II	Spartan	Implementation Example			Key Features	Application Examples
										Occ	MHz	Device		
Communication & Networking														
3G FEC Package	Xilinx	LogiCORE		V-II	V-E	V							Viterbi Decoder, Turbo Codec, Convolutional Encoder	3G Wireless Infrastructure
8b/10b Decoder	Xilinx	LogiCORE	V-IIP	V-II	V-E	V	S-IIE	S-II		0.4%	160	XC2V40-5	Industry std 8b/10b en/decode for serial data transmission	Physical layer of Fiber Channel
8b/10b Encoder	Xilinx	LogiCORE	V-IIP	V-II	V-E	V	S-IIE	S-II		0.4%	160	XC2V40-5	Industry std 8b/10b en/decode for serial data transmission	Physical layer of Fiber Channel
ADPCM, 16 channel	Amphion Semiconductor Ltd.	AllianceCORE		V-II		V				89%	16	XCV150-6	Supports G.721 G.723 G.726 G.726a G.727 G.727a, u-law, a-law	DECT, VOIP, cordless telephony
ADPCM, 32 channel	Xilinx	LogiCORE		V-II	V-E	V		S-II		62%	25	XC2V500	G.726, G.727, 32 duplex channels	DECT, VOIP, Wireless local loop, DSLAM, PBX
ADPCM, 64 channel	Xilinx	LogiCORE		V-II	V-E	V		S-II		61%	27	XC2V500	G.726, G.727, 64 duplex channels	DECT, VOIP, Wireless local loop, DSLAM, PBX
ADPCM, 256 channel	Amphion Semiconductor Ltd.	AllianceCORE		V-II	V-E					66%	30	XCV400E-8	Supports G.721 G.723 G.726 G.726a G.727 G.727a, u-law, a-law	DECT, VOIP, cordless telephony
ADPCM, 512 channel	Amphion Semiconductor Ltd.	AllianceCORE		V-II		V				49%	6	XCV400E-8		
ADPCM, 768 channel	Amphion Semiconductor Ltd.	AllianceCORE		V-II		V				89%	50	XC2V500-5	Supports G.721 G.723 G.726 G.726a G.727 G.727a, u-law, a-law	DECT, VOIP, cordless telephony
ADPCM, 1024 channel	Amphion Semiconductor Ltd.	AllianceCORE		V-II	V-E			S-II	S	89%	50	XC2V500-5	Supports G.721 G.723 G.726 G.726a G.727 G.727a, u-law, a-law	DECT, VOIP, cordless telephony
AES Decryption core family	Amphion Semiconductor Ltd.	AllianceCORE		V-II	V-E	V		S-II		36%	103	XC2V250-5		eCommerce, Banking, Video phones, PDA, satellite communications
AES Encryption Core	CAST, Inc.	AllianceCORE		V-II	V-E	V		S-II		16%	131	XC2V250-5	Supports ECB, OFB, CFB, CBC modes; Supports 128, 192 and 256-bit keys	Transaction and secure communications; surveillance, storage and embedded systems
AES Encryption core family	Amphion Semiconductor Ltd.	AllianceCORE		V-II	V-E	V		S-II		26%	134	XC2V250-5		eCommerce, Banking, Video phones, PDA, satellite communications
AWGN - Additive White Gaussian Noise	Xilinx	LogiCORE	V-IIP	V-II						93.0%	245	XC2V80-7	Probability density function (PDF) deviates less than 0.2 percent from the Gaussian PDF for $\|x\| < 4.8\sigma$ and is obtained from a closed-form expression	BER measurements for Forward Error Correction cores such as Reed-Solomon, Viterbi Decoder,Turbo Convolutional code or Turbo Product code
Bit Stream Analyzer and Data Extractor	Telecom Italia Lab S.p.A.	AllianceCORE				V		S-II	S	71%	67	XCV50-6	Data syntax analysis of IP, MPEG, ATM	ATM, IP, MPEG
Bluetooth Baseband Processor	NewLogic GmbH	AllianceCORE		V-II		V						XC2V1000-4	Compliant to Bluetooth v1.1, BQB qualified software for L2CAP, LHP, HC1, voice support	Bluetooth applications
Bluetooth Hardware Baseband Controller	Wipro, Ltd.	AllianceCORE		V-II		V				69%	25	XC2V1500-4		
Cell Assembler	Paxonet Communications	AllianceCORE				V			S		60	XC4005XL-1	Octet wide operation, HEC computation, cell scrambling	ATM adapter cards, routers, switches
Cell Delineation	Paxonet Communications	AllianceCORE				V			S		40	XC4010XL-9	Octet wide operation, HEC verification, cell scrambling	ATM adapter cards, rtouters, switches
Convolutional Encoder	Telecom Italia Lab S.p.A.	AllianceCORE				V		S-II	S	2%	144	XCV50-6	code rate, gen. vectors, CMSTR length customizable	Error correction
Convolutional Encoder	Xilinx	LogiCORE	V-IIP	V-II	V-E	V	S-IIE	S-II		10%	26	XC2V40-6	k from 3 to 9, puncturing from 2/3 to 12/13	3G base stations, broadcast, wireless LAN, cable modem, xDSL, satellite com, uwave
CRC10 Generator and Verifier	Paxonet Communications	AllianceCORE				V			S	22%	20	XCS30-4	Separate generator and verifier blocks, compatible with ITU-T I.363 for AAL3/AAL4	ATM, SONET, and Ethernet
CRC32 Generator and Verifier	Paxonet Communications	AllianceCORE				V			S	44%	29	XCS30-4	Separate generator and verifier blocks, compat with ITU-T I.363 for AAL5	ATM, SONET, and Ethernet
DES3 Encryption	CAST, Inc.	AllianceCORE		V-II	V-E	V		S-II		15%	167	XC2V1000-5		
DES and 3DES Cryptoprocessor	inSilicon Corporation	AllianceCORE				V		S-II	S		48	XC2S150-6	Compliant with ANSI X9.52, 128-bit key or two independent 64-bit keys	Secure communication, data storage
DES and 3DES encryption engine	Memec Core	AllianceCORE							S	79%	25	XCS20-4	NIST certified, supports EBC, CBC, CFB, and OFB	Secure communication, data storage
DES Cryptoprocessor	inSilicon Corporation	AllianceCORE				V		S-II	S		94	XC2S100-6	NIST certified, supports ECB, CBC, CFB, and OFB	Secure communication, data storage
DES Encryption	CAST, Inc.	AllianceCORE		V-II	V-E	V		S-II		93%	204	XC2V40-5		
Distributed Sample Descrambler	Telecom Italia Lab S.p.A.	AllianceCORE				V		S-II	S	14%	74	XCV50-6	Compliant with ITU-T I.432. Parameterizable data width, cell & header length	ATM PHY layer
Distributed Sample Scrambler	Telecom Italia Lab S.p.A.	AllianceCORE				V		S-II	S	9%	104	XCV50-6	Compliant with ITU-T I.432 scrambler. Parameterizable data width, cell length, header length	ATM PHY layer
DVB Satellite Modulator	Memec Core	AllianceCORE				V					45-70	XCV50-4	Conforms to ETSI EN 300 421 v1.1.2, selectable convolutional code rate	Digital broadcast, microwave transmitter
Ethernet MAC, 1 Gigabit Full Duplex	Alcatel Technology Licensing Group	AllianceCORE		V-II						46%	31	XC2V1500-5	Single/multi-mode fiber optics; 802.3x full duplex flow control; 10-bit SERDES for GMII; Auto-negotiation for 1000BASE-X	NICs, routers, switches, hubs
Gb Ethernet MAC/ 1000BaseX MAC+PHY Half/Full duplex	Xilinx	LogiCORE	V-IIP	V-II	V-E		S-IIE			23%	125 (XGMII) or 1.25 Gbps	XC2V1000-4	IEEE 802.3-2000 compliant, supports 8-bit GMII interface or integrated PCS/PMA interface, supporting 1000BASE-X applications	GbE Network Interface Cards (NICs), Edge switches and terabit routers – packet based line cards, iSCSI line cards, PL3 to Gb Ethernet and other bridges
10 Gb Ethernet MAC, 10000BaseX MAC+PHY Full Duplex	Xilinx	LogiCORE	V-IIP	V-II						25%	156.25 DDR for XGMII or 4 channels of 3.125 Gbps rocket io transceivers	XC2V3000-5	Designed to IEEE 802.3ae, version D4.1 supports both 32-bit XGMII parallel interface or XAUI interface, supports 10 GBASE-X, WAN/LAN functionality, Statistics gathering	Layer 2 swtiches/hubs, test equipment, bridge to POS PHY4, iSCSI line cards
Ethernet MAC, 10/100	Alcatel Technology Licensing Group	AllianceCORE		V-II				S-II		13%	31	XC2V1500-5	Single/multi-mode fiber optics; 10/100 MII PHY, 10Base-T, 100Base-T/TX/FX/4; RMON & Etherstats	NICs, routers, switches, hubs, printers
Ethernet MAC, 10/100	Paxonet Communications	AllianceCORE				V		S-II	S	45%	50	XCV150-4	IEEE 802.3 compliant RMON, MIBs stats, MII support	Ethernet switched, hub, NICS
SPI-4.1 (Flexbus 4) Interface Core, 1-Channel	Xilinx	LogiCORE		V-II						12%	200	XC2V1000 FG456-5	OIF SPI-4 Phase 1 and Flexbus4 compliant. Fully HW interoperable with AMCC OC-192 framers.	Line card: terabit routers & optical switches
SPI-4.1 (Flexbus 4) Interface Core, 4-Channel	Xilinx	LogiCORE		V-II						27%	200	XC2V1000 FG456-5	OIF SPI-4 Phase 1 and Flexbus4 compliant. Fully HW interoperable with AMCC OC-192 framers.	Line card: terabit routers & optical switches
HDLC Controller Core, 1-Channel	Xilinx	LogiCORE		V-II	V-E	V		S-II		15%	115	XC2V250	16/32-bit frame seq, 8/16-bit addr insert/delete, flag/zerop insert/detect	X.25, POS, cable modems, frame relay switches, video conferencing over ISDN
HDLC Controller, 1-Channel	Memec Core	AllianceCORE				V		S-II		95%	77	XC2S15-5	16/32-bit frame seq, 8/16-bit addr insert/delete, flag/zerop insert/detection	X.25, Frame Relay, B/D-Channel
HDLC Controller Core, 32-Channel	Xilinx	LogiCORE		V-II	V-E	V		S-II		34%	81	XC2V250	32 full duplex, CRC-16/32, 8/16-bit address insertion/deletion	X.25, POS, cable modems, frame relay switches, video conferencing over ISDN
HDLC-PPP for Packet over SONET	Paxonet Communications	AllianceCORE				V		S-II		75%	80	XC2S150-6	RFC1619 (IP&IPX) POS, 16/32 bit FCS generation and verification, stats	Bridges, switches, WAN links
Interleaver/De-interleaver	Xilinx	LogiCORE	V-IIP	V-II	V-E	V	S-IIE	S-II		30%	208	XC2V40-6	Block & convolutional, width up to 256 bits, 256 branches	Broadcast, wireless LAN, cable modem, xDSL, satellite com,uwave nets, digital TV, CDMA2000
Interleaver/Deinterleaver	Telecom Italia Lab S.p.A.	AllianceCORE				V		S-II	S	21%	73	XCV50-6	Block & convolutional support. param features. 3GPP, UMTS, GSM, DVB compliant	Channel coding in telecom/wireless, broadcast
Inverse Multiplexer for ATM	ModelWare, Inc.	AllianceCORE		V-II	V-E					100%	31	XC2V1000-4	Supports up to 32 links/32 groups; UTOPIA L2 PHY & ATM I/Fs, supports IDCR	Access systems, multi-service switches, DSLAMs, Basestation controllers
Network Processor	IP Semiconductors A/S	AllianceCORE		V-II	V-E						80	XC2V1500-5	Total Solution requires this core + SPEEDAnalyzer ASIC, 2.5 Gbps full duplex wire speed; network processor (NPV), low power an low device count than competing network processors.	Networking, edge and access, Switches and routers
Noisy Transmission Channel Model	Telecom Italia Lab S.p.A.	AllianceCORE				V		S-II	S	23%	100	XCV50-6	Programmable noise generation profile	Noise emulation in transmission channel
PCM Codec, G.711	Xilinx	LogiCORE			V-E	V		S-II		12%	44	XCV50	µ-Law, ITU G.711, EBI for A-Law	Digital telephony, DECT, T1 & E1 Links
PCM Compressor, G.711	Xilinx	LogiCORE			V-E	V		S-II		7%	44	XCV50	µ-Law, ITU G.711, EBI for A-Law	Digital telephony, DECT, T1 & E1 Links
PCM Expander, G.711	Xilinx	LogiCORE			V-E	V		S-II		6%	57	XCV50	Digital telephony, DECT, T1 & E1	Digital telephony, DECT, T1 & E1 Links
SPI-3 (PL3) POS-PHY L3 Link Layer Interface, 1-Ch	Xilinx	LogiCORE	V-IIP	V-II	V-E	V	S-IIE	S-II		10%	200	XC2V1000 FG456-4	OIF SPI-3 compliant. Fully HW interoperable with PMC-Sierra OC-48 framers.	Line cards, iSCSI cards, gigabit routers and switches
SPI-3 (PL3) POS-PHY L3 Link Layer Interface, 2-Ch	Xilinx	LogiCORE	V-IIP	V-II	V-E	V	S-IIE	S-II		55%	200	XCV50E-8	OIF SPI-3 compliant. Fully HW interoperable with PMC-Sierra OC-48 framers.	Line cards, iSCSI cards, gigabit routers and switches
SPI-3 (PL3) POS-PHY L3 Link Layer Interface, 4-Ch	Xilinx	LogiCORE	V-IIP	V-II	V-E	V	S-IIE	S-II		15%	200	XC2V1000 FG456-4	OIF SPI-3 compliant. Fully HW interoperable with PMC-Sierra OC-48 framers.	Line cards, iSCSI cards, gigabit routers and switches
SPI-3 (PL3) Link Layer Interface 1-256 Ch	Xilinx	LogiCORE	V-IIP	V-II	V-E	V	S-IIE	S-II		9%	175	XC2V1000 FG456-4	OIF SPI-3 compliant. Fully HW interoperable with PMC-Sierra OC-48 framers.	Line cards, iSCSI cards, gigabit routers and switches
SPI-3 (PL3) POS-PHY L3 Physical Layer Interface	Xilinx	LogiCORE			V-E					52%	104	XCV50E-8	OIF SPI-3 compliant.	Line cards, iSCSI cards, gigabit routers and switches8b/10b

Function	Vendor Name	IP Type	Virtex-II Pro	Virtex-II	Virtex-E	Virtex	Spartan-IIE	Spartan-II	Spartan	Implementation Example			Key Features	Application Examples
										Occ	MHz	Device		
Communication & Networking (continued)														
SPI-4.2 (PL4) Multi-Channel Interface	Xilinx	LogiCORE	V-IIP	V-II						25% w/ static alignment; 29% w/ dynamic alignment	400 DDR w/ static alignment; 350 DDR w/ dynamic alignment	XC2V3000 FG676-5	OIF SPI-4 Phase 2 compliant. Fully HW interoperable with PMC-Sierra and Mindspeed OC-192 framers.	Line cards, switches, routers and optical switches
SPI-4.2 (PL4) to SPI-4.1 (Flexbus4) Bridge	Xilinx	LogiCORE		V-II						35%	200 on FB4, 350 DDR on PL4, 175 internal	XC2V3000 FG676-5	OIF SPI-4 Phase 1& 2 compliant. Fully HW interoperable with AMCC, PMC-Sierra and Mindspeed OC-192 framers.	
XGMII(10GE MAC) to SPI-4.2 Bridge	Xilinx	LogiCORE		V-II						53%	350 DDR on SPI-4.2	2V3000 156 DDR on XGMII	OIF SPI-4.2 compliant. Designed to IEEE 80z.3ae	Line cards, switches, routers, etc.
Reed-Solomon Encoder	Xilinx	LogiCORE	V-IIP	V-II	V-E	V	S-IIE	S-II	S	40%	98	XC2V250-6	Std or cust coding, 3-12 bit width, up to 4095 symbols with 256 check symb.	Broadcast, wireless LAN, cable modem, xDSL, satellite com,uwave nets, digital TV
Reed Solomon Encoder	Telecom Italia Lab S.p.A.	AllianceCORE		V-II		V				97%	61	XC2V500-5	parameterizable, RTL available	Error correction
Reed Solomon Encoder	Amphion Semiconductor Ltd.	AllianceCORE				V			S	50%	50	XCV100-4		Error Correction
Reed Solomon Decoder	Memec Core	AllianceCORE				V		S-II	S	83%	73	XCV50-6	Customizable, >580 Mbps	Error correction
Reed-Solomon Encoder	Xilinx	LogiCORE	V-IIP	V-II	V-E	V	S-IIE	S-II	S	42%	180	XC2V40-6	Std or cust coding, 3-12 bit width, up to 4095 symbols with 256 check symb.	Broadcast, wireless LAN, cable modem, xDSL, satellite com,uwave nets, digital TV
Reed Solomon Encoder	Amphion Semiconductor Ltd.	AllianceCORE				V			S	11%	82	XCV50-4		Error correction
Reed Solomon Encoder	Memec Core	AllianceCORE				V		S-II	S	12%	113	XCV50-6	Customizable, > 900 Mbps	Error Correction
SDLC Controller	CAST, Inc.	AllianceCORE		V-II		V				11%	158 MHz	XC2V1000-5	Like Intel 8XC152 Global Serial Channel, Serial Comm., HDLC apps, telecom	Embedded systems, professional audio, video
SHA-1 Encryption processor	CAST, Inc.	AllianceCORE		V-II	V-E	V	S-IIE	S-II		24%	79	XC2V500-6	SHA-1 algorithm compliant	Secure comms, video suveillance, data storage, financial transactions
T1 Deframer	Xilinx	LogiCORE			V-E	V		S-II		15%	54	XC2S150		ISDN PRA links, mux equip, satellite com, digital PABX, high-speed computer links
T1 Framer	Virtual IP Group	AllianceCORE											D4, ESF, SLC-96 formats. For XC4000.	DSI trunk, PBX I/F
T1/E1 Framer	Xilinx	LogiCORE			V-E	V		S-II		7%	72	XC2S150		ISDN PRA links, mux equip, satellite com, digital PABX, high-speed computer links
Turbo Convolutional Decoder - 3GPP Compliant	Xilinx	LogiCORE		V-II	V-E	V				80%	40	XC2V500	3GPP specs, 2 Mbps, BER=10-6 for 1.5dB SNR	3G Wireless Infrastructure
Turbo Decoder, 3GPP	SysOnChip, Inc.	AllianceCORE		V-II		V					66	XC2V500-5	3GPP/UMTS compliant, IMT-2000, 2Mbps data rate	Error correction, wireless
Turbo Decoder, DVB-RCS	iCoding Technology, Inc.	AllianceCORE		V-II	V-E	V				44%	71	XC2V2000-5	DVB-RCS compliant, 9Mbps, data rate, switchable code rates and frame sizes	Error correction, wireless, DVB, Satellite data link
Turbo Decoder	Telecom Italia Lab S.p.A.	AllianceCORE		V-II		V				70%	65	XC2V2000-5	3GPP/UMTS compliant, >2Mbps data rate	Error correction, wireless
Turbo Convolutional Encoder - 3GPP Compliant	Xilinx	LogiCORE		V-II	V-E	V				65%	60	XC2V250	Compliant w/ 3GPP, puncturing	3G Wireless Infrastructure
Turbo Encoder, DVB-RCS	iCoding Technology, Inc.	AllianceCORE		V-II	V-E	V				2%	69	XC2V2000-5	DVB-RCS compliant, 9Mbps, data rate, switchable code rates and frame sizes	Error correction, wireless, DVB, Satellite data link
Turbo Encoder	Telecom Italia Lab S.p.A.	AllianceCORE		V-II		V		S-II		48%	120	XC2V80-5	3GPP/UMTS compliant, upto 4 interleaver laws	Error correction, wireless
Turbo Product Code Decoder	Xilinx	LogiCORE	V-IIP	V-II						31%	285	XC2V40-7	Fully compliant with IEEE 802.16 and 802.16a standards	Error Correction, LMDS, MMDS
Turbo Product Code Encoder	Xilinx	LogiCORE	V-IIP	V-II						64%	150	XC2V1000-7	Fully compliant with IEEE 802.16 and 802.16a standards	Error Correction, LMDS, MMDS
UTOPIA level 2 slave inteface	Paxonet Communications	AllianceCORE											Cell handshake in SPHY mode, 8/16 bit operation, internal FIFO, detects runt cells	ATM PHY layer
UTOPIA Level-2 PHY Side RX Interface	Telecom Italia Lab S.p.A.	AllianceCORE				V		S-II	S	8%	53	XCV50-6	Protocol conversion from Pb (RACE BLNT) to UTOPIA L2, 8/16 bit operation	ATM PHY layer
UTOPIA Level-2 PHY Side TX Interface	Telecom Italia Lab S.p.A.	AllianceCORE				V		S-II	S	10%	61	XCV50-6	Protocol conversion from UTOPIA L2 Pb (RACE BLNT), 8/16 bit operation	ATM PHY layer
UTOPIA Level-3 ATM Receiver	inSilicon Corporation	AllianceCORE				V		S-II	S					
UTOPIA Level-3 ATM Transmitter	inSilicon Corporation	AllianceCORE				V		S-II	S					
UTOPIA Level-3 PHY Receiver	inSilicon Corporation	AllianceCORE				V		S-II	S					
UTOPIA Level-3 PHY Transmitter	inSilicon Corporation	AllianceCORE				V		S-II	S					
UTOPIA Master	Paxonet Communications	AllianceCORE				V		S-II	S				SPHY, MPHY, HEC processing, round robin polling, ind. transmitter receiver	ATM PHY layer
UTOPIA Slave	Paxonet Communications	AllianceCORE				V		S-II	S	26%	79	XCV50-4	Cell handshake in SPHY mode, 8/16 bit operation, 32 bit FIFO interface, detects runt cells	ATM PHY layer
Viterbi Decoder, IEEE 802-compatible	Xilinx	LogiCORE	V-IIP	V-II	V-E	V	S-IIE	S-II		35%	157	XC2V500-5	Parameterizable source code with constraint length(k)=7, G0=171, G1=133; or G0=133, G1=171, includes BestState Logic, ability to change code rate and traceback depth on the fly, supports Trellis Coded Modulation, IEEE802.11a/16a compatible, reaches OC3 (155Mbps) and higher	3G base stations, broadcast, wireless LAN, cable modem, xDSL, satellite com, uwave, CDMA2000
Viterbi Decoder, General Purpose	Xilinx	LogiCORE	V-IIP	V-II	V-E	V	S-IIE	S-II		38%	128	XC2V500-5	Puncturing, serial & parallel architecture, dynamic rate change, paramterized constraint length, soft/hard decision with programmable number of soft bits, dual rate decoder, erasure pins for external puncturing, compatible with standards such as DVB ETS, 3GPP2, IEEE802.16, Hiperlan, Intelsat IESS-308/309	3G base stations, broadcast, wireless LAN, cable modem, xDSL, satellite com, uwave, CDMA2000
Viterbi Decoder	Telecom Italia Lab S.p.A.	AllianceCORE		V-II	V-E			S-II		74%	91	XC2V500-5	Radix-2/radix4 architectures, BER, depuncturing. Code rate, contraint length parameterizable	Data transmission, wireless
Digital Signal Processing														
Bit Correlator	Xilinx	LogiCORE	V-IIP	V-II	V-E	V	S-IIE	S-II					4096 taps, serial/parallel input, 4096 bits width	
Cascaded Integrator Comb (CIC) Filter	Xilinx	LogiCORE	V-IIP	V-II	V-E	V	S-IIE	S-II					32 bits data width, rate change from 8 to 16384	
Comb Filter	Xilinx	LogiCORE							S				Not recommended for new designs. Suggested replacement: Cascaded Integrator Comb Filter	
CORDIC	Xilinx	LogiCORE	V-IIP	V-II	V-E	V	S-IIE	S-II					Polar to rectangular, rectangular to polar, sin & cos, sinh & cosh, atan & atanh, square root	Digital receivers
Digital Down Converter (DDC)	Xilinx	LogiCORE	V-IIP	V-II	V-E	V	S-IIE	S-II		47%	116	XC2V500-5	Configurable datapath comprising mixer, DDS, optional CIC filter, optional polyphase decimators, 25 to 108db DDS spurious free dynamic range	Wireless & wireline communication systems such as software defined radios, digital receivers, cable modems, BPSK, QPSK, QAM demodulators, spread spectrum communication systems, CDMA2000 & 3G basestations
Direct Digital Synthesizer (DDS)	Xilinx	LogiCORE	V-IIP	V-II	V-E	V	S-IIE	S-II		12%	245	XC2V80-6	8-65K samples, 32-bits output precision, phase dithering/offset	
FFT/IFFT, 1024-Point Complex	Xilinx	LogiCORE			V-E	V								
FFT/IFFT for Virtex-II, 1024-Point Complex	Xilinx	LogiCORE		V-II						62%	41us, 100MHz	XC2V500	16 bit complex data, 2's comp, forward and inverse transform	
FFT/IFFT, 16-Point Complex	Xilinx	LogiCORE		V-II	V-E									
FFT/IFFT for Virtex-II, 16-Point Complex	Xilinx	LogiCORE		V-II						37%	123ns 130MHz	XC2V500	16 bit complex data, 2's comp, forward and inverse transform	
FFT/IFFT, 256-Point Complex	Xilinx	LogiCORE		V-II	V-E	V								
FFT/IFFT for Virtex-II, 256-Point Complex	Xilinx	LogiCORE		V-II						54%	7.7us, 100MHz	XC2V500	16 bit complex data, 2's comp, forward and inverse transform	
FFT/IFFT, 32-Point Complex	Xilinx	LogiCORE	V-IIP	V-II	V-E	V	S-IIE	S-II		29%	110	XC2V500-6	Complex FFT, Forward and Inverse transform. Supports bit precisions from 2-32 bits. Embedded memory	
FFT/IFFT, 64-, 256-, 1024-Point Complex	Xilinx	LogiCORE	V-IIP	V-II						32%	140	XC2V1500-6	64-,256-,1024-point programmable point size, forward and inverse transform, 16-bit complex data, 18-bit phase factors, 2's complement, built-in memories, programmable data scaling, 140 MHz, 1024-point transform - 7.31 us, 256-point transform - 1.83 us, 64-point transform - 0.46 us	
FFT/IFFT, 64-Point Complex	Xilinx	LogiCORE			V-E	V								
FFT/IFFT for Virtex-II, 64-Point Complex	Xilinx	LogiCORE		V-II						38%	1.9us, 100MHz	XC2V500	16 bit complex data, 2's comp, forward and inverse transform	
FIR Filter, Distributed Arithmetic (DA)	Xilinx	LogiCORE	V-IIP	V-II	V-E	V	S-IIE	S-II					32-bit input/coeff width, 1024 taps, 1-8 chan, polyphase, online coeff reload	
FIR Filter, Distributed Arithmetic Parallel	Xilinx	LogiCORE							S				Not recommended for new designs. Suggested replacement: Distributed Arithmetic FIR Filter	
FIR Filter, Distributed Arithmetic Serial	Xilinx	LogiCORE							S				Not recommended for new designs. Suggested replacement: Distributed Arithmetic FIR Filter	
FIR Filter, MAC	Xilinx	LogiCORE	V-IIP	V-II	V-E	V	S-IIE	S-II		16%		XC2V250	Single rate, Polyphase Decimator, Polyphase Interpolator	3G base stations, wireless communications, image filtering

Function	Vendor Name	IP Type	Virtex-II Pro	Virtex-II	Virtex-E	Virtex	Spartan-IIE	Spartan-II	Spartan	Implementation Example Occ	Implementation Example MHz	Implementation Example Device	Key Features	Application Examples
Digital Signal Processing (continued)														
LFSR, Linear Feedback Shift Register	Xilinx	LogiCORE	V-IIP	V-II	V-E	V	S-IIE	S-II					168 input widths, SRL16/register implementation	
Oscillator, Dual-Channel Numerically Controlled	Xilinx	LogiCORE			V-E	V	S-IIE	S-II	S				Not recommended for new designs. Suggested replacement: Direct Digital Synthesizer	
Oscillator, Numerically Controlled	Xilinx	LogiCORE			V-E	V	S-IIE	S-II	S				Not recommended for new designs. Suggested replacement: Direct Digital Synthesizer	
Time-Skew Buffer, Nonsymmetric 16-Deep	Xilinx	LogiCORE							S				Not recommended for new designs.	
Time-Skew Buffer, Nonsymmetric 32-Deep	Xilinx	LogiCORE							S				Not recommended for new designs.	
Time-Skew Buffer, Symmetric 16-Deep	Xilinx	LogiCORE							S					
TMS32025 DSP Processor core	CAST, Inc.	AllianceCORE		V-II	V-E	V		S-II		66%	63	XC2V500-5		
Math Functions														
1s and 2s Complement	Xilinx	LogiCORE							S				Not recommended for new designs. Suggested replacement: Bus Gate or Twos Complementer	
Accumulator	Xilinx	LogiCORE	V-IIP	V-II	V-E	V	S-IIE	S-II					1-256s bit wide	
Adder Subtracter	Xilinx	LogiCORE	V-IIP	V-II	V-E	V	S-IIE	S-II					1-256s bit wide	
Divider, Pipelined	Xilinx	LogiCORE		V-II	V-E	V	S-IIE	S-II	S				32-bit input data width, multiple clock per output	
Floating Point Adder	Digital Core Design	AllianceCORE		V-II		V		S-II			66	XC2V250-5	Full IEEE-754 compliance, 4 pipelines, Single precision real format support	DSP, Math, Arithmetic apps
Floating Point Divider	Digital Core Design	AllianceCORE		V-II		V		S-II			53	XC2V250-5	Full IEEE-754 compliance, 15 pipelines, Single precision real format support	DSP, Math, Arithmetic apps
Floating Point Multiplier	Digital Core Design	AllianceCORE		V-II	V-E	V		S-II			74	XC2V250-5	Full IEEE-754 compliance, 7 pipelines,32x32 mult, Single precision real format support	DSP, Math, Arithmetic apps.
Floating Point Square Comparator	Digital Core Design	AllianceCORE		V-II		V		S-II			91	XC2V80-5	Full IEEE-754 compliance, 4 pipelines, Single precision real format support	DSP, Math, Arithmetic apps.
Floating Point Square Root Operator	Digital Core Design	AllianceCORE		V-II	V-E			S-II			66	XC2V250-5	Full IEEE-754 compliance, 4 pipelines, Single precision real format support	DSP, Math, Arithmetic apps
Floating Point to Integer Converter	Digital Core Design	AllianceCORE		V-II		V		S-II			66	XC2V250-5	Full IEEE-754 compliance, 4 pipelines, Single precision real format support	DSP, Math, Arithmetic apps
Integer to Floating Point Converter	Digital Core Design	AllianceCORE		V-II		V		S-II			73	XC2V250-5	Full IEEE-754 compliance, double word input, 2 pipelines, Single precision real output	DSP, Math, Arithmetic apps
Integrator	Xilinx	LogiCORE							S				Not recommended for new designs. Suggested replacement: Cascaded Integrator Comb Filter	
Multiplier, Constant Coefficient	Xilinx	LogiCORE							S				Not recommended for new designs. Suggested replacement: Multiplier	
Multiplier, Constant Coefficient - Pipelined	Xilinx	LogiCORE							S				Not recommended for new designs. Suggested replacement: Multiplier	
Multiplier, Dynamic Constant Coefficient	Xilinx	LogiCORE			V-E	V							Not recommended for new designs. Suggested replacement: Multiplier	
Multiplier, Parallel - Area Optimized	Xilinx	LogiCORE							S				Not recommended for new designs. Suggested replacement: Multiplier	
Multiplier for Virtex, Variable Parallel	Xilinx	LogiCORE			V-E	V	S-IIE	S-II					Not recommended for new designs. Suggested replacement: Multiplier	
Multiply Accumulator (MAC)	Xilinx	LogiCORE	V-IIP	V-II		V	S-IIE	S-II					Input width up to 32 bits, 65-bit accumulator, truncation rounding	
Multiply Generator	Xilinx	LogiCORE	V-IIP	V-II	V-E	V	S-IIE	S-II					64-bit input data width, constant, reloadable or variable inputs, parallel/sequential implementation	
Registered Adder	Xilinx	LogiCORE							S				Not recommended for new designs. Suggested replacement: Adder Subtracter	
Registered Loadable Adder	Xilinx	LogiCORE							S				Not recommended for new designs. Suggested replacement: Adder Subtracter	
Registered Loadable Subtracter	Xilinx	LogiCORE							S				Not recommended for new designs. Suggested replacement: Adder Subtracter	
Registered Scaled Adder	Xilinx	LogiCORE							S				Not recommended for new designs.	
Registered Serial Adder	Xilinx	LogiCORE							S				Not recommended for new designs.	
Registered Subtracter	Xilinx	LogiCORE							S				Not recommended for new designs. Suggested replacement: Adder Subtracter	
Scaled-by-One-Half Accumulator	Xilinx	LogiCORE							S				Not recommended for new designs. Suggested replacement: Accumulator	
Sine Cosine Look Up Table	Xilinx	LogiCORE	V-IIP	V-II	V-E	V	S-IIE	S-II	S	12%	270	XC2V40-6	3-10 bit in, 4-32 bit out, distributed/block ROM	
Square Root	Xilinx	LogiCORE							S				Not recommended for new designs. Suggested replacement: CORDIC	
Twos Complementer	Xilinx	LogiCORE	V-IIP	V-II	V-E	V	S-IIE	S-II					Input width up to 256 bits	
Memories & Storage Elements														
ATM Utopia Level 2	Xilinx	LogiCORE	V-IIP											
Block Memory, Dual-Port	Xilinx	LogiCORE	V-IIP	V-II	V-E	V	S-IIE	S-II					1-256 bits, 2-13K words	
Block Memory, Single-Port	Xilinx	LogiCORE	V-IIP	V-II	V-E	V	S-IIE	S-II					1-256 bits, 2-128K words	
Content Addressable Memory (CAM)	Xilinx	LogiCORE	V-IIP	V-II	V-E	V	S-IIE	S-II					1-512 bits, 2-10K words, SRL16	
CAM, for Internet Protocol	Telecom Italia Lab S.p.A.	AllianceCORE				V		S-II	S	19%	49	XCV50-6		IP routers
Distributed Memory	Xilinx	LogiCORE	V-IIP	V-II	V-E	V	S-IIE	S-II					1-1024 bit, 16-65536 word, RAM/ROM/SRL16, opt output regs and pipelining	
FIFO, Asynchronous	Xilinx	LogiCORE	V-IIP	V-II	V-E	V	S-IIE	S-II					1-256 bits, 15-65535 words, DRAM or BRAM, independent I/O clock domains	
FIFO, Synchronous	Xilinx	LogiCORE							S				Not recommended for new designs. Suggested replacement: Synchronous FIFO supporting Spartan-II/Spartan-IIE	
FIFO, Synchronous	Xilinx	LogiCORE	V-IIP	V-II	V-E	V	S-IIE	S-II					1-256 bits, 16-256 words, distributed/block RAM	
Pipelined Delay Element	Xilinx	LogiCORE							S				Not recommended for new designs. Suggested replacement: Distributed Memory using SRL16 based memory type	
Registered ROM	Xilinx	LogiCORE							S				Not recommended for new designs. Suggested replacement: Distributed Memory	
Registered Single Port RAM	Xilinx	LogiCORE							S				Not recommended for new designs. Suggested replacement: Distributed Memory	
Microprocessors, Controllers & Peripherals														
10/100 Ethernet MAC w/OPB interface	Xilinx	LogiCORE	V-IIP	V-II	V-E	V	S-IIE	S-II			125	XC2V80-5	CoreConnect Bus (OPB), Ethernet Core ($)	Processor applications
10/100 Ethernet MAC Lite w/OPB interface	Xilinx	LogiCORE	V-IIP	V-II	V-E	V	S-IIE	S-II			125	XC2V80-5	CoreConnect Bus (OPB), Ethernet Core ($)	Processor applications
16-bit proprietary RISC processor	Loarant Corporation	AllianceCORE		V-II	V-E	V		S-II			91 MHz	XC2V500-5	44 opcodes, 64-K word data, program, Harvard arch.	Control functions, State machines, Coprocessor
16-Word-Deep Registered LUT	Xilinx	LogiCORE							S					
16450 UART	Virtual IP Group	AllianceCORE							S		60	XC2S50-6	Independently controlled transmit, receive and data interrupts. 16X clock.	Serial data applications, modems
16450 UART w/OPB interface	Xilinx	LogiCORE	V-IIP	V-II	V-E	V	S-IIE	S-II			125	XC2V80-5	CoreConnect Bus (OPB), UART Core ($)	Processor applications
16450 UART w/PLB interface	Xilinx	LogiCORE	V-IIP								150	Virtex-II Pro (-6)	CoreConnect Bus (PLB), UART Core ($)	PowerPC embedded system design
16550 UART w/FIFOs	Virtual IP Group	AllianceCORE							S		16	XCS20-4	Prog. Data width, parity, stop bits. 16X internal clock, FIFO mode, false start bit detection	Serial data applications, modems
16550 UART w/FIFOs & synch interface	CAST, Inc.	AllianceCORE		V-II	V-E	V	S-IIE	S-II		57%	87	XC2V80-5	Supports 16450 and 16550a synchronous s/w; programmable serial interface	Serial and modem applications
16550 UART w/OPB interface	Xilinx	LogiCORE	V-IIP	V-II	V-E	V	S-IIE	S-II			125	XC2V80-5	CoreConnect Bus (OPB), UART Core ($)	Processor applications
16550 UART w/PLB interface	Xilinx	LogiCORE	V-IIP								150	Virtex-II Pro (-6)	CoreConnect Bus (PLB), UART Core ($)	PowerPC embedded system design
2901 microprocessor slice	CAST, Inc.	AllianceCORE				V		S-II		19%	36	XC2S50-6	Eight function ALU, 4 status flags- Carry, Overflow, Zero and Negative	Simple microcontroller applications
2910A microprogram controller	CAST, Inc.	AllianceCORE				V		S-II	S	12%	63	XCV50-6	Based on AMD 2910a	High-speed bit slice design
68000 compatible microprocessor	CAST, Inc.	AllianceCORE		V-II		V				89%	32	XC2V500-5	MC68000 Compatible	Embedded systems, professional audio, video
80186 compatible processor	eInfochips Pvt. Ltd.	AllianceCORE		V-II		V				77%	49	XC2V1000-5	i80186 compatible plus enhanced mode	Industrial, wireless, communications, embedded
8051 compatible microcontroller	CAST, Inc.	AllianceCORE				V		S-II		52%	68	XCV200E-8	80C31 instruction set, 8 bit ALU, 8 bit control, 32 bit I/O ports, two 16 bit timer/counters, SFR I/F	Embedded systems, telecom
8051 compatible microcontroller	Digital Core Design	AllianceCORE		V-II		V		S-II			73	XC2V250-5	80C31 instruction set, RISC architecture 6.7X faster than standard 8051	Embedded systems, telecom, video

Function	Vendor Name	IP Type	Virtex-II Pro	Virtex-II	Virtex-E	Virtex	Spartan-IIE	Spartan-II	Spartan	Implementation Example Occ	Implementation Example MHz	Implementation Example Device	Key Features	Application Examples
Microprocessors, Controllers & Peripherals (continued)														
8051 compatible microcontroller	Digital Core Design	AllianceCORE		V-II		V		S-II			90	XC2V250-5	80C31 instruction set, high speed multiplier, RISC architecture 6.7X faster than standard 8051	Embedded systems, telecom, video
8051 compatible microcontroller	Dolphin Integration	AllianceCORE				V		S-II	S	33%	29.8	XCV300-6	12X faster (average) and code compatible wrt legacy 8051, verification bus monitor, SFR interface	Telecom, industrial, high speed control
8051 compatible microcontroller	Dolphin Integration	AllianceCORE		V-II	V-E			S-II		39%	38	XC2V1000-5	8X faster (average) and code compatible wrt legacy 8051, verification bus monitor, SFR interface, DSP focused	DSP, Telecom, industrial, high speed control
80515 high-speed 8-bit RISC microcontroller	CAST, Inc.	AllianceCORE				V				90%	42	XCV200E-8	RISC implementation, 8 bit ALU, 8 bit control, 32 bit I/O, 16 bit timer/counters, SFR I/F, ext. memory I/F	High speed embedded systems, audio, video
8052 compatible microcontroller	Digital Core Design	AllianceCORE		V-II		V		S-II			71	XC2V250-5	80C31 instruction set, high speed multiplication and division ,RISC architecture 6.7X faster than standard 8051	Embedded systems, telecom, video
80530 8-bit microcontroller, compact	CAST, Inc.	AllianceCORE				V		S-II		88%	51	XC2S150-6	32 bit I/O, 3 counters, interrupt controller, SFR interface, dual data pointer	Low cost embedded systems, telecom
80530 8-bit microcontroller	CAST, Inc.	AllianceCORE				V				81%	66	XCV200E-8	32 bit I/O, 3 counters, 27-bit watchdog timer, 3-priority interrupt controller, SFR interface	Embedded systems, telecom
80C51 compatible RISC microcontroller	CAST, Inc.	AllianceCORE			V-E	V		S-II		75%	34	XC2S150-6	12X faster, SRF I/F	Embedded systems
8237 programmable DMA controller	CAST, Inc.	AllianceCORE		V-II	V-E	V		S-II		40%	34	XC2S100-6	4 independent DMA channels (expandable), software DM	Microprocessor based systems
8250 UART	Memec Core	AllianceCORE							S	58%	10	XCS10-4	DC to 625K baud	Serial communications
8254 programmable interval timer/counter core	CAST, Inc.	AllianceCORE		V-II	V-E	V		S-II		74%	68	XC2V80-5	Status feedback, counter latch, Square wave mode, 6 counter modes, binary/BCD count, LSB/MSB R/W	Event counterr, baud rate generator
8254 programmable timer	Virtual IP Group	AllianceCORE				V		S-II	S					
8254 programmable timer/counter	eInfochips Pvt. Ltd.	AllianceCORE		V-II				S-II		11%	51	XC2V1000-4	Status red, Six prog, counter modes, Intel8254 like	Processor I/O interface
8255 programmable I/O controller	eInfochips Pvt. Ltd.	AllianceCORE		V-II				S-II		2%	175	XC2V1000-5	Three 8-bit parallel ports, 24 programmable IO lines, 8-bit bidi data bus	Processor I/O interface
8255 programmable peripheral interface	Memec Core	AllianceCORE							S	64%	8	XCS05-4	Bit set/reset support	Embedded systems
8255 programmable peripheral interface	Virtual IP Group	AllianceCORE				V		S-II	S		227	XCV50E-8	Three 8-bit peripheral ports, 24 programmable I/O lines, 8-bit bidi data bus	Processor I/O interface
8255A peripheral interface	CAST, Inc.	AllianceCORE				V		S-II		10%	227	XCV50E-8	Three 8-bit peripheral ports, 24 programmable IO lines, 8-bit bidi data bus	Processor I/O interface
8256 multifunction microprocessor support controller	Memec Core	AllianceCORE							S	89%	10	XCS20-4	Baud rate generator for 13 common baud rates, parallel I/O ports, prog. timer/counters	Communication, embedded systems
8259 programmable interrupt controller	Virtual IP Group	AllianceCORE							S			XC2S50-6	8 vectored priority interrupts, all 8259/A modes programmable- e.g., special mask, buffer	Real-time interrupt based uP designs
8259A programmable interrupt controller	CAST, Inc.	AllianceCORE		V-II	V-E	V		S-II		90%	142	XC2V40-5	8 vectored priority interrupts, all 8259/A modes programmable- e.g., special mask, buffer	Real-time interrupt based uP designs
8279 programmable keyboard display interface	Memec Core	AllianceCORE							S	46%	8	XCS20-4	8 char keyboard FIFO, 2-key lockout, n-key rollover, 4-16 char display	Embedded systems interface
Arbiter w/OPB interface	Xilinx	LogiCORE	V-IIP	V-II	V-E	V	S-IIE	S-II			125	XC2V80-5	CoreConnect Bus (OPB), Infrastructure Core	Processor applications
Arbiter w/PLB interface	Xilinx	LogiCORE	V-IIP								150	Virtex-II Pro (-6)	CoreConnect Bus (PLB), Infrastructure Core	PowerPC embedded system design
ARC 32-bit configurable RISC processor	ARC International plc	AllianceCORE			V-E			S-II		89%	37	XC2S150-6	4 stage pipeline, 16 single cycle instructions10, 3 interrupt exception levels, 24 bit stack pointer	32 bit processing, DSP
ATM Utopia Level 2 Master and Slave w/OPB Interface	Xilinx	LogiCORE	V-IIP	V-II	V-E	V	S-IIE	S-II			125	XC2V80-5	CoreConnect Bus (OPB), ATM Core ($)	Networking, communications, processor apps
ATM Utopia Level 2 Master and Slave w/PLB Interface	Xilinx	LogiCORE	V-IIP								150	Virtex-II Pro (-6)	CoreConnect Bus (PLB), ATM Core ($)	Networking, communications, processor apps
BRAM Controller w/OPB interface	Xilinx	LogiCORE	V-IIP	V-II	V-E	V	S-IIE	S-II			125	XC2V80-5	CoreConnect Bus (OPB), Memory Controller Core	Processor applications
BRAM Controller w/PLB interface	Xilinx	LogiCORE	V-IIP								150	Virtex-II Pro (-6)	CoreConnect Bus (PLB), Memory Controller Core	PowerPC embedded system design
External Memory Controller (EMC) w/OPB interface (Includes support for Flash, SRAM, ZBT, System ACE)	Xilinx	LogiCORE	V-IIP	V-II	V-E	V	S-IIE	S-II			125	XC2V80-5	CoreConnect Bus (OPB), Memory Controller Core	Processor applications
External Memory Controller (EMC) w/PLB interface (Includes support for Flash, SRAM, ZBT, System ACE)	Xilinx	LogiCORE	V-IIP								150	Virtex-II Pro (-6)	CoreConnect Bus (PLB), Memory Controller Core	PowerPC embedded system design
GPIO w/OPB interface	Xilinx	LogiCORE	V-IIP	V-II	V-E	V	S-IIE	S-II			125	XC2V80-5	Bundled in the Development Kit, CoreConnect Bus (OPB)	Processor applications
HDLC Controller (Single Channel) w/OPB interface	Xilinx	LogiCORE	V-IIP	V-II	V-E	V	S-IIE	S-II			125	XC2V80-5	CoreConnect Bus (OPB), HDLC Core ($)	Processor applications
I2C w/OPB interface	Xilinx	LogiCORE	V-IIP	V-II	V-E	V	S-IIE	S-II			125	XC2V80-5	CoreConnect Bus (OPB), I2C Core ($)	Networking, communications, processor apps
Interrupt Controller (IntC) w/OPB interface	Xilinx	LogiCORE	V-IIP	V-II	V-E	V	S-IIE	S-II			125	XC2V80-5	Bundled in the Development Kit, CoreConnect Bus (OPB)	Processor applications
IPIF Address Decode w/OPB interface	Xilinx	LogiCORE	V-IIP	V-II	V-E	V	S-IIE	S-II			125	XC2V80-5	CoreConnect Bus (OPB), Interface to custom IP	Processor applications
IPIF DMA w/OPB interface	Xilinx	LogiCORE	V-IIP	V-II	V-E	V	S-IIE	S-II			125	XC2V80-5	CoreConnect Bus (OPB), Interface to custom IP	Processor applications
IPIF Interrupt Controller w/OPB interface	Xilinx	LogiCORE	V-IIP	V-II	V-E	V	S-IIE	S-II			125	XC2V80-5	CoreConnect Bus (OPB), Interface to custom IP	Processor applicationsn
IPIF Master/Slave Attachment w/OPB interface	Xilinx	LogiCORE	V-IIP	V-II	V-E	V	S-IIE	S-II			125	XC2V80-5	CoreConnect Bus (OPB), Interface to custom IP	Processor applicationsn
IPIF Read/Write Packet FIFO w/OPB interface	Xilinx	LogiCORE	V-IIP	V-II	V-E	V	S-IIE	S-II			125	XC2V80-5	CoreConnect Bus (OPB), Interface to custom IP	Processor applications
IPIF Scatter/Gather w/OPB interface	Xilinx	LogiCORE	V-IIP	V-II	V-E	V	S-IIE	S-II			125	XC2V80-5	CoreConnect Bus (OPB), Interface to custom IP	Processor applications
Java processor, 32-bit	Digital Communications Technologies, Ltd.	AllianceCORE		V-II		V		S-II		33%	40	XC2V1000-5	32bit data, 24 bit address, 3 Stage pipeline, Java/C dev. tools	Internet appliance, industrial control, HAVi multimedia, set top boxes
Java processor, configurable core	Derivation Systems, Inc.	AllianceCORE		V-II		V				38%	20	XC2V1000-5	32b data/address optional DES	Internet appliance, industrial control
JTAG UART w/OPB interface	Xilinx	LogiCORE	V-IIP	V-II	V-E	V	S-IIE	S-II			125	XC2V80-5	Bundled in the Development Kit, CoreConnect Bus (OPB)	Processor applications
MicroBlaze Soft RISC Processor	Xilinx	LogiCORE	V-IIP	V-II	V-E	V	S-IIE	S-II			150	Virtex-II Pro (-6)	Soft RISC Processor, 102 D-MIPS, 150 MHz, 900 LUTs in Virtex-II Pro	Networking, communications
OPB2OPB Bridge	Xilinx	LogiCORE	V-IIP	V-II	V-E	V	S-IIE	S-II			125	XC2V80-5	CoreConnect Bus (OPB), Infrastructure Core	Processor applications
OPB2PLB Bridge	Xilinx	LogiCORE	V-IIP								150	Virtex-II Pro (-6)	CoreConnect Bus (PLB), Infrastructure Core	PowerPC embedded system design
PCI2OPB Full Bridge (32/33)	Xilinx	LogiCORE	V-IIP	V-II	V-E	V	S-IIE	S-II			125	XC2V80-5	CoreConnect Bus (OPB), PCI Core ($)	Processor applications
PIC125x fast RISC microcontroller	Digital Core Design	AllianceCORE		V-II		V		S-II			126	XC2V80-5	PIC 12c4x like, 2X faster, 12-bit wide instruction set, 33 instructions	Embedded systems, telecom, audio and video
PIC1655x fast RISC microcontroller	Digital Core Design	AllianceCORE		V-II		V		S-II			140	XC2V80-5	S/W compatible with PIC16C55X, 14-bit instruction set, 35 instructions	Embedded systems, telecom, audio and video
PIC165X compatible microcontroller	CAST, Inc.	AllianceCORE		V-II		V		S-II		61%	128	XC2V80-5	Microchip 16C5X PIC like	Embedded systems, telecom
PIC165x fast RISC microcontroller	Digital Core Design	AllianceCORE		V-II	V-E	V		S-II			126	XC2V80-5	PIC 12c4x like, 2X faster, 12-bit wide instruction set, 33 instructions	Embedded systems, telecom, audio and video
PLB2OPB Bridge	Xilinx	LogiCORE	V-IIP								150	Virtex-II Pro (-6)	CoreConnect Bus (PLB), Infrastructure Core	PowerPC embedded system design
PowerPC 405 Boot Code	Xilinx	LogiCORE	V-IIP								150	Virtex-II Pro (-6)	CoreConnect Bus (PLB), Software IP	PowerPC embedded system design
PowerPC 405 System Reset	Xilinx	LogiCORE	V-IIP								150	Virtex-II Pro (-6)	Used to reset PowerPC based system	
PowerPC Bus Master	Eureka Technology	AllianceCORE				V				3%	80	XCV400-6		
PowerPC Bus Slave	Eureka Technology	AllianceCORE			V-E					10%	80	XCV400E-8		
SDRAM Controller	Eureka Technology	AllianceCORE				V				37%	91	XCV50-6		
SDRAM Controller	NMI Electronics, Ltd.	AllianceCORE				V		S-II			137	XCV50-6	SDRAM refresh, customizable	Embedded systems using SDRAMs
SDRAM Controller, 200 MHz	Rapid Prototypes, Inc.	AllianceCORE				V		S-II						
SDRAM Controller, DDR	Memec Core	AllianceCORE		V-II	V-E			S-II		7%	133	XC2V1000-5	DDR SDRAM burst length support for 2,4,8 per access, supports data 16,32, 64, 72.	Digital video, embedded computing, networking

Function	Vendor Name	IP Type	Virtex-II Pro	Virtex-II	Virtex-E	Virtex	Spartan-IIE	Spartan-II	Spartan	Implementation Example Occ	 MHz	 Device	Key Features	Application Examples
Microprocessors, Controllers & Peripherals (continued)														
SPI	Xilinx	LogiCORE	V-IIP	V-II	V-E	V	S-IIE	S-II			125	XC2V80-5	Bundled in the Development Kit, CoreConnect Bus (OPB)	Networking, communications, processor apps
SDRAM Controller w/OPB interface	Xilinx	LogiCORE	V-IIP	V-II	V-E	V	S-IIE	S-II			125	XC2V80-5	CoreConnect Bus (OPB), Memory Controller Core	Processor applications
SDRAM Controller w/PLB interface	Xilinx	LogiCORE	V-IIP								150	Virtex-II Pro (-6)	CoreConnect Bus (PLB), Memory Controller Core	PowerPC embedded system design
Timebase/Watch Dog Timer (WDT) w/OPB interface	Xilinx	LogiCORE	V-IIP	V-II	V-E	V	S-IIE	S-II			125	XC2V80-5	Bundled in the Development Kit, CoreConnect Bus (OPB)	Processor applications
Timer/Counter w/OPB interface	Xilinx	LogiCORE	V-IIP	V-II	V-E	V	S-IIE	S-II			125	XC2V80-5	Bundled in the Development Kit, CoreConnect Bus (OPB)	Processor applications
UART, generic compact	Memec Core	AllianceCORE		V-II	V-E	V	S-IIE	S-II	S	15%	73	XC2S50E-6	UART and baud rate generator	Serial data communication
UART Lite w/OPB interface	Xilinx	LogiCORE	V-IIP	V-II	V-E	V	S-IIE	S-II			125	XC2V80-5	Bundled in the Development Kit, CoreConnect Bus (OPB)	Processor applications
V8-uRISC 8-bit RISC Microprocessor	ARC International plc	AllianceCORE									16	XC4000E	Proprietary 8-bit processor, 8 bit ALU, 16 bit stack pointer, 33 opcodes, 4 addr. Modes, 2 user opcodes	Embedded systems, 8-bit processing apps.
VxWorks Board Support Package (BSP)	Xilinx	LogiCORE	V-IIP								150	Virtex-II Pro (-6)	Interfaces HW and WindRiver RTOS	Embedded system design
Z80 compatible programmable timer/counter core	CAST, Inc.	AllianceCORE		V-II	V-E	V		S-II		9%	167	XC2V500-5		Programmable frequency divider, Pulse counter, pulse generator, interrupt controller
Z80 peripheral I/O controller core	CAST, Inc.	AllianceCORE		V-II	V-E	V		S-II		49%	76	XC2S50-6		Programmable , dual-port device, keyboards, printers, paper table readers
Z80CPU Microprocessor	CAST, Inc.	AllianceCORE		V-II		V		S-II		56%	72 MHz	XC2V500-5	Zilog Z80 compatible, 8-bit processor	Embedded systems, Communications
Standard Bus Interfaces														
Arbiter	Telecom Italia Lab S.p.A.	AllianceCORE				V		S-II	S	24%	33	XCV50-6	Two priority classes - strong/weak, access counters	General purpose bus arbitration
I2C Bus Controller	CAST, Inc.	AllianceCORE		V-II	V-E	V		S-II		21%	103	XC2S100-6	Philips I2C 1.1; supports master tx/rx and slave tx/rx modes	Embeded microcontroller and communications
I2C Bus Controller Master	Digital Core Design	AllianceCORE		V-II	V-E			S-II	S		143	XC2V40-5	I2C-like, multi master, fast/std. modes	Embedded systems
I2C Bus Controller Slave	Digital Core Design	AllianceCORE		V-II	V-E			S-II	S		157	XC2V40-5	I2C-like, Slave	Embedded
I2C Bus Controller Slave Base	Digital Core Design	AllianceCORE		V-II	V-E			S-II	S		187	XC2V40-5	I2C-like, Slave	Embedded Systems
I2C Two-Wire Serial Interface Master-Only	Memec Core	AllianceCORE		V-II	V-E	V	S-IIE	S-II		16%	83	XC2S50E-6	I2C-like, multi master fast/std. modes	Embedded microprocessor systems, I2C peripherals
I2C Two-Wire Serial Interface Master-Slave	Memec Core	AllianceCORE		V-II	V-E	V	S-IIE	S-II		28%	108	XC2V80-4	I2C-like, multi master fast/std. modes	Embedded microprocessor systems, I2C peripherals
PCI 64-bit/66-MHz master/target interface	Eureka Technology	AllianceCORE		V-II	V-E					22%	66	XC2V1000-5		
PCI host bridge	Eureka Technology	AllianceCORE		V-II	V-E					22%	33	XC2V1000-5		
PCI Express Single Lane Endpoint (DO-DI-PCIEXP-X1)	Xilinx	LogiCORE	V-IIP							25%	Single Channel 2.5 Gbps RocketIO Transceiver	XC2VP20-6	Protocol and electrically compliant to PCI Express specification v1.0	PC and Server boards, backplanes, control planes, high end video
PCI32 Interface Design Kit (DO-DI-PCI32-DKT)	Xilinx	LogiCORE	V-IIP	V-II	V-E	V	S-IIE	S-II		6%	66	XC2V1000 FG456-5	Includes PCI32 board, driver development kit, and customer education 3-day training class for US & Canada locations	PC boards, CPCI, Embedded, hiperf video, gb ethernet
PCI32 Interface, IP Only (DO-DI-PCI32-IP)	Xilinx	LogiCORE	V-IIP	V-II	V-E	V	S-IIE	S-II		6%	66	XC2V1000 FG456-5	v2.3 compiliant, assured PCI timing, 3.3/5-V, 0-waitstate, CPCI hot swap friendly	PC add-in boards, CPCI, Embedded
PCI32 Single-Use License for Spartan (DO-DI-PCI32-SP)	Xilinx	LogiCORE					S-IIE	S-II		12%	66	XC2S200 PQ208-6	v2.3 compiliant, assured PCI timing, 3.3/5-V, 0-waitstate, CPCI hot swap friendly	PC add-in boards, CPCI, Embedded
PCI64 & PCI32, IP Only (DO-DI-PCI-AL)	Xilinx	LogiCORE	V-IIP	V-II	V-E	V	S-IIE	S-II		6 - 7%	66	XC2V1000 FG456-5	v2.3 compliant, assured PCI timing, 3.3/5-V, 0-waitstate, CPCI hot swap friendly	PC boards,CPCI,Embedded,hiperf video,gb ethernet
PCI64 Interface Design Kit (DO-DI-PCI64-DKT)	Xilinx	LogiCORE	V-IIP	V-II	V-E	V	S-IIE	S-II		7%	66	XC2V1000 FG456-5	v2.3 compiliant, assured PCI timing, 3.3/5-V, 0-waitstate, CPCI hot swap friendly, customer education 3-day training class for US & Canada locations	PC boards, CPCI, Embedded, hiperf video, gb ethernet
PCI64 Interface, IP Only (DO-DI-PCI64-IP)	Xilinx	LogiCORE	V-IIP	V-II	V-E	V	S-IIE	S-II		7%	66	XC2V1000 FG456-5	v2.3 compiliant, assured PCI timing, 3.3/5-V, 0-waitstate, CPCI hot swap friendly	PC boards,CPCI,Embedded,hiperf video,gb ethernet
PCI-X 64/100 Interface for Virtex-II (DO-DI-PCIX64-VE). Includes PCI 64 bit interface at 33 MHz	Xilinx	LogiCORE		V-II						30%	100	XC2V1000 FG456-5	PCI-X 1.0a comp, 64/32-bit, 66 MHz PCI-X initiator and target IF, PCI 2.3 comp, 64/32-bit, 33 MHz PCI initiator and target IF, 3.3 V PCI-X at 33-66 MHz, 3.3 V PCI at 0-33 MHz	Server,Embedded,gb ethernet,U320 SCSI,Fibre Ch,RAID cntl,graphics
PCI-X 64/66 Interface for Virtex-E (DO-DI-PCIX64-VE). Includes PCI 64 bit interface at 33 MHz	Xilinx	LogiCORE			VE					30%	66	XCV300E-8	PCI-X 1.0a comp, 64/32-bit, 66 MHz PCI-X initiator and target IF, PCI 2.3 comp, 64/32-bit, 33 MHz PCI initiator and target IF, 3.3 V PCI-X at 33-66 MHz, 3.3 V PCI at 0-33 MHz	comm systems, SAN, clustered servers, Ultra 3 SCSI/Fibre Ch RAID, multi-port Gb
HyperTransport 8-bit Single Ended Slave (DO-DI-HT-SES)	Xilinx	LogiCORE		V-II						21%	100	2V6000FF1152-6	Fully compliant with HyperTransport specification v1.0.1a, verified with API testbench and hardware	Routers, switches, backplane, control plane, data path, embedded sys, high speed interface to memory and encryption engines, high end video
RapidIO 8-bit port LP-LVDS Phy Layer (DO-DI-RIO8-PHY)	Xilinx	LogiCORE	V-IIP	V-II						24%	250	XC2V1000 FG456-5	RapidIO Interconnect v1.1 compliant, verified with	Routers, switches, backplane, control plane, data path, embedded sys, high speed interface to memory and encryption engines, high end video
RapidIO Logical (I/O) and Transport Layer (DO-DI-RIO-LOG)	Xilinx	LogiCORE		V-II						20%	62.5	XC2V1000 FG456-5	RapidIO Interconnect v1.1 compliant, verified with	Routers, switches, backplane, control plane, data path, embedded sys, high speed interface to memory and encryption engines, high end video
Serial Protocol Interface (SPI) Slave	CAST, Inc.	AllianceCORE		V-II	V-E	V	S-IIE			14%	80	XC2S50E-6		Embedded microprocessor boards, and SOCs, audio/video, home and automotive radio
USB 1.1 Device Controller	Memec Core	AllianceCORE		V-II	V-E			S-II			12 MHz	XC2V1000-5	Compliant with USB1.1 spec., Supports VCI bus, Performs CRC, Supports 1.5 Mbps & 12 Mbps	Scanners, Printers, Handhelds, Mass Storage
USB 1.1 Function Controller	CAST, Inc.	AllianceCORE		V-II	V-E	V		S-II		92%	48	XC2S200-6	USB 1.1; up to 31 endpoints; suspend and resume power mgmt; remote wake-up	Embedded systems, communications
Video & Image Processing														
2D discrete/inverse cosine transform	Barco-Silex	AllianceCORE		V-II	V-E	V		S-II		77%	133	XC2V250-5		Picture and video, archiving, digital television compression and transmission, teleconference
2D Forward Discrete Cosine Transform	CAST, Inc.	AllianceCORE		V-II	V-E	V		S-II		42%	83	XC2V500-5		
2D Inverse Discrete Cosine Transform	CAST, Inc.	AllianceCORE		V-II	V-E	V		S-II		45%	95	XC2V500-5		
Block-based 2D Discrete Wavelet Transform	CAST, Inc.	AllianceCORE		V-II	V-E	V		S-II		62%	52	XC2V250-5		
Combined 2D Forward/Inverse Discrete Cosine Transform	CAST, Inc.	AllianceCORE		V-II	V-E	V		S-II		65%	95	XC2V500-5		
Combined 2D Forward/Inverse Discrete Wavelet Transform	CAST, Inc.	AllianceCORE		V-II	V-E	V		S-II		55%	95	XC2V500-5		
Compact Video Controller	Xylon d.o.o.	AllianceCORE		V-II		V		S-II			88	XC2V250-4	Single & double panel, LCD/CRT support, 4 gray, 256 colors	Video phone, Set-top box, PDA display
DCT/IDCT Forward/Inverse Discrete Cosine Transform, 1-D	Xilinx	LogiCORE	V-IIP	V-II	V-E	V	S-IIE	S-II					8-32 pt FDCT, IDCT with 8-24 bits for coeff & input	JPEG, MPEG, H.261, H.263
DCT/IDCT Forward/Inverse Discrete Cosine Transform, 2-D	Xilinx	LogiCORE	V-IIP	V-II	V-E	V	S-IIE	S-II		32%	140 MHz	XC2V1000-5	8x8 parameterized FDCT, IDCT & IEEE 1180-1990 compliant IDCT	JPEG, MPEG, H.261, H.263
Discrete Cosine Transform	eInfochips Pvt. Ltd.	AllianceCORE		V-II	V-E	V	S-IIE	S-II		35%	83	XC2V1000-5	8-bit input/12-bit output precision; 76 clock cycle latency	Video coding and security, medical imaging, scanners, copiers, digital still cameras
Fast JPEG color image decoder	Barco-Silex	AllianceCORE		V-II		V				78%	56 MHz	XC2V1000-4	Conforms to ISO/IEC Baseline 10918-1, color, multi-scan, Gray-Scale	Video editing, digital camera, scanners
Fast JPEG gray scale image decoder	Barco-Silex	AllianceCORE		V-II	V-E	V				68%	73	XC2V1000-4	Conforms to ISO/IEC Baseline 10918-1, Gray-Scale	Video editing, digital camera, scanners
FIDCT Forward/Inverse Discrete Cosine Transform	Telecom Italia Lab S.p.A.	AllianceCORE				V		S-II		77%	78	XCV200-6	DCT for 8X8, 16X16, IDCT IEEE1180-1990 compliant	JPEG, MPEG, H.26X
Huffman Decoder	CAST, Inc.	AllianceCORE		V-II	V-E	V	S-IIE	S-II		22%	25	XC2V1000-5		
JPEG encoder/decoder	inSilicon Corporation	AllianceCORE				V		S-II	S		20	XCV400E-8	Conforms to ISO/IEC Baseline 10918-1, 4 quantization tables, 4 Huffman tables. Stallable	Video editing, digital camera, scanners
Line-based programmable forward DWT	CAST, Inc.	AllianceCORE		V-II	V-E	V		S-II		145%	51	XC2V250-5		

Function	Vendor Name	IP Type	Virtex-II Pro	Virtex-II	Virtex-E	Virtex	Spartan-IIE	Spartan-II	Spartan	Implementation Example			Key Features	Application Examples
										Occ	MHz	Device		
Video & Image Processing (continued)														
Longitudinal Time Code Generator	Deltatec S.A.	AllianceCORE				V				36%	80	XC2S15-5	SMTPE/EBU compliant, PAL/NTSC, lock-on external video reference	Audio/Video recording and editing equipment
Motion JPEG Codec core V1.0	Amphion Semiconductor Ltd.	AllianceCORE		V-II	V-E	V					40	Virtex-II		
Motion JPEG Decoder core V1.0	Amphion Semiconductor Ltd.	AllianceCORE		V-II	V-E	V					42	Virtex-II		
Motion JPEG Encoder core V2.0	Amphion Semiconductor Ltd.	AllianceCORE		V-II	V-E	V					70	Virtex-II		
RGB2YCrCb Color Space Converter	CAST, Inc.	AllianceCORE		V-II	V-E	V	S-IIE	S-II		29%	96	XC2S50E-7	8-bit I/O, 10-bit coeff, 13-bit internal precision; 5-cycle latency; fully synchronous.	Digital RGB to TV output conversion, image filtering, machine vision, still and video image processing.
RGB2YCrCb Color Space Converter	Perigee, LLC	AllianceCORE				V		S-II	S		202	XCV100E-8	One clock cycle throughput	HDTV, real time TV output modulation
YCrCb2RGB Color Space Converter	Perigee, LLC	AllianceCORE				V		S-II	S			XCV100E-8	One clock cycle throughput	HDTV, real time video
Basic Elements														
Binary Counter	Xilinx	LogiCORE	V-IIP	V-II	V-E	V	S-IIE	S-II					2-256 bits output width	
Binary Decoder	Xilinx	LogiCORE	V-IIP	V-II	V-E	V	S-IIE	S-II					2-256 bits output width	
Bit Bus Gate	Xilinx	LogiCORE	V-IIP	V-II	V-E	V	S-IIE	S-II					1-256 bits wide	
Bit Gate	Xilinx	LogiCORE	V-IIP	V-II	V-E	V	S-IIE	S-II					1-256 bits wide	
Bit Multiplexer	Xilinx	LogiCORE	V-IIP	V-II	V-E	V	S-IIE	S-II					1-256 bits wide	
BUFE-based Multiplexer Slice	Xilinx	LogiCORE	V-IIP	V-II	V-E	V	S-IIE	S-II					1-256 bits wide	
BUFT-based Multiplexer Slice	Xilinx	LogiCORE	V-IIP	V-II	V-E	V	S-IIE	S-II					1-256 bits wide	
Bus Gate	Xilinx	LogiCORE	V-IIP	V-II	V-E	V	S-IIE	S-II					1-256 bits wide	
Bus Multiplexer	Xilinx	LogiCORE	V-IIP	V-II	V-E	V	S-IIE	S-II					IO widths up to 256 bits	
Comparator	Xilinx	LogiCORE	V-IIP	V-II	V-E	V	S-IIE	S-II					1-256 bits wide	
FD-based Parallel Register	Xilinx	LogiCORE	V-IIP	V-II	V-E	V	S-IIE	S-II					1-256 bits wide	
FD-based Shift Register	Xilinx	LogiCORE	V-IIP	V-II	V-E	V	S-IIE	S-II					1-64 bits wide	
Four-Input MUX	Xilinx	LogiCORE							S				Not recommended for new designs. Suggested replacement: Bit Multiplexer or Bus Multiplexer	
LD-based Parallel Latch	Xilinx	LogiCORE	V-IIP	V-II	V-E	V	S-IIE	S-II					1-256 bits wide	
Parallel-to-Serial Converter	Xilinx	LogiCORE							S				Not recommended for new designs. Suggested replacement: FD-based Shift Register	
RAM-based Shift Register	Xilinx	LogiCORE	V-IIP	V-II	V-E	V	S-IIE	S-II					1-256 bits wide, 1024 words deep	
Register	Xilinx	LogiCORE							S				Not recommended for new designs. Suggested replacement: FD-based Parallel Register	
Three-Input MUX	Xilinx	LogiCORE							S				Not recommended for new designs. Suggested replacement: Bit Multiplexer or Bus Multiplexer	
Two-Input MUX	Xilinx	LogiCORE							S				Not recommended for new designs. Suggested replacement: Bit Multiplexer or Bus Multiplexer	
Memory Interfaces														
XAPP608:DDR SDRAM DIMM Interface	Xilinx	Reference Design		V-II						645 Slices	100 MHz	XC2V6000-5	64-bit Data at 200 Mbits/s. Burst Sizes 2, 4, 8, or full page. CAS Latency 2.	
XAPP266:Synthesizable FCRAM Controller	Xilinx	Reference Design		V-II							154 MHz	XC2V1000-5	Data Rate 308 Mbits/s. Burst Sizes 2 or 4. CAS Latency 2 or 3.	
XAPP262:Quad DataRate (QDR) SRAM Interface	Xilinx	Reference Design		V-II						150 Slices	167 MHz	XC2V1000-5	Data Rate 333 MHz. Burst Size 2-word.	
XAPP254:The Virtex-II SiberBridge	Xilinx	Reference Design		V-II						838 Slices		XC2V1000-5	Interface between a 32-bit host (network processor) and a SiberCAM device or a cascade of SiberCAM devices.	
XAPP253:Synthesizable 400MBits/s DDR SDRAM Controller	Xilinx	Reference Design		V-II						896 Slices	200 MHz	XC2V3000-5	32-bit Data at 400 Mbits/s. Burst Sizes 2,4,8 or full page. CAS Latency 3.	
XAPP242:Interfacing to Lara Networks Search Engine Using Virtex Devices	Xilinx	Reference Design				V				412 Slices	112 MHz		Write & Burst Write to,Read & Burst Read from, and Search a data or mask array. Single Read and Single Write to an external SRAM device.	
XAPP214:Virtex Device Quad Data Rate SRAM	Xilinx	Reference Design				V				110 Slices	100 MHz	XCV150	18-bit Data at 200 Mbits/s. Burst Size 2-word.	
Interface														
XAPP200:Double Data Rate SDRAM	Xilinx	Reference Design			V-E	V					!00 MHz for V and S-II		64-bit Data at 266 Mbits/s. Burst Sizes 2,4,8. CAS Latency 2,2.5,3.	
											133 MHz for V-E -7			
XAPP136:Synthesizable 200 MHz ZBT SRAM	Xilinx	Reference Design				V					200 MHz for pipelined	XCV300-6	36-bit Data at 200 MHz.	
Interface											100 MHz for flowthrough			
XAPP134:Virtex Synthesizable High Performance SDRAM Controller	Xilinx	Reference Design				V					125 MHz for V-6		32-bit Data. Burst Sizes 1,2,4,8. CAS Latency 2,3.	
Storage Devices														
XAPP291:Self Addressing FIFO	Xilinx	Reference Design	V-II P	V-II							140 MHz for Input Data 200 MHz for Output Data		Main purpose of these FIFOs is to transfer data between clock domains while avoiding the necessity of using a clock tree.	
XAPP261:Data Width Conversion FIFOs using Block RAM Memory	Xilinx	Reference Design	V-II P	V-II									Synchronous and Asynchronous FIFOs.	
XAPP260:Using Virtex-II Block RAM for High-Performance Read/Write CAMs	Xilinx	Reference Design		V-II									Single clock cycle match(read) and write(erase). CAM depth can be increased in multiples of 32.	
XAPP258:FIFOs Using Virtex-II Block RAM	Xilinx	Reference Design	V-II P	V-II									Synchronous and Asynchronous FIFOs.	
XAPP256:FIFOs Using Virtex-II Shift Registers	Xilinx	Reference Design	V-II P	V-II									Synchronous FIFOs. Depth increases in multiples of 16.	
XAPP205:Data Width Conversion FIFOs using Virtex Block SelectRAM Memory	Xilinx	Reference Design				V							Synchronous and Asynchronous FIFOs.	
XAPP204:CAM in Block SelectRAM	Xilinx	Reference Design			V-E	V							Independent write and match data input buses. Fully synchronous match and write ports.Single clock cycle match and write.	
XAPP203:Designing Flexible,Fast CAMs with Virtex Slices	Xilinx	Reference Design			V-E	V							Single clock cycle match. Flexible CAM width and depth.	
XAPP202:CAM in ATM Applications	Xilinx	Reference Design			V-E	V								
XAPP131:170 MHz Synchronous and Asynchronous FIFOs Using the Virtex Block Select RAM Features	Xilinx	Reference Design				V								

Please contact your Xilinx representative for the most up-to-date information.