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The Programmable Logic Company℠

XILINX SPARTAN FPGAs

http://www.xilinx.com/spartan

PRODUCT SELECTION MATRIX

		CLB Resources					BLK RAM		CLK Resources					I/O Features				Speed				
	System Gates (see note 1)	CLB Array (Row X Col)	Number of Slices	Logic Cells (see note 2)	CLB Flip-Flops	Max. Distributed RAM Bits	# Block RAM	Block RAM (kbits)	# Dedicated Multipliers	DLL Frequency (min/max)	# DLL's	Frequency Synthesis	Phase Shift	Digitally Controlled Impedance	Number of Differential I/O Pairs	Max. I/O	I/O Standards	Commercial Speed Grades (slowest to fastest)	Industrial Speed Grades (slowest to fastest)	Serial PROM Family		Config. Memory (Bits)
Spartan-IIE Family — 1.8 Volt																						.18/.15um Six Layer Metal Process
XC2S50E	50K	16 x 24	768	1,728	1,536	24K	8	32K	NA	25/320	4	YES	YES	NA	83	182	LVTTL,LVCMOS2,	-6 -7	-6	ISP	OTP	0.6M
XC2S100E	100K	20 x 30	1,200	2,700	2,400	37K	10	40K	NA	25/320	4	YES	YES	NA	86	202	LVCMOS18, PCI33, PCI66,	-6 -7	-6			0.9M
XC2S150E	150K	24 x 36	1,728	3,888	3,456	54K	12	48K	NA	25/320	4	YES	YES	NA	114	265	GTL, GTL+, HSTL I, HSTL III,	-6 -7	-6			1.1M
XC2S200E	200K	28 x 42	2,352	5,292	4,704	73K	14	56K	NA	25/320	4	YES	YES	NA	120	289	HSTL IV, SSTL3 I, SSTL3 II,	-6 -7	-6			1.4M
XC2S300E	300K	32 x 48	3,072	6,912	6,144	96K	16	64K	NA	25/320	4	YES	YES	NA	120	329	SSTL2 I, SSTL2 II, AGP-2X,	-6 -7	-6			1.9M
XC2S400E	400K	40 x 60	4,800	10,800	9,600	150K	40	160K	NA	25/320	4	YES	YES	NA	172	410	CTT, LVDS, BLVDS, LVPECL	-6 -7	-6			2.7M
XC2S600E	600K	48 x 72	6,912	15,552	13,824	216K	72	288K	NA	25/320	4	YES	YES	NA	205	514		-6 -7	-6			4.0M
Spartan-II Family — 2.5 Volt																						.22/.18um Six Layer Metal Process
XC2S15	15K	8 x 12	192	432	384	6K	4	16K	NA	25/200	4	YES	YES	NA	NA	86	LVTTL, LVCMOS2,	-5 -6	-5	ISP	OTP	0.2M
XC2S30	30K	12 x 18	432	972	864	13.5K	6	24K	NA	25/200	4	YES	YES	NA	NA	132	PCI33 (3.3V & 5V),	-5 -6	-5			0.4M
XC2S50	50K	16 x 24	768	1,728	1,536	24K	8	32K	NA	25/200	4	YES	YES	NA	NA	176	PCI66 (3.3V), GTL, GTL+,	-5 -6	-5			0.6M
XC2S100	100K	20 x 30	1,200	2,700	2,400	37.5K	10	40K	NA	25/200	4	YES	YES	NA	NA	196	HSTL I, HSTL III, HSTL IV,	-5 -6	-5			0.8M
XC2S150	150K	24 x 36	1,728	3,888	3,456	54K	12	48K	NA	25/200	4	YES	YES	NA	NA	260	SSTL3 I, SSTL3 II, SSTL2 I,	-5 -6	-5			1.1M
XC2S200	200K	28 x 42	2,352	5,292	4,704	73.5K	14	56K	NA	25/200	4	YES	YES	NA	NA	284	SSTL2 II, AGP-2X, CTT	-5 -6	-5			1.4M
Spartan-XL Family — 3.3 Volt																						
XCS05XL	5K	10 x 10	100	238	200	3.1K	NA	NA	NA	NA	NA	NA	NA	NA	NA	77	TTL, LVTTL, CMOS,	-4 -5	-4	ISP	OTP	0.05M
XCS10XL	10K	14 x 14	196	466	392	6.1K	NA	NA	NA	NA	NA	NA	NA	NA	NA	112	LVMOS, PCI	-4 -5	-4			0.09M
XCS20XL	20K	20 x 20	400	950	800	12.5K	NA	NA	NA	NA	NA	NA	NA	NA	NA	160		-4 -5	-4			0.18M
XCS30XL	30K	24 x 24	576	1,368	1,152	18.0K	NA	NA	NA	NA	NA	NA	NA	NA	NA	192		-4 -5	-4			0.25M
XCS40XL	40K	28 x 28	784	1,862	1,568	24.5K	NA	NA	NA	NA	NA	NA	NA	NA	NA	224		-4 -5	-4			0.33M

PACKAGE OPTIONS AND USER I/O

			Spartan-IIE (1.8V)							Spartan-II (2.5V)						Spartan-XL (3.3V)				
			XC2S50E	XC2S100E	XC2S150E	XC2S200E	XC2S300E	XC2S400E	XC2S600E	XC2S15	XC2S30	XC2S50	XC2S100	XC2S150	XC2S200	XCS05XL	XCS10XL	XCS20XL	XCS30XL	XCS40XL
Pins	**Body Size**	**I/O's**	182	202	265	289	329	410	514	86	132	176	196	260	284	77	112	160	192	224
PLCC Packages																				
84	30 x 30 mm															61	61			
PQFP Packages (PQ)																				
208	28 x 28 mm		146	146	146	146	146				132	140	140	140	140			160	169	169
240	32 x 32 mm																		192	192
VQFP Packages (VQ)																				
100	14 x 14 mm									60	60					77	77	77	77	
TQFP Packages (TQ)																				
144	20 x 20 mm		102	102						86	92	92	92				112	113	113	
Chip Scale Packages — wire-bond chip-scale BGA (0.8 mm ball spacing)																				
144	12 x 12 mm									86	92						112	113		
280	16 x 16 mm																		192	224
FGA Packages (FT) — wire-bond fine-pitch thin BGA (1.0 mm ball spacing)																				
256	17 x 17 mm		182	182	182	182	182	182												
FGA Packages (FG) — wire-bond fine-pitch BGA (1.0 mm ball spacing)																				
256	17 x 17 mm											176	176	176	176					
456	23 x 23 mm			202	265	289	329	329	329				196	260	284					
676	27 x 27 mm							410	514											
BGA Packages																				
256	27 x 27 mm																		192	205

Note: 1. System Gates include 20-30% of CLBs used as RAM
2. Logic Cell is defined as a 4 input LUT and a register

Important: Verify all Data with Device Data Sheet (http://www.xilinx.com/spartan)

Numbers indicated in the matrix are the maximum number of user I/O's for that package and device combination.

Automotive products are highlighted:
-40C to +125C junction temperature for FPGAs

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