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XILINX VIRTEX-II SERIES FPGAs

http://www.xilinx.com/products/platform/

Pins	Body Size	I/O's	Virtex-II Pro (1.5V)										Virtex-II (1.5V)									
			XC2VP2	XC2VP4	XC2VP7	XC2VP20	XC2VP30	XC2VP40	XC2VP50	XC2VP70	XC2VP100	XC2VP125	XC2V40	XC2V80	XC2V250	XC2V500	XC2V1000	XC2V1500	XC2V2000	XC2V3000	XC2V4000	XC2V6000	XC2V8000
Chip Scale Packages — wire-bond chip-scale BGA (0.8 mm ball spacing)																						
144	12 x 12 mm												88	92	92								
BGA Packages (BG) — wire-bond standard BGA (1.27 mm ball spacing)																						
575	31 x 31 mm																328	392	408				
728	35 x 35 mm																			516			
FGA Packages (FG) — wire-bond fine-pitch BGA (1.0 mm ball spacing)																						
256	17 x 17 mm		140	140									88	120	172	172	172						
456	23 x 23 mm		156	248	248										200	264	324						
676	27 x 27 mm																	392	456	484			
FFA Packages (FF) — flip-chip fine-pitch BGA (1.0 mm ball spacing)																						
672	27 x 27 mm		204	348	396																		
896	31 x 31 mm				396	556	556										432	528	624				
1152	35 x 35 mm					564	644	692	692											720	824	824	824
1148*	35 x 35 mm							804	812														
1517	40 x 40 mm							804	852	964											912	1104	1108
1704	42.5 x 42.5 mm									996	1040	1040											
1696*	42.5 x 42.5 mm										1164	1200											
BFA Packages (BF) — flip-chip fine-pitch BGA (1.27 mm ball spacing)																						
957	40 x 40 mm																		624	684	684	684	

Note: Within the same family, all devices in a particular package are pin-out (footprint) compatible.
Virtex-II packages FG456 and FG676 are also footprint compatible.
Virtex-II packages FF896 and FF1152 are also footprint compatible.
* The FF1148 and FF1696 packages support higher number of user I/O and zero RocketIO™ multi-gigabit transceivers.
Important: Verify all Data with Device Data Sheet (http://www.xilinx.com/partinfo/databook.htm)

Numbers indicated in the matrix are the maximum number of user I/O's for that package and device combination, I/Os for RocketIO MGTs are not included in this table.

Virtex-II Pro Package Configurations with Available RocketIO Transceiver Blocks

Package	XC2VP2	XC2VP4	XC2VP7	XC2VP20	XC2VP30	XC2VP40	XC2VP50	XC2VP70	XC2VP100	XC2VP125
FG256	4	4								
FG456	4	4	8							
FF672	4	4	8							
FF896			8	8	8					
FF1152				8	8	12	16			
FF1148						0*	0*			
FF1517						12	16	16		
FF1704								20	20	24
FF1696									0*	0*

Note: * FF1148 and FF1696 packages support higher number of user I/O and zero RocketIO multi-gigabit transceivers

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			CLB Resources				Memory Resources			DSP	Clock Resources		I/O Features				Speed						
		System Gates (see note 1)	CLB Array (Row X Col)	Number of Slices	Logic Cells (see note 4)	CLB Flip-Flops	Max. Distributed RAM Bits(kbits)	# 18 kbits Block RAM	Total Block RAM (kbits)	# 18x18 Dedicated Multipliers	DCM Frequency (min/max)	# DCM Blocks (see note 2)	Digitally Controlled Impedance	Maximum Differential I/O Pairs	Max. I/O	I/O Standards	Commercial Speed Grades (slowest to fastest)	Industrial Speed Grades (slowest to fastest)	Serial PROM Family	System ACE	Config. Memory (Bits)	RocketIO™ Transceiver Blocks	PowerPC Processor Blocks
Platform FPGAs	**Virtex-II Pro Family — 1.5 Volt**																**.13um Nine Layer Copper Process**						
	XC2VP2	*	16 x 22	1,408	3,168	2,816	44	12	216	12	24/420	4	YES	100	204	LDT-25, LVDS-25, LVDSEXT-25, BLVDS-25, ULVDS-25, LVPECL-25, LVCMOS25, LVCMOS18, LVCMOS15, PCI33, LVTTL, LVCMOS33, PCI-X, PCI66, GTL, GTL+, HSTL I (1.5V,1.8V), HSTL II (1.5V,1.8V), HSTL III (1.5V,1.8V), HSTL IV (1.5V,1.8V), SSTL2I, SSTL2II, SSTL18 I, SSTL18 II	-5 -6 -7	-5 -6	ISP/OTP	ISP	1.31M	4	0
	XC2VP4	*	40 x 22	3,008	6,768	6,016	94	28	504	28	24/420	4	YES	172	348		-5 -6 -7	-5 -6			3.01M	4	1
	XC2VP7	*	40 x 34	4,928	11,088	9,856	154	44	792	44	24/420	4	YES	196	396		-5 -6 -7	-5 -6			4.49M	8	1
	XC2VP20	*	56 x 46	9,280	20,880	18,560	290	88	1,584	88	24/420	8	YES	276	564		-5 -6 -7	-5 -6			8.21M	8	2
	XC2VP30[3]	*	80 x 46	13,696	30,816	27,392	428	136	2,448	136	24/420	8	YES	372	644		-5 -6 -7	-5 -6			11.36M	8	2
	XC2VP40[3]	*	88 x 58	19,392	43,632	38,784	606	192	3,456	192	24/420	8	YES	396	804		-5 -6 -7	-5 -6			15.56M	0**or 12	2
	XC2VP50[3]	*	88 x 70	23,616	53,136	47,232	738	232	4,176	232	24/420	8	YES	420	852		-5 -6 -7	-5 -6			19.02M	0**or 16	2
	XC2VP70[3]	*	104 x 82	33,088	74,448	66,176	1,034	328	5,904	328	24/420	8	YES	492	996		-5 -6 -7	-5 -6			25.60M	16 or 20	2
	XC2VP100[3]	*	120 x 94	44,096	99,216	88,192	1,378	444	7,992	444	24/420	12	YES	572	1,164		-5 -6 -7	-5 -6			33.65M	0**or 20	2
	XC2VP125[3]	*	136 x 106	55,616	125,136	111,232	1,738	556	10,008	556	24/420	12	YES	644	1,200		-5 -6 -7	-5 -6			42.78M	0**,20, or 24	4
	Virtex-II Family — 1.5 Volt																**.15um Eight Layer Metal Process**						
	XC2V40	40K	8 x 8	256	576	512	8	4	72	4	24/420	4	YES	44	88	LDT-25, LVPECL-33, LVDS-33, LVDS-25, LVDSEXT-33, LVDSEXT-25, BLVDS-25, ULVDS-25, LVTTL, LVCMOS33, LVCMOS25, LVCMOS18, LVCMOS15, PCI33, PCI66, PCI-X, GTL, GTL+, HSTL I, HSTL II, HSTL III, HSTL IV, SSTL2I, SSTL2II, SSTL3 I, SSTL3 II, AGP, AGP-2X	-4 -5 -6	-4 -5	ISP/OTP	ISP	0.4M		
	XC2V80	80K	16 x8	512	1,152	1,024	16	8	144	8	24/420	4	YES	60	120		-4 -5 -6	-4 -5			0.6M		
	XC2V250	250K	24 x16	1,536	3,456	3,072	48	24	432	24	24/420	8	YES	100	200		-4 -5 -6	-4 -5			1.7M		
	XC2V500	500K	32 x 24	3,072	6,912	6,144	96	32	576	32	24/420	8	YES	132	264		-4 -5 -6	-4 -5			2.8M		
	XC2V1000	1M	40 x 32	5,120	11,520	10,240	160	40	720	40	24/420	8	YES	216	432		-4 -5 -6	-4 -5			4.1M		
	XC2V1500	1.5M	48 x 40	7,680	17,280	15,360	240	48	864	48	24/420	8	YES	264	528		-4 -5 -6	-4 -5			5.7M		
	XC2V2000	2M	56 x 48	10,752	24,192	21,504	336	56	1,008	56	24/420	8	YES	312	624		-4 -5 -6	-4 -5			7.5M		
	XC2V3000[3]	3M	64 x 56	14,336	32,256	28,672	448	96	1,728	96	24/420	12	YES	360	720		-4 -5 -6	-4 -5			10.5M		
	XC2V4000[3]	4M	80 x 72	23,040	51,840	46,080	720	120	2,160	120	24/420	12	YES	456	912		-4 -5 -6	-4 -5			15.7M		
	XC2V6000[3]	6M	96 x 88	33,792	76,032	67,584	1,056	144	2,592	144	24/420	12	YES	552	1,104		-4 -5 -6	-4 -5			21.9M		
	XC2V8000[3]	8M	112 x 104	46,592	104,832	93,184	1,456	168	3,024	168	24/420	12	YES	554	1,108		-4 -5				29.1M		

Note: 1. System Gates include 20-30% of CLBs used as RAM
2. DCM – Digital Clock Management
3. Virtex-II Series EasyPath solution available to provide a no risk, no effort cost reduction path for volume production.
4. Logic cell = (1) 4 Input (LUT) Look Up Table + Flip Flop + Carry Logic.
* System gate count not meaningful for Virtex-II Pro devices with immersed special blocks such as PowerPC processors and multi-gigabit transceivers.
** The FF1148 and FF1696 packages support higher number of user I/O and zero RocketIO multi-gigabit transceivers.
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