Virtex-II IP-Immersion™ Technology Enables Next-Generation Platform FPGAs

Innovative technology allows the integration of discrete silicon components within Platform FPGAs.

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The Field Programmable Gate Array Revolution began when Ross Freeman, a founder of Xilinx, conceived the FPGA architecture. Abandoning the restrictions of sum-of-products architecture, Ross utilized a host of 16-bit LUTs (Look-Up-Tables), each accompanied by a flip-flop circuit, and all interconnected with programmable routing pathways. This revolutionary formula, first deployed in 1984 in the Xilinx XC2000 family, is still the basis of all FPGA devices today, despite the unprecedented growth in the scale of programmable logic and continual advances in the complexity of the device architecture. It is a testament to the power of Ross's architectural vision that the FPGA has withstood the test of time, and many proposed alternatives in the marketplace.

Introducing the Revolutionary Platform FPGA

Today, in 2001, however, another revolution in programmable logic has begun with the introduction of Xilinx Virtex®-II Platform FPGAs. At the heart of this revolution is the ability to integrate the functions of other discrete silicon devices, such as microprocessors, within an FPGA platform. The integration provided by the Platform FPGA architecture delivers these advantages:

- Increased performance made possible by high-bandwidth, low-latency coupling of intellectual property (IP) blocks
- Enhanced architectural flexibility by virtue of immersion within a high-performance programmable fabric
- Reduced board space, power, and cost.

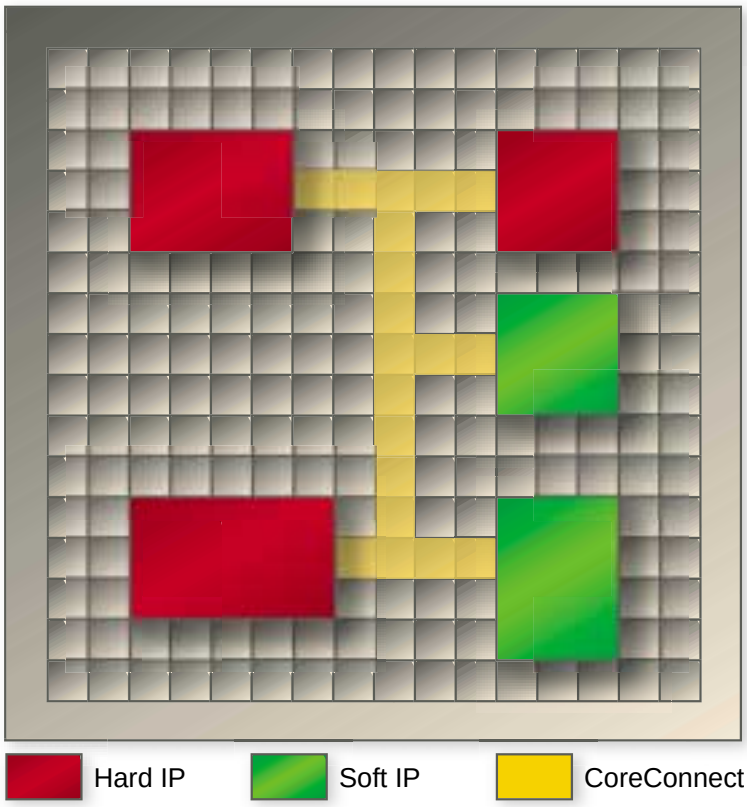
Although Platform FPGAs represent a revolutionary step forward, they still retain the fundamental advantages over ASICs (Application Specific Integrated Circuits) – namely, reprogrammability, off-the-shelf availability, and zero non-recurring engineering (NRE) costs. These advantages comprise the infrastructure that has enabled the development of the innovative IP-Immersion superstructure.

Enhanced Performance Through IP-Immersion

The Virtex-II IP-Immersion™ architecture embodies the concept that high-bandwidth, hard-IP blocks – implemented in full-custom or ASIC-style standard cell logic – can be immersed within the matrix of FPGA CLBs (Configurable Logic Blocks). The two-dimensional array of Virtex-II CLBs is ideally suited for this task, because the array possesses three all-important properties:

1. **Configurable layout** – Because hard-IP blocks (such as microprocessors) have a particular shape, the designer can "cut out" just the right amount of CLBs, creating an empty space for the IP-block. As a result, high performance hard-IP blocks, such as the IBM PowerPC 405 32-bit RISC CPU, can be implemented using advanced circuit design and layout techniques that maximize performance and minimize silicon area. The Virtex-II IP-Immersion architecture accommodates virtually any pre-defined rectilinear shape.

IP-Immersion Technology



2. **Programmable routing** – Through its step-and-repeat of CLB tiles, the segmented routing of FPGA architecture allows the creation of specific "on-ramps" and "off-ramps" at every CLB border. In other words, because the Virtex-II routing architecture has some wiring segments that start within every CLB, these starting segments provide an ideal way for the hard-IP block to interconnect with the logic, memory, and I/Os of the FPGA platform. To provide the transition between the platform fabric and the hard-IP, Virtex-II devices introduce a new tile type: an "immersion tile." The immersion tile allows programmable interconnections between the IP-block and the fabric – much like the interconnection of discrete devices on a printed circuit board. For example, a designer can instantiate a large block and wire it to other parts of the system. In wiring this block, the designer can choose to connect an output pin to a net, leave an output unconnected, tie inputs to fixed one or zero levels, or connect an input to a particular net. In this way, the designer has full design flexibility in using IP blocks.

3. **High performance functionality** – The high wiring density and fully active nature of the Virtex-II routing architecture allows connections to occur in large quantities and at high speed, thus enabling the high-bandwidth interconnect necessary to fully exploit the potential of on-chip IP blocks.

Taken together, these three properties constitute the key ingredients of the new Virtex-II IP-Immersion architecture.

Conclusion

The Virtex-II series of Platform FPGAs are engineered to provide leading-edge functionality in logic, routing, clocking, DSP, memory, and I/O. Thanks to the innovative IP-Immersion architecture and development relationships with leading companies such as IBM, Xilinx Virtex-II Platform FPGAs are facilitating the next generation of advanced system designs.