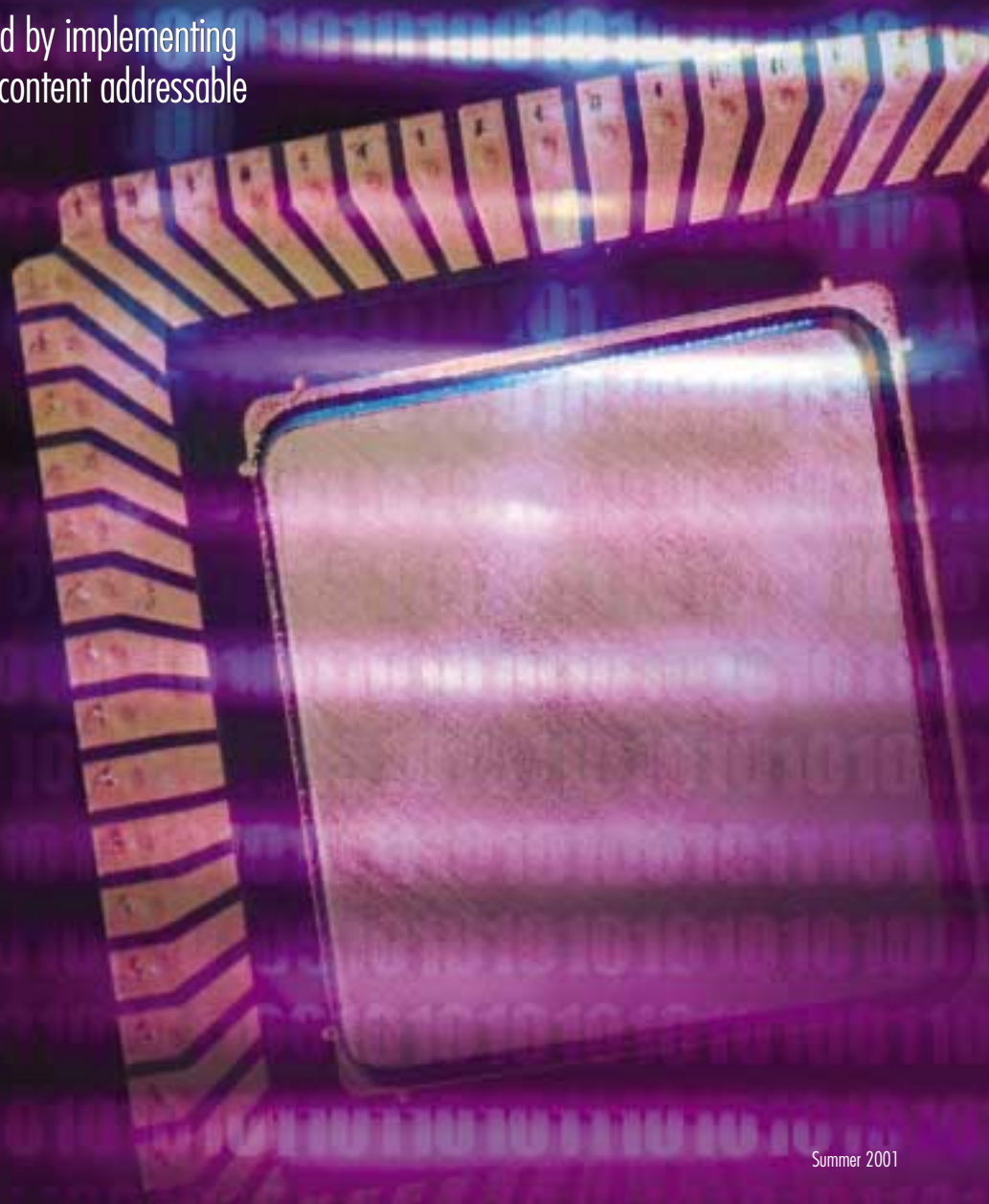
SiberBridge: A Virtex-II Platform FPGA Interface for SiberCAM Arrays

You can quadruple your network speed by implementing a Xilinx Platform FPGA interface with content addressable memory arrays from SiberCore.



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Forwarding and classifying packets typically devour 60% to 70% of a network processor's cycle capacity. Canada-based SiberCore Technologies, however, has developed a large capacity packet forwarding and classification network co-processor – SiberCAM™ – that can significantly increase switch and router throughput by off-loading packet forwarding and classification functions from the network processor.

To help you determine how much one or more SiberCAM co-processors can improve the efficiency of your network, Xilinx and SiberCore have teamed to create the Virtex™-II SiberBridge – a high-performance Platform FPGA RTL (Register Transfer Level) reference design that inter-

faces a 32-bit host processor (typically a network processor) with one or more SiberCAM co-processors. The SiberBridge initiates searches, obtains search results, and performs table maintenance operations for the SiberCAM packet-forwarding subsystem through a single 32-bit synchronous SRAM (Static RAM) interface. The SiberBridge offers fully synthesizable Verilog/VHDL reference code operating at 100 MHz to dramatically simplify board design, maximize system performance, and accelerate time to market for network equipment developers.

The SiberBridge utilizes the special features of the Virtex-II Platform FPGA architecture, including:

- DCM (Digital Clock Manager) to deskew the system clock
- Dedicated block SelectRAM™ for enhanced performance in saving context results
- DDR (Double Data Rate) registers in Virtex-II I/O blocks to burst data into the SiberCAM device.

As a reference design, the SiberBridge has a relatively low gate count.

SiberCAM Device Overview

A CAM (Content Addressable Memory) is a storage device designed to quickly determine whether a particular value exists in its memory, and if so, at which location. The SiberCAM device uses a ternary search operator that takes three arguments: "0", "1", and "don't care". Data can be of variable width.

Data is presented to the SiberCAM device on its search data port. After several clock cycles, a result is provided at its search result port. This result is the address of the best match between the input data and data within the SiberCAM device.

The SiberCAM device is either configured or loaded with its ternary data by performing maintenance operations. To maximize performance, these maintenance operations can be done at the same time as search operations by using a separate 36-bit maintenance port. Both the search data and search result ports remain available, permitting uninterrupted address lookups.

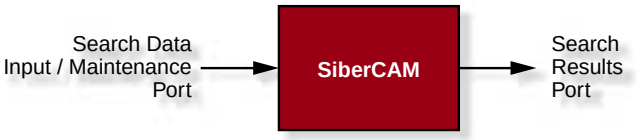

Figure 1 - SiberCAM device in 2-port mode

For applications that do not require maintenance operations to be performed in parallel with search operations, the SiberCAM device can be used in a 2-port mode. In this mode, the maintenance operations are performed using the search data port (Figure 1). In either case, the SiberCAM device expects maintenance operations to be performed in 36-bit/72-bit multiplexed quantities.

Virtex-II – SiberCAM Interface

Optimal performance of the SiberCAM device is achieved when it is used in its native 3-port or 2-port modes. However, in some applications, it is desirable to perform maintenance operations, initiate search operations, and retrieve search results from a single 32-bit interface (for example, when the SiberCAM device is used as a co-processor with a network processor).

The SiberBridge RTL reference design permits either a single SiberCAM device or a cascade of SiberCAM devices to connect to a single 32-bit port. Typically, the 32-bit port would be on a network processor. With SiberBridge, this processor can initiate searches, obtain search results, and perform maintenance operations, all using a single 32-bit synchronous SRAM or ZBT (Zero Bus Turnaround) SRAM interface. The Virtex-II DCM, block SelectRAM, and on-chip DDR registers combine to make the Xilinx FPGA an ideal choice for this interface. Figure 2 shows the interface signals between the SiberCAM device on one side of the SiberBridge design and a network processor on the other.

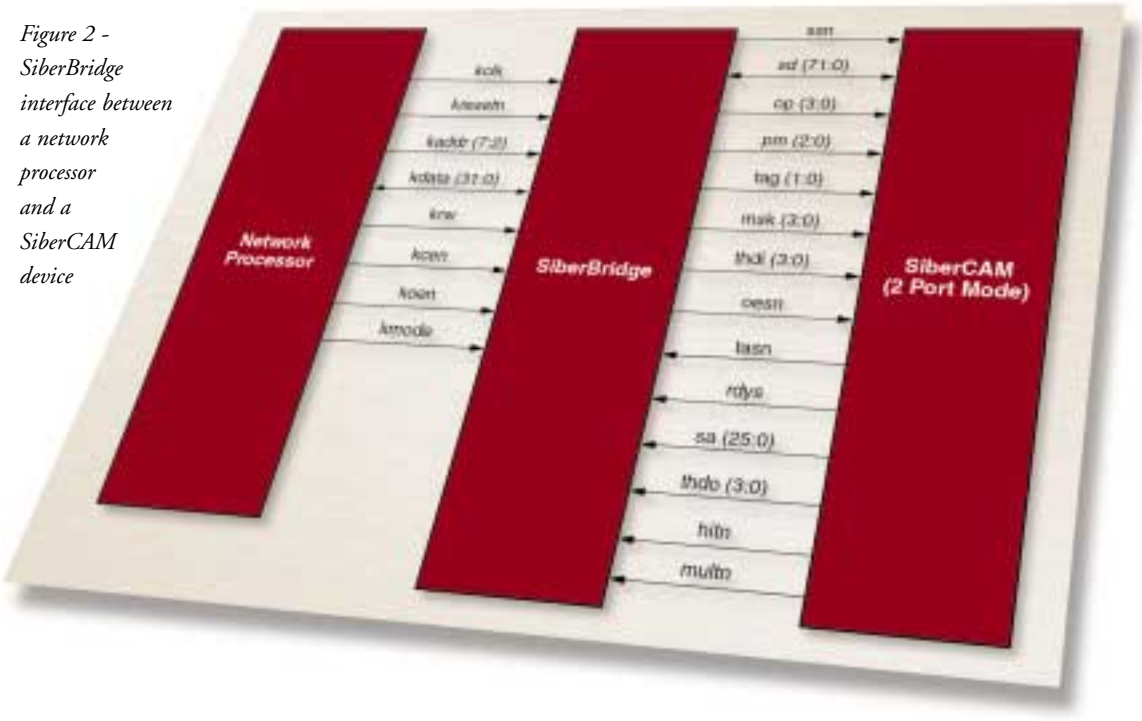

Figure 2 - SiberBridge interface between a network processor and a SiberCAM device

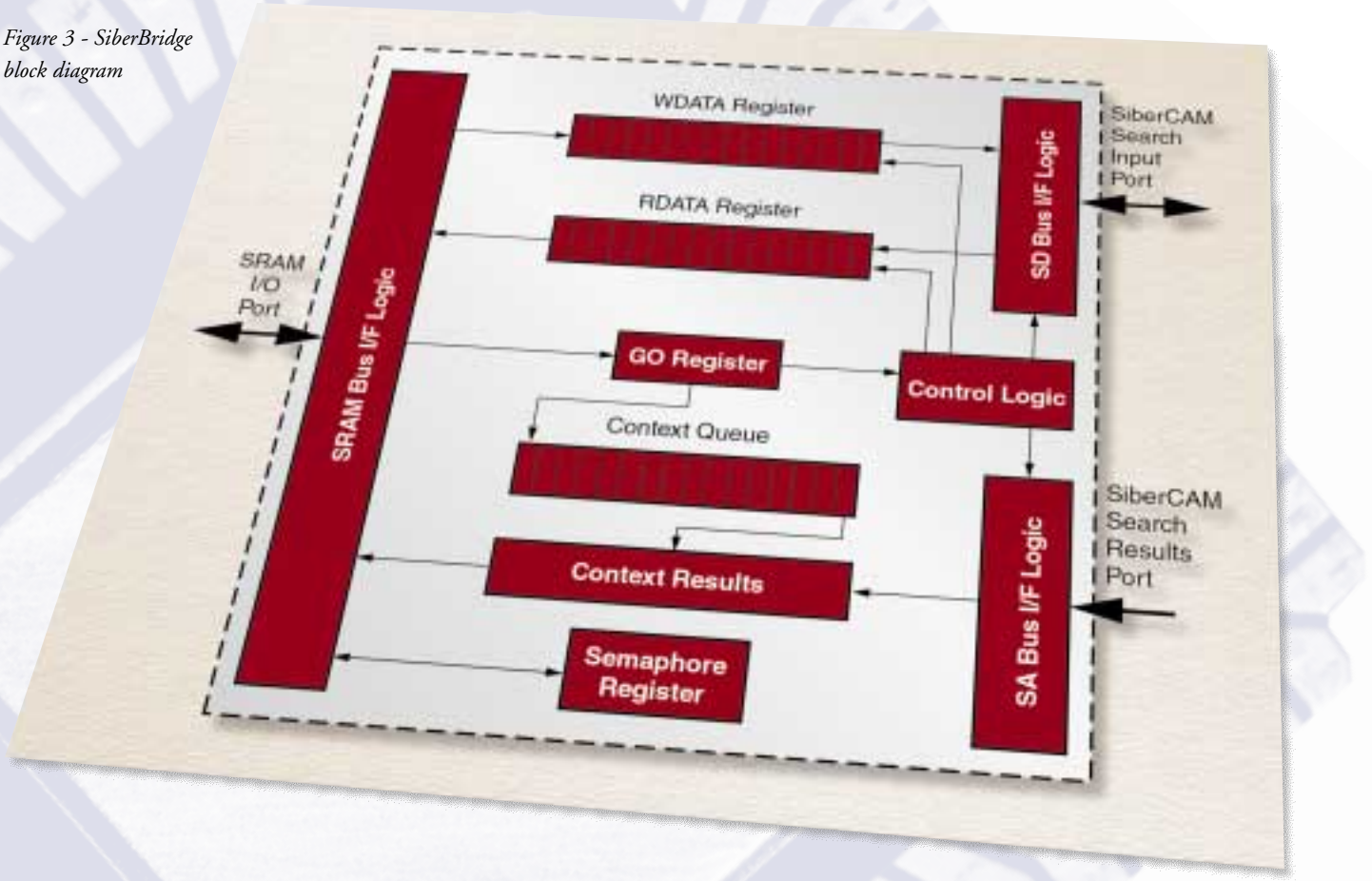

Figure 3 - SiberBridge block diagram

How SiberBridge Works

The SiberBridge design enables maintenance and search operations to be initiated using 32-bit registers. Up to 32 concurrent search requests can be supported, each in its own context.

The SiberBridge interface contains two register files that can be written to or read by the processor in 32-bit quantities. These registers communicate with the SiberCAM device using 72-bit transfers. These transfers are initiated by writing to the GO register. For example, consider a maintenance write operation. The opcode, address, and data are all written to the "write data" register file. Once the data is loaded, writing to the GO register transfers the data to the SiberCAM device, and the operation commences. Search operations are initiated in a similar manner.

For maintenance operations that get data from the SiberCAM device, the SiberBridge captures the data in 72-bit quantities. The data is then stored in the "read data" register file until it is accessed by the processor.

The SiberBridge does not decode the data written to the write data register file. As a result, it is unaware of whether a maintenance operation will return data. While this simplification significantly reduces the complexity of the SiberBridge, it does impose a slightly greater software burden. The software has to know when to expect return data. The block diagram in Figure 3 illustrates the registers that write data to the SiberCAM device and capture data from it.

Virtex-II Solution for Next-Generaton Networking

Combining a SiberCAM co-processor with an existing network processor can increase router or switch throughput by as much as four times. For example, a router with a processor operating at 622 Mbps can increase its throughput to 2,488 Mbps by adding a SiberCAM co-processor.

The enabling technology – a Virtex-II Platform FPGA – is a single-chip solution. With as many as 10 million system gates, an abundance of on-chip memory options, and advanced routing resources, the Virtex-II Platform FPGA interface enables you to eliminate external termination resistors with on-chip XCITE™ digitally controlled impedance technology, manage 16 pre-engineered low skew clock domains, and control frequency and phase with digital clock managers. Furthermore, on-chip DDR registers (input and output) and 18 Kb dual-port RAM make the Virtex-II Platform FPGA the technology of choice for next-generation of network switching and routing subsystems.

For more information, see www.xilinx.com/xapp/xapp254.pdf and www.sibercore.com/products.htm.