System ACE Technology: Configuration Manager Breakthrough

New configuration manager technology from Xilinx provides a flexible, pre-engineered, high-density configuration solution for FPGA-based systems.

by Eric Thacker
Product Marketing Manager, Xilinx
eric.thacker@xilinx.com

Systems designers today face unprecedented challenges and opportunities in bringing advanced products to market. Design schedules are compressing, and new technologies and standards are constantly arising and changing. Customer demands have competitors aggressively vying for superior market positioning. In such an environment, customers are increasingly turning to programmable logic to meet time-to-market requirements, achieve system flexibility and performance targets, and tap into new technologies sooner than competitors using static or custom logic elements.

To meet the demands of state-of-the-art system designers, Xilinx has launched its Platform FPGA Initiative, which provides designers with next-generation FPGA architectures, cutting-edge design tools, and all the necessary implementation technologies needed to design advanced Platform FPGA-based systems.

One of the most important considerations in designing high performance systems is FPGA configuration management. As the number, size, and complexity of FPGAs per system grow, providing a pre-engineered, flexible, and high-density configuration solution becomes even more critical. As part of its Platform FPGA Initiative, Xilinx has developed the System ACE™ configuration manager. This solution provides unprecedented configuration flexibility, storage density, and scalability in a drop-in, ready-to-implement module.

Trends in FPGA Usage

Until recently, programmable logic devices were primarily used as "glue logic," tying various system functions together and acting as programmable high-speed interface logic. FPGA usage was usually limited to one or two devices per system.

Now, however, due to the integration of specialized functionality and the expansion of performance and capabilities, current-generation reprogrammable FPGAs are becoming the core of advanced electronic systems, performing a variety of specialized and generic functions. FPGAs are at the heart of system development because the Xilinx Platform FPGA Initiative integrates specialized functions, high-performance applications, and interface circuitries into the FPGA "fabric." The increased capabilities and flexibility of FPGAs relative to ASICs – especially in a world of greatly compressed product development cycles – has accelerated the use of multiple FPGAs for system core logic. Additionally, the average density of FPGAs designed into new systems is growing rapidly. According to Dataquest, average individual FPGA design-in density grew 113% in 1999 and 67% in 2000.

Configuration Challenges

The increased usage of FPGAs in individual electronic systems is leading to a growing focus on FPGA configuration design. When only one or two FPGAs are used in a system, often only one configuration bitstream is needed. In this case, a dedicated configuration PROM is a fast and simple configuration solution. The speed and ease of implementing a PROM-based solution offsets the cost of additional board space taken up by the PROM.

As the number of FPGAs per system and the need for flexibility in configuration grows, however, using multiple dedicated PROMs becomes unwieldy. With multi-FPGA systems, it becomes more efficient to have a centralized source for configuring all FPGAs. The standard solution has been to use an on-board flash memory controlled by an embedded microprocessor or PLD.

Figure 1 - The System ACE configuration manager is a two-component solution: an ACE Flash module (left) and an onboard ACE Controller logic device.

With a microprocessor, configuration data is pulled directly from system memory over the memory bus and fed to the FPGAs through the JTAG interface. Alternatively, PLDs paired with commodity flash memory can be used to configure FPGA chains, supplying bitstream data either serially or eight bits at a time. PLDs manage the chip enable and address lines while configuration data is fed to the FPGA chain.

While these are valid options, such embedded FPGA configuration techniques are complex design challenges requiring valuable development resources. For example, system engineers must devote design effort to develop and test microprocessor code for FPGA configuration. Furthermore, system startup times are delayed as the microprocessor attempts to manage general system startup and FPGA configuration simultaneously.

Bus contention is also a danger during system startup when the FPGAs compete with other board resources for microprocessor and memory access. Moreover, embedded solutions require extra board space for the additional configuration storage memory. Using JTAG Boundary Scans for board testing and FPGA programming can require separate trace lines and scan-chain-control devices. When using FPGAs and CPLDs (Complex Programmable Logic Devices) as configuration controllers, a device is added to the board simply to convert FPGA clocks to address increments, and in serial mode, to serialize the data. The FPGA also needs a separate PROM to configure it as the controller.

The System ACE Configuration Solution

Given the options described above and the growing need for configuration flexibility, designers using multiple FPGAs were faced with the need to make a tradeoff: Use a self-contained, pre-engineered, multi-PROM solution at the expense of board space, or devote engineering development and debug time to design customized, space-efficient, flexible configuration solutions using onboard resources.

To solve this problem, Xilinx developed the System Advanced Configuration Environment (System ACE) configuration manager – a space-efficient, pre-engineered, high-density configuration solution for multi-FPGA systems. The System ACE configuration manager is a very flexible, two-piece configuration solution comprised of the ACE Flash™ module and the ACE Controller™ chip, as shown in Figure 1. The ACE Flash interface accommodates removable CompactFlash (64 Mb to more than 1 Gb) modules, or the IBM Microdrive (2 Gb to 8 Gb), all with the same form factor and board space requirements.

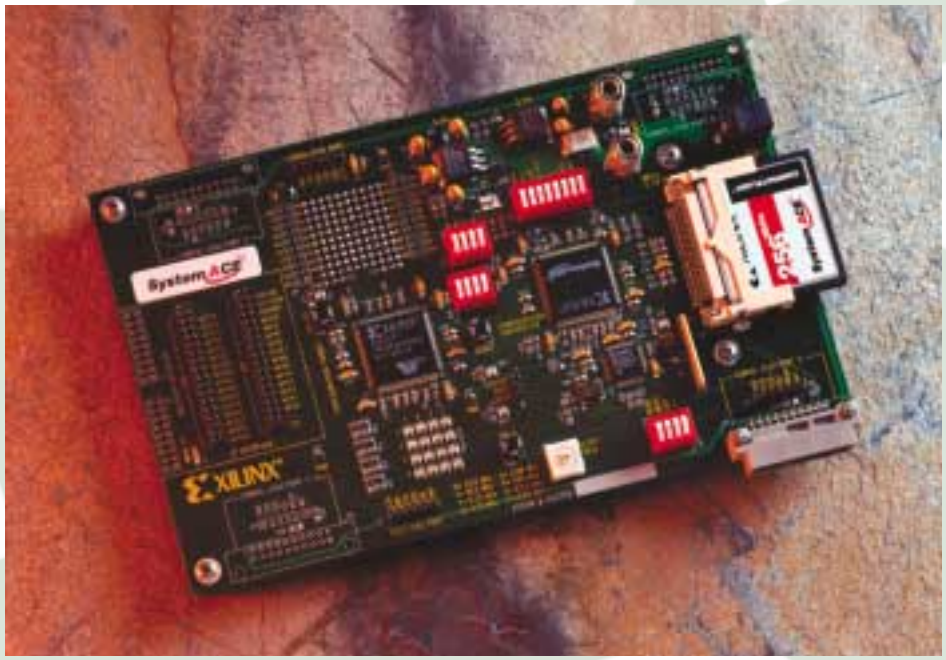

Figure 2 - This System ACE demonstration board features a Virtex-II FPGA, an ACE Controller chip, and a removable 256 Mb ACE Flash module.

For perspective, individual Virtex-II FPGAs require from 300 Kb to 33.5 Mb of configuration data. This means that more than 200 of the largest members of the V-II family can be configured with one System ACE solution. The use of a CompactFlash interface gives system designers access to high-density flash memory in a very efficient footprint that does not change with density or product generation. This technology gives designers the flexibility to change the density of ACE Flash memory without a board redesign. Because the CompactFlash interface supports removable media, designers can change or upgrade the content of the memory by either swapping removable modules or programming in-system.

The ACE Controller chip comes with built-in control logic and a variety of specialized interfaces. This device is the interface to the ACE Flash module, the FPGA chain, an external test environment, and a system microprocessor. The circuitry is optimized for reading data from and writing data to the ACE Flash module. The default configuration mode takes bitstreams from the memory module and configures a chain of FPGAs via a JTAG chain. There is also a test JTAG interface for programming and testing of any devices supporting JTAG Boundary Scan.

The two main advantages of the System ACE solution are system configuration management and upgrade management.

System Management

System ACE technology is the first pre-engineered, centralized configuration solution to provide both the bit density and the control logic to manage configuration for all FPGAs within a system. Along with an optimized memory-to-FPGA-chain interface, there is also an interface for access to the FPGA chain by external programmers/testers, and a generic microprocessor interface for integrating System ACE technology with the rest of the system.

Centralizing configuration management minimizes board space, simplifies changing bitstreams (either during prototyping or in the field), and allows system microprocessors to have a more interactive role in leveraging reconfiguration to increase system flexibility. In systems with multiple boards connected through a backplane, one System ACE module can be used per board to manage the FPGA configuration of each board. If, however, one JTAG chain connects all FPGAs across multiple boards, one System ACE module can configure all FPGAs across multiple boards.

System ACE technology allows for the storage of multiple bitstreams at one time in one location, permitting one board design to serve multiple purposes. For example, if slight variations of an FPGA-based system are being shipped to different markets (for example, to accommodate different interface, broadcast, or electrical standards), a single board can be designed for all these markets, simply with different default system configuration bitstreams determining system functionality.

For designs using FPGAs with Empower! embedded processors, System ACE can be used to configure the FPGA, provide the boot code for the embedded processor core, and store and deliver the application software to be run on the processor core. This gives a self-contained, drop-in configuration and software storage solution for FPGAs with embedded processors, requiring no interaction with an external processor.

Upgrade Management

System ACE technology greatly simplifies upgrading or debugging FPGA-based systems. To add or update a configuration to an FPGA-based system, a new or changed bitstream is stored in the ACE Flash module. Because it is centralized, System ACE technology enables entire system updates simply by physically replacing the ACE Flash module or – better yet – reprogramming the module in-system.

Because System ACE technology uses removable media, system managers or designers can easily remove an ACE Flash memory module (See Figure 2) and either reprogram it on a desktop or replace it with another module containing the updated bitstream files. Whether for a prototyping board in a lab or an installed system in the field, manually reconfigur-

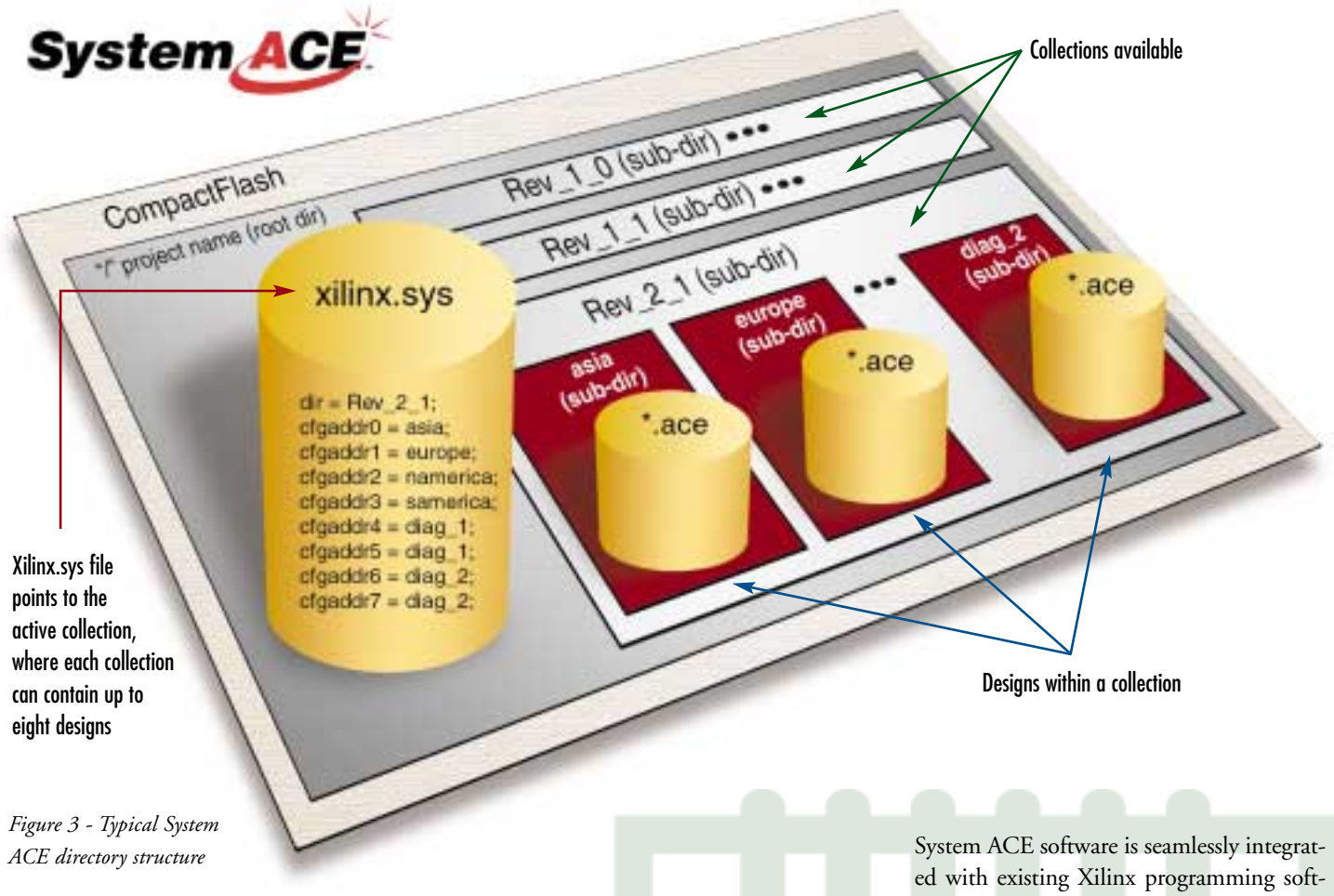

Figure 3 - Typical System ACE directory structure

ing an FPGA-based system using System ACE technology requires little effort.

ACE Flash memory can also be programmed and read in-system, facilitating easy updates and revisions. This capability eliminates many requirements for systems to be manually updated. In-system programming can be accomplished by download cable or through a network interface. Network reconfiguration of System ACE memory eliminates the need for a direct interface. Designers can remotely update or debug systems by transmitting a new bitstream over a network (such as, Internet or wireless WAN). In addition, the ability to store multiple bitstreams and have the microprocessor activate any bitstream at any time allows system administrators to maintain direct access to all previous versions of system configuration.

The ACE Flash file structure simplifies the storage and management of multiple bitstreams. This multiple bitstream capability empowers designers to use a single ACE Flash card to run BIST (Built-In Self Test) patterns, PCI applications, or to store multiple bitstream variations on a single design (for example, versions for North America, South America, Europe, and Asia – see Figure 3). Also, Xilinx FPGA designers with Empower! embedded processors can store the FPGA configuration bits and the processor microcode in the same source. System ACE technology handles the initialization of both the FPGA cells and the delivery of microprocessor initialization software. In addition to configuration data, designers can store related information with the bitstreams, including release notes, revision history, user guides, FAQs, or any other supporting files. The microprocessor interface helps to fully use the ACE Flash capacity for purposes other than bitstream storage, such as generic scratchpad memory.

System ACE software is seamlessly integrated with existing Xilinx programming software. A standard file management structure allows for drag-and-drop file manipulation on ACE Flash modules from any Windows™ environment. Unix versions will also be available in 2001.

Designers can use ACE Flash modules supplied by Xilinx (128 Mb or 256 Mb) or any standard CompactFlash modules available from a variety of third-party suppliers. IBM Microdrives may also be used. The ACE Controller will be offered in a 144-pin TQFP package.

Conclusion

Multiple FPGAs are becoming the core logic of modern electronic systems, resulting in a growing demand for pre-engineered, flexible, and robust configuration solutions. System ACE technology frees systems engineers from reinventing an FPGA configuration system for each design project, enabling them to focus their design efforts on maximizing system performance and achieving faster time to market.