The Future of Platform FPGAs

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A look at the Xilinx philosophy behind the Virtex family development.

The Virtex FPGA family is, without a doubt, the most advanced programmable logic solution ever conceived. Because of its system-level features, extreme density, and high performance, this family has given you design options that were never possible before, and has made it much easier for you to produce better designs in less time.

We designed the Virtex architecture, from the very beginning, as a technology platform on which we can build future generations of the Virtex family. This platform is optimized for use with both hard cores and soft cores, allowing us to offer you the flexibility of programmable logic along with the performance advantages of embedded hard logic, all tightly integrated with our high level development tools that significantly increase your productivity.

The Virtex family just keeps getting better, and the future looks very bright.

Performance Philosophy

Our first priority, with all of our devices, is to continuously improve the performance, density, and features. We work very closely with our manufacturing partners to refine our manufacturing processes, creating increasingly smaller geometry CMOS technologies that result in faster, denser devices, for less cost – we will introduce a new generation every year with increasingly advanced process technology. In addition, we are continuously developing new ways to improve our device architectures, to get better performance through enhanced routing and design features.

Today, you can purchase Virtex-II devices with up to 6 million system gates, a huge advancement in density over previous FPGAs. Yet, within three or four years we will offer 50 million gate devices – enough logic to build very complex, very high performance systems, on a single chip. In addition, Virtex-II devices now operate at internal clock speeds above 200 Mhz, the equal of many custom ASICs. Yet, every year, for the next four to five years, we expect a performance increase of 30% to 50%. (The inherent silicon performance increase is about 30% per year. Then, as we improve the routing infrastructure and so on, we expect up to another 20%.) As you can see, programmable logic technology is advancing very quickly, giving you more options, more capability, more flexibility, and more reasons to move away from ASICs and fixed logic designs.

The basic structure of an FPGA determines not only its capability and its ease of use, it also determines its ability to evolve as new technologies are developed and implemented. You want your FPGA family to grow with your needs without having to learn new tools, processes, and design techniques. That's why we developed a flexible, highly predictable, forward-thinking architecture that can easily integrate custom logic, soft cores, hard cores and mixed signal capability.

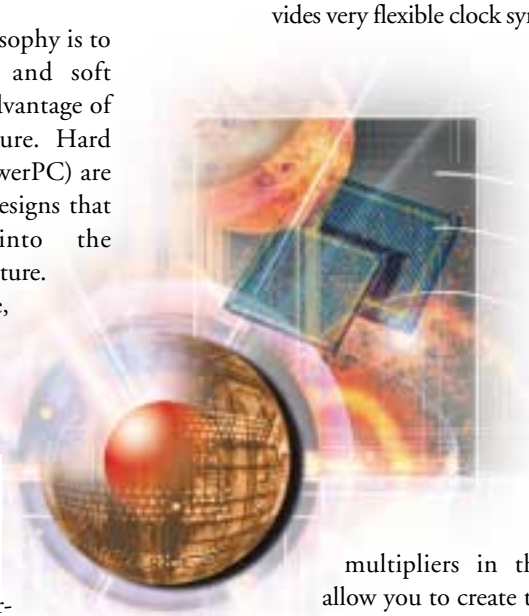
With the Virtex-II family you'll not only achieve high performance, you'll do it with a high degree of predictability and family stability which is key to your productivity. Plus, migrating to larger devices with higher performance, as they are developed, is easy.

It all starts with a strong FPGA platform, tightly integrated with fast, high-level development tools – and there is no end in sight to where this family can go.

Core Philosophy

As device densities keep increasing, it becomes even more important that we provide a wide range of intellectual property or cores, which help you quickly develop your design. Without cores, it would take many engineer-years to complete a 10-million gate design. With cores you can quickly create key parts of your system using proven, reliable designs.

Our "platform" philosophy is to provide both hard and soft cores that take full advantage of our Virtex architecture. Hard cores (such as the PowerPC) are actually fixed logic designs that we incorporate into the FPGA device architecture. Wherever possible, we'll offer soft cores to solve your design challenges because they are more flexible and are used on an as needed basis. We'll offer hard cores when there is a performance or density advantage. The Virtex architecture allows you to easily integrate both types of cores into your designs, giving you the maximum flexibility and performance



Hard Cores

As we move forward, we'll integrate more and more hard cores into our FPGA platform to increase the performance and ease of use. Examples include central processors, memory blocks, clock managers, multipliers, and high speed I/O systems.

Processor cores save you a lot of development time and they give you a known, reliable design. Our philosophy is to tightly integrate our processor cores into the FPGA fabric so you can achieve tremendous performance advantages that would not be available if you used a separate processor chip.

Memory is a critical part of most designs. The ratio of memory to logic gates in the Virtex family will continue to increase over time because our customers are demanding more and more memory. The amount of block RAM and distributed RAM will increase, as well as the ability to access off-chip memory – as memory standards evolve, so will our memory interface capability.

Clock management is another critical factor in large designs. The Virtex-II Delay Locked Loop Digital Clock Manager is already the most advanced, feature rich, clock manager in the industry. It eliminates clock skew, provides very flexible clock synthesis capabilities, and gives you the ability to drive and synchronize clocks both on and off chip, thus eliminating external components and simplifying your design. It will evolve as we develop even more advanced techniques.

The embedded multipliers in the Virtex family allow you to create the fastest possible DSP designs. Our customers are achieving unprecedented speeds, well over 600 billion MACs (Multiply-Accumulate Cycles per second). Many customers are pushing the limits of performance and density in their networking designs, requiring very sophisticated DSP algorithms to extract the data from the noise. Because these hard core multipliers are so useful, in a wide range of applications, they will be added to every Virtex-family FPGA.

We will continue to develop hard and soft cores that make full use of the Virtex family architecture, to bring you all the ease-of-use and performance advantages that make Platform FPGAs so attractive.

I/O Philosophy

Over the last few years we have made tremendous progress in the I/O capabilities of our devices. In the past, I/O blocks were

very standard, and they could usually support just one voltage. Today with the Virtex-II family we support the vast majority of I/O standards in the industry. If you look at a combination of different standards and drive currents, we have 49 different ways that you can program every single I/O pin. And we will continue to add new I/O capabilities as standards evolve.

High Speed Serial I/O

The demands of high speed networking, and other high performance systems, requires the use of gigabit-per-second serial I/O capability for interconnecting devices, backplanes, and systems. In addition, some of the new communications standards and backplane standards are based on these high speed serial I/O capabilities, including POS-PHY4, FlexBus4, HyperTransport™, InfiniBand™, Fibre Channel, Gigabit Ethernet, and so on. With the Virtex-II I/O capability you can connect directly to a backplane without external components.

Through our Conexant Skyrail™ licensing agreement, we gained access to the highest speed I/O technology available – currently giving us a serial transceiver capability of up to 3.125 Gbps. With our RocketChips® acquisition, we expect our serial transceiver technology to reach 10 Gbps or more, as our process and design technologies continue to improve. Future Virtex families will allow you to make full use of this important capability.

Processor Philosophy

We intend to offer you a choice of processors using both hard and soft cores; all using the same peripherals so you can easily combine processors in your designs.

PowerPC Hard-Core Processor

Our PowerPC hard core is being developed in partnership with IBM. It gives you a well-known, very high performance architecture. We will embed this processor within our programmable logic fabric, so all of the processor I/O pins are available to the internal programmable logic for maximum flexibility. Plus, the processor I/O pins do not take up valuable FPGA I/O resources, unless you need them. This allows you to move data much faster than the competition. Our competition's embedded processor does not have the same performance or flexibility as our PowerPC core.

Our philosophy is to provide all of the peripherals and so on as soft cores so they require no resources if you don't need them; we chose to provide the PowerPC processor as a hard core because it gives you a performance advantage. As IBM continues to improve the performance of the PowerPC, Xilinx will continue to offer the latest PowerPC processor core technology, optimized for the Virtex architecture.

MicroBlaze Soft-Core Processor

Our MicroBlaze™ soft-core processor was developed by Xilinx. It uses only about 800 logic cells, requires about the same physical space as the PowerPC, and runs at 125 Mhz. By next year, it will be running at over 150 Mhz.

MicroBlaze is fully integrated with the Core Connect architecture of IBM which means it can use the peripheral modules we're developing for the PowerPC processor. In fact, you can use it in addition to the power PC processor. For example, you can have a combination of the PowerPC and one or more MicroBlaze cores spread around it, all using the same memory and peripherals. The possibilities are limitless.

No other company has this flexible multiprocessor capability. Plus, our MicroBlaze soft core runs almost as fast as our competition's hard core processor

Board Integration Philosophy

With each new generation of the Virtex family we will integrate more and more of the discrete components that are required to create a working system, making your PC boards simpler and less expensive. Our goal is to make our I/O structure so extensive that you will never have to use glue logic or understand the intricacies of each new standard. For example, by integrating a variety of different memory interfaces into our FPGAs, you can easily connect any known memory device without having to create your own custom interface designs.

All of these trends will continue in the future – as new I/O standards are introduced, we'll make them available on our FPGAs.

XCITE

The Xilinx Controlled Impedance TEchnology (XCITE) is another example of PC board simplification and improved signal integrity. XCITE places digitally controlled termination resistors on the FPGA, so you don't have to manually terminate your signals with huge numbers of discrete external resistors. This not only saves you a lot of board space and cost, it makes board layout much simpler. This built-in termination adjusts itself for temperature and voltage variations as well, so your boards are not only less expensive, they are also more reliable. XCITE solves the signal integrity issues that both circuit and PCB designers are now dealing with, allowing you to run your PC boards at full speed and get them to market quickly.

Conclusion

Our FPGAs add more than just logic; they are tremendously more valuable because, they make your design simpler, they eliminate other components on your board, and they continue to decrease your development time and costs.

If you want to build the systems of the future, and keep your costs down, you need a solid foundation on which your designs can grow and evolve as technology advances. You need a logic solution that will grow with you and help you solve the problems that have yet to be encountered. You need the devices, software tools, and company support that make a complete solution. That's what you get with the Xilinx Virtex-II Platform FPGA family. It's already the industry leader, by far, and it just keeps getting better.

I hope you enjoy this Virtex-II Special Edition of our Xcell Journal.