Internet Reconfigurable Logic with Alpha Data's ADM-XRC

Here's how to create a remotely upgradeable system on a Motorola MCP750 single board computer fitted with an Alpha Data ADM-XRC card.

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It would be very advantageous if you could add new features, fix bugs, or make modifications to your existing designs, in the field, without replacing any hardware or sending a technician. That's the motivation behind the Xilinx® IRL™ (Internet Reconfigurable Logic) effort, which encompasses their PAVE (PLD API VxWorks™ Embedded) framework.

IRL and PAVE

Internet Reconfigurable Logic allows you to modify your FPGA designs after they have been deployed in the field, over any network, using well-known and standard methods of connectivity such as TCP/IP. And, unlike the flash BIOS on most PCs, IRL-based systems can automatically revert to a default known-good configuration.

For example, if you have a single board computer (SBC) with an FPGA embedded on it – it doesn't matter whether the FPGA is on a PCI Mezzanine card or coupled tightly to the CPU – you can incorporate the IRL framework into your VxWorks application. Then, when you deploy your SBC on a network, it starts listening for upgrade requests from a remote host or it sends an upgrade request when necessary. In the event of a failed upgrade, this type of IRL system can remain fully functional, because a read-only fallback configuration can be programmed into nonvolatile memory, at the factory, and used to reload a working configuration.

PAVE is a well-defined application-programming interface for loading bitstreams into FPGAs. It presents a common interface across all FPGA cards that it supports so you don't need to understand the process or figure out how to access the memory-mapped registers – the board support packages for the cards that you're using know how to do this, much like a device driver.

A Practical IRL System

A Motorola SBC750 SBC and an Alpha Data ADM-XRC can be combined to form an IRL system.

The MCP750 SBC

The MCP750 is a single board computer from Motorola. The important features, as far as IRL is concerned, are:

- A small NVRAM (nonvolatile RAM)
- On-board flash memory fitted as standard
- The ability to connect EIDE CompactFlash cards.

The ADM-XRC

The ADM-XRC is a PCI Mezzanine card with a Virtex™, Virtex-E, or Virtex-II FPGA and some local memory. A fast PCI interface is provided, capable of a real throughput of about 100 Mbps along with a flash memory for storing FPGA configurations.

The IRL System

As shown in Figure 1, we use the on-board flash memory (1) of the MCP750 to hold default known good images for the VxWorks kernel and VxWorks application. These images are written at the factory and never overwritten during the lifetime of the system in the field. Also contained in this flash memory is a bootloader, described below.

We use the flash memory (2) on the ADM-XRC to hold the default known good bitstream for the Virtex-II FPGA. This bitstream is written at the factory and is never overwritten during the lifetime of the system. On power-up, the default bitstream is automatically loaded into the FPGA.

- We put the upgradeable images of the VxWorks kernel, the VxWorks application, and the FPGA bitstream into the flash card (3). This has the benefit of making manual upgrades easy.

In summary, we use the flash memories as follows:

MCP750 on-board flash (1)	Flash on ADM-XRC (2)	EIDE flash card (3)
• Boot loader • Default VxWorks kernel • Default VxWorks application	• Default FPGA bitstream	• Upgradeable VxWorks kernel • Upgradeable VxWorks application • Upgradeable FPGA bitstream

Table 1. Flash memory usage

The Boot Loader

An important firmware component is the boot loader that resides in the on-board flash memory of the MCP750 (see Table 1, column 1). The boot loader's job is to decide whether to use the default or the upgradeable configuration. It makes several checks to decide this, including:

- Are the checksums of the upgradeable components valid/correct?
- Is the "clean shutdown" flag in the NVRAM of the MCP750 set to TRUE?

If these checks fail, the boot loader selects the default configuration.

The Upgrade Process

When we want to upgrade the system, we typically establish a TCP/IP session (for example, TFTP) with the target system to download new images and bitstreams for the components listed in column 3 of Table 1.

At the end of a successful download, the target system marks the upgraded components as valid. We then issue a reset command to reboot the system with the new software.

Conclusion

Using IRL, PAVE, and Xilinx FPGAs, it's easy to create a system with upgradeable hardware that is guaranteed to work reliably. For more information on this application, go to: *www.alphadata.co.uk*

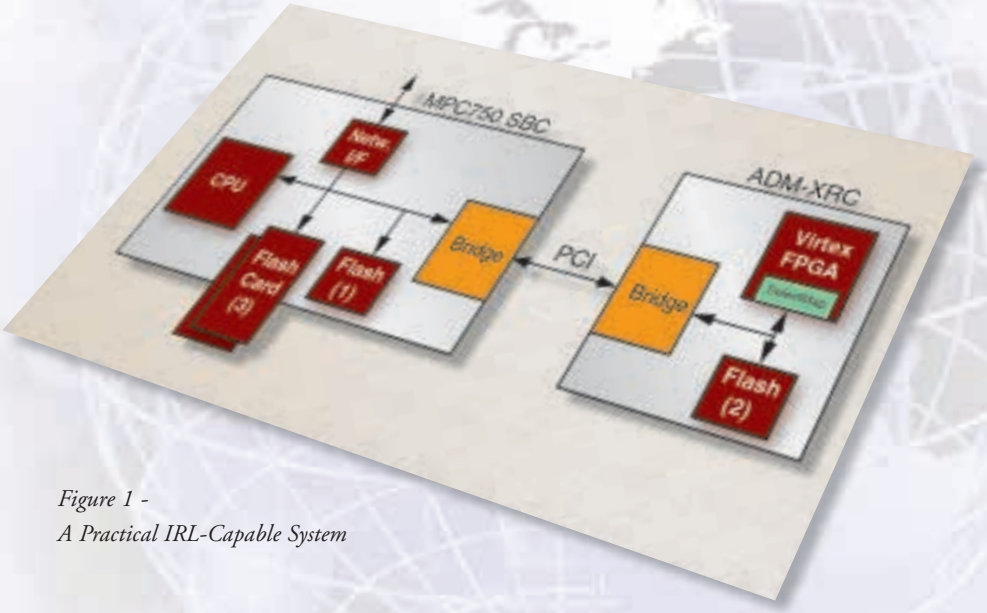

Figure 1 - A Practical IRL-Capable System