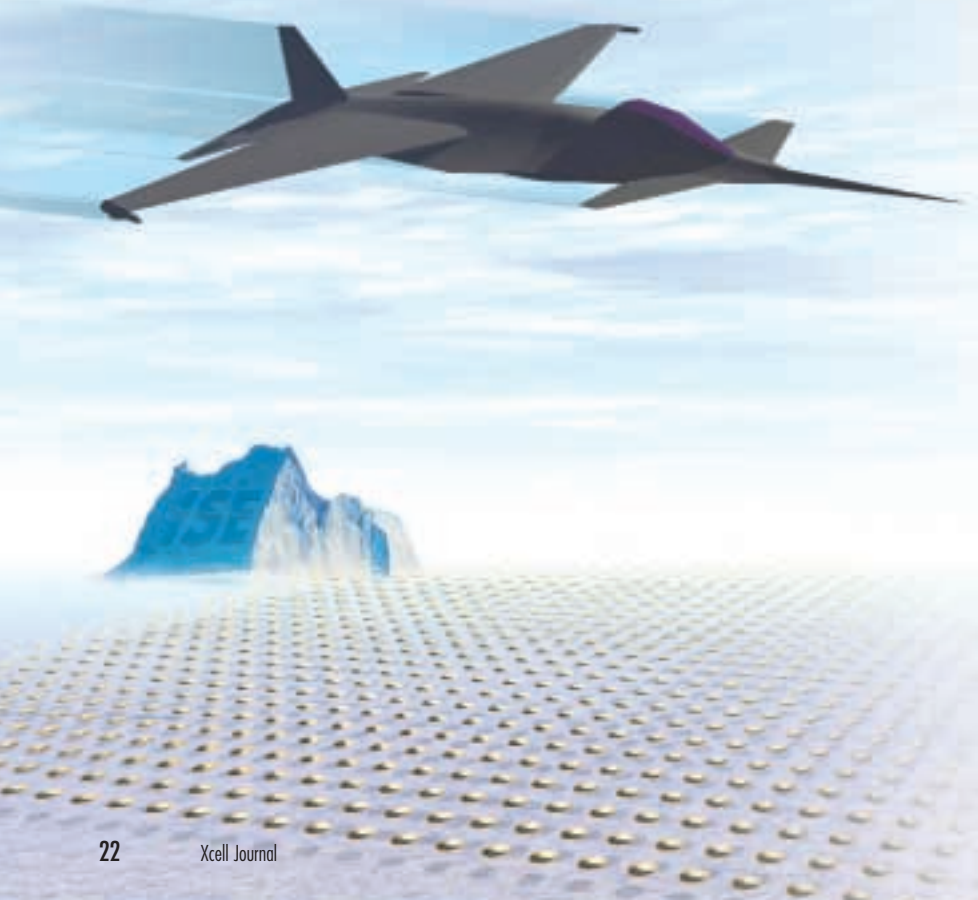
Finish Faster with ISE 5.1i Architecture Wizards

The latest release of ISE 5.1i allows you to complete Virtex-II Pro designs faster with Architecture Wizards for multigigabit I/O configurations and complex clocking schemes.



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Flexibility and performance are just two of the many reasons why engineers today are choosing Xilinx Platform FPGAs more than any other logic devices. Now, Xilinx ISE (Integrated Software Environment) 5.1i logic design tools, and new Architecture Wizards, make it easy to take advantage of such advanced functionality as programmable RocketIO™ interfaces and advanced digital clock management. These features enable high clock speeds within the chip, and high bandwidth when communicating between chips and across high-speed backplanes.

Flexibility by Design

The Xilinx Virtex-II Pro™ platform for programmable systems can be used to enhance your design's performance, both internal and external to the chip. Today's multiclock systems with internal clock rates exceeding 300 MHz will benefit from the added functionality of the Xilinx Digital Clock Manager (DCM). With DCM, you can synthesize a number of low-skew clock signals and customize almost every aspect of the clock's behavior with such features as:

- **Frequency synthesis** – supports user-programmable clock multiplication and division, with several options
- **Phase shifting** – configurable for both coarse and fine-grained shifting with dynamic phase shift control
- **Clock de-skew** – both on-chip and off-chip with user-designated clock references.

Based on your application, you might use multiple configurations – and even combinations of DCMs – in your design. With these complex clock management capabilities, you can create higher performance designs than ever before.

Xilinx Virtex-II Pro FPGAs provide as many as 24 RocketIO transceivers to support several emerging serial connectivity standards, including PCI Express, serial RapidIO™, InfiniBand™, Fibre Channel, and 10 Gigabit Ethernet XAUI. Each RocketIO transceiver delivers 622 Mbps to 3.125 Gbps baud rate – as well as channel bonding to aggregate multiple channels – thus supporting a wide range of baud rates within these standards.

In addition, the transceivers have several configurable features, such as bypassable 8B/10B encoder/decoder, scalable FPGA data path interface, programmable output voltage swing, and so on. Choose from among the 100 predefined configurations to manage the myriad I/O standards and proprietary interfaces prevalent today. In fact, by leveraging the flexibility offered by RocketIO multi-gigabit transceivers in Virtex-II Pro FPGAs, Xilinx customers have already delivered working designs incorporating new serial standards demonstrated at Programmable World 2002 and SuperComm 2002.

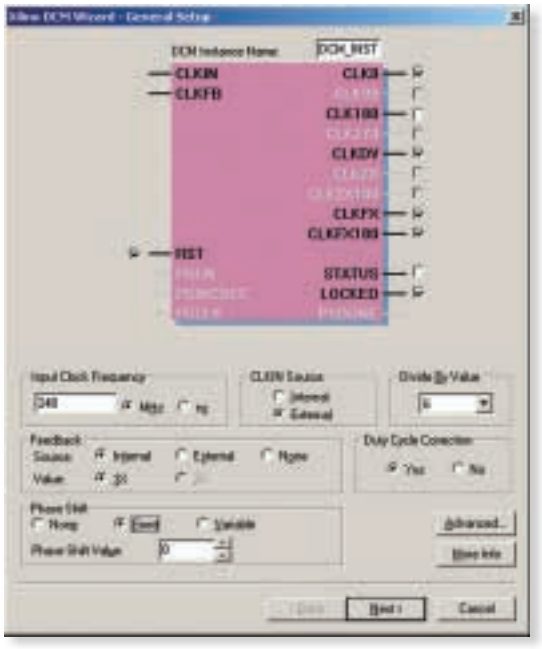

Figure 1 - Digital Clock Manager Wizard

What Design Gap?

One of the challenges plaguing design engineers over the years has been the "design gap" – that gap between the capabilities available in leading-edge ICs and a design team's ability to take advantage of them. For example, even though Xilinx customers don't have to deal with the complexity of physical design in ASICs, the immense flexibility of such advanced features as DCM and RocketIO blocks can make it difficult to use their capabilities fully – introducing a programmable logic design gap.

Xilinx Platform FPGAs have always put you on a design platform closer to your goals. We keep the design gap to a minimum – and give you a jump-start on developing leading-edge systems – by making it easy to use device features. Continuing in this tradition, ISE 5.1i offers new Architecture Wizards that enable you to configure and harness the full capabilities of the advanced features in Virtex-II Pro FPGAs.

The Architecture Wizards

You don't have to be a rocket scientist to design with RocketIO and DCM. Driven by an intuitive graphical user interface (GUI), one Architecture Wizard walks you through the process of customizing the RocketIO or DCM capabilities and generating HDL. The Architecture Wizard ensures that it's done right the first time, and that your design will interface with all leading HDL synthesis and simulation tools from Xilinx and our partners.

Figure 1 illustrates some of the clock management capabilities provided by the DCM Wizard, and the way you can use it to define DCM inputs and outputs. A second DCM Architecture Wizard provides control over the definition of the generated clock.

Figure 2 depicts the general setup dialog box of the RocketIO Wizard. You can see that the GUI makes it easy to define the transceiver's configuration. Additional dialog boxes are used to define advanced configuration features, such as channel bonding.

Figure 2 - RocketIO Wizard

The Architecture Wizards are tightly integrated with ISE's Project Navigator, and they are also available for standalone operations. From within the Project Navigator, Architecture Wizards are initiated by adding new source code to your ISE project. To operate it as a standalone, simply type the command line arwz, and the intuitive GUI makes it easy to define the appropriate parameters for your application.

Conclusion

ISE's 5.1i Architecture Wizards enable you to take advantage of the programmable logic industry's most advanced features quickly and easily. The ISE Architecture Wizards help you finish faster by automating the creation of synthesizable HDL – helping you to build world-class designs that include multi-gigabit transceivers and advanced clocking schemes. Go to *www.xilinx.com/xcell_ise/* to find out more about the latest and greatest features of ISE 5.1i.