New ChipScope Pro Integrated Bus Analyzer

Powerful Debugging Tools for Virtex-II Pro FPGAs

Debugging bus transactions is now faster and easier than ever before.

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Debugging complex system-level Virtex-II Pro™ designs can be quite a challenge. These FPGAs contain many advanced features, including PowerPC™ processors and RocketIO™ multi-gigabit serial transceivers – all the signals you need to verify are inside the device and inaccessible to the usual logic analyzers. However, now there is an elegant way to trace any internal Virtex-II Pro signal; it's called the ChipScope™ Pro Analyzer.

Two years after defining on-chip debugging, the ChipScope engineers have created the latest solution called IBA (Integrated Bus Analyzer). Using this new core, you now have point access to the bus transactions that occur in the IBM CoreConnect™ structure – this is the critical interface between processor peripheral logic cores and the processor itself. Because the CoreConnect bus is implemented in programmable logic, ChipScope Pro cores have access to every available signal. Add to this complete knowledge of the IBM CoreConnect standard definition, and you have a powerful ally in your quest to debug and verify your next FPGA design.

Point Access to System Busses

ChipScope Pro cores support true system-level debugging that includes bus-level monitoring and debug capabilities. The 5.1i release of ChipScope Pro tool includes the first of several new IBA cores designed specifically for the IBM CoreConnect Bus Architecture. The first core available has

been predefined and built specifically for the On-chip Peripheral Bus (OPB) and is based on the IBM CoreConnect standards specification. The OPB bus is designed to alleviate congestion and system performance bottlenecks on the Processor Local Bus. Many common peripherals such as UARTS, GPIO, system timers, and other devices will use the OPB to interface to PowerPC or MicroBlaze™ processors.

The ChipScope Pro IBA core provides point access to each of the 32-bit address and data buses as well as control signals associated with the OPB, allowing you to view individual transactions. In addition, ChipScope Pro tools provide OPB protocol error violation detection, capable of detecting and reporting any of the 79 different OPB protocol violations that can occur.

CoreConnect IBA Core Features

ChipScope CoreConnect IBA cores are optimized for the Virtex-II series fabric and include the following features and capabilities:

- **Fast** – CoreConnect IBA cores are designed to operate at the CoreConnect OPB frequency
- **Small** – IBA cores use at little at 3% to 4% of available logic and memory resources in Virtex-II devices.
- **Flexible** – You can use multiple cores in a single design, and place multiple IBA cores to access processor OPB busses associated with PowerPC and or MicroBlaze processors.

ChipScope Pro Analyzer

ChipScope Pro 5.1i features a completely redesigned project-centric user interface that not only supports the new cores available in 5.1i but also provides a convenient interface for system level debugging. The new ChipScope Pro Analyzer provides the following features and benefits:

- Project-centric interface allows you to set up and view data from multiple cores in different windows within the ChipScope Pro Analyzer.
- Advanced trigger setup dialogs support bus analysis as well as logic analysis. You can use the advanced trigger setup capabilities to define complex bus and logic trigger statements; this is ideal for debugging system busses with multiple control signals.
- A powerful listing viewer is now an alternative to the traditional waveform display, and provides the opportunity to view descriptive bus transactions in order of execution.
- Optional time-stamps in the cores allow you to display signal activity and bus transactions referenced to absolute time or by transaction number.

Figure 1 - ChipScope Pro System

- Advanced data display options in the new Analyzer will allow you to plot data-versus-time and data-versus-data; this is a valuable tool for debugging DSP applications.

Easily Add ChipScope Pro Cores to New and Existing Designs

Whether you are working with an existing design or are specifying your next project, ChipScope Pro Analyzer provides quick, easy-to-use tools that allow you define and generate the debugging cores you need.

You can generate cores using the standalone ChipScope Pro Core Generator™ tool or specify ChipScope Pro cores from within the Core Generator tools, part of the Xilinx ISE design environment. These tools will create an HDL file that you can add to the project design HDL for synthesis and implementation.

Alternatively, you can add cores to an existing design using the ChipScope Pro Core Inserter tool. This tool allows you to identify existing signals and nodes within a design and generate ChipScope Pro cores. The ChipScope Pro Core Inserter tool generates the cores needed and creates a design netlist that is merged with your design netlist.

Additional functionality is provided via the FPGA editor tools available in the ISE design environment. Using the FPGA editor, you can reassign signals to existing ChipScope Pro cores without having to create new cores and with minimal impact to your design.

Complete On-Chip Debugging and Verification System

In addition to providing the latest generation CoreConnect IBA core, ChipScope Pro features a new, enhanced ILA (Integrated Logic Analysis) Pro core and the new ATC (Agilent Trace Core) developed by Agilent Technologies. Together these tools make up a complete on-chip system (see Figure 1) that supports core generation, insertion, device configuration, debugging, and verification.

Conclusion

Don't let debugging and verification get the best of your time in your next design. The new ChipScope Pro 5.1i tools are available today and can help you greatly reduce overall development time by shortening the critical debugging and verification phase of a design. Visit *www.xilinx.com/chipscopepro/* today to download a free 30-day full-featured evaluation copy of the tools.