Upgrade to Synopsys FPGA Compiler II Synthesis Tool to Maximize Virtex-II PRO Performance

FPGA Compiler II's unique algorithms aid in designing chips correctly and on time.

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When you target Virtex-II PRO™ Platform FPGA, you are using one of the best FPGAs on the market – and you need a high-performance synthesis tool to match. That's why Synopsys Inc. is focusing efforts on its premier FPGA Compiler II™ FPGA synthesis tool and continuing to hone its support for top-of-the-line programmable logic devices. In 2002, FPGA Compiler II is superceding FPGA Express™, which will be discontinued.

This article will explain the differences between the two synthesis tools, summarize key features carried forward from FPGA Express to the FPGA Compiler II, and explain how you can upgrade to FPGA Compiler II today.

FPGA Compiler II Has Unique Capabilities

FPGA Compiler II (FCII) was developed for high-performance devices such as Virtex-II PRO Platform FPGAs. FCII combines the architecture-specific synthesis engine of FPGA Express with advanced technologies suitable for ASIC-like design challenges, as shown in Figure 1. These leading-edge capabilities are unique to FPGA Compiler II and not found in any other synthesis tools on the market.

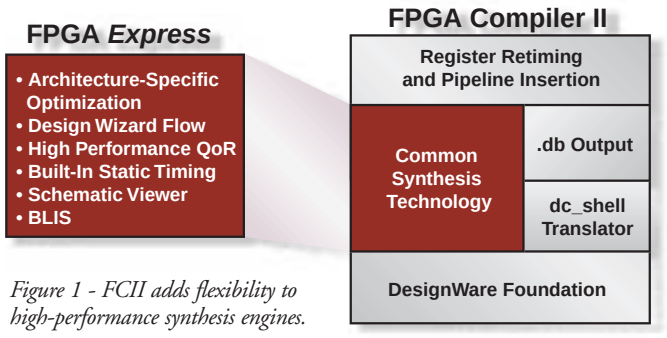

Figure 1 - FCII adds flexibility to high-performance synthesis engines.

Register Retiming

FCII uses sophisticated retiming algorithms to boost clock speed automatically. Retiming works by analyzing all the combinational logic in the design, and then selecting the optimal register placement to meet your design goals. See Figure 2.

Retiming can also pipeline your design automatically. Just code in the number of register banks to match your latency requirements, and FCII does the rest, moving the registers into the optimal position to form your pipeline.

Register retiming is easy to use in FCII. All you have to do is set the retiming variable in your script, and FCII will automatically position your registers in the optimal places to maximize clock speed.

```
current_chip my_chip
set_chip_retiming -enable
```

You can also use the FCII graphical interface to invoke retiming, if you prefer. Just select Edit->Constraints from the menu and check the retiming box in the Xilinx vendor options tab. Synopsys full-chip retiming optimizes performance of all datapath, control, and random logic in the high end of the Xilinx line – the Virtex™, Virtex-II, and Virtex-II PRO families of devices.

DesignWare Foundation IP Library

ASIC designers save design time by reusing components from the Synopsys DesignWare Foundation IP library. Although some components in the library are also useful for production FPGA designs, the biggest benefits come for those who are using a Virtex-II PRO

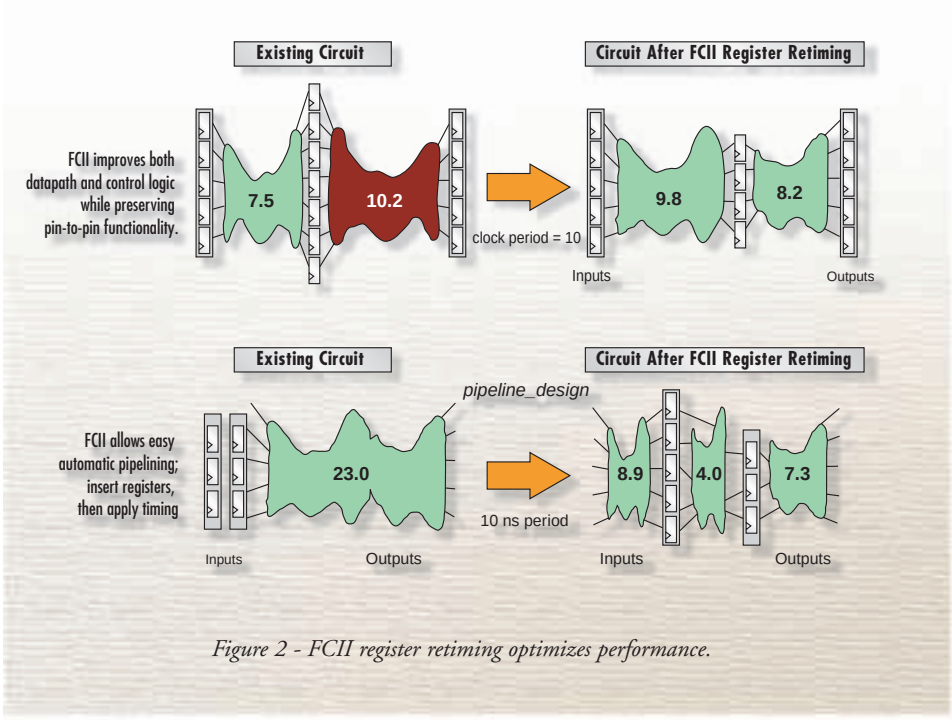

Figure 2 - FCII register retiming optimizes performance.

device to prototype an ASIC or SOC. For a prototype, FCII's ability to implement the DesignWare components in the FPGA provides confidence that the ASIC will work as planned, because it allows you to verify exactly the same IP that is used in the ASIC.

Full Flow Support

FPGA Compiler II allows designers to take advantage of other high-performance tools for FPGA design and verification. When undertaking large, complex Virtex-II PRO devices, designers need to verify the silicon before it gets into the lab. That process starts with a quick analysis of the source code using the LEDA® HDL checker. The LEDA checker leverages general-purpose rules along with Xilinx-specific rules to alert designers to potential problems and optimization opportunities in the HDL. Then the HDL functionality is verified using a fast simulator such as VCS™ for Verilog or Scirocco™ for VHDL. After the optimization by FPGA Compiler II, designers can use Formality® to formally verify the design, avoiding time-consuming simulation runs. Of course, the timing of the design is comprehensively checked through static timing analysis. In this way, Synopsys FCII customers can leverage all available means to get their designs done correctly and on time.

Architecture-Specific Synthesis Engine

FPGA Compiler II carries forward the same architecture-specific synthesis engine you've relied on in FPGA Express. This includes:

- Support for all Xilinx devices through Virtex-II PRO and beyond
- Block Level Incremental Synthesis (BLIS) to speed your design cycle time by re-doing only the blocks in the design that have changed
- User control of register duplication to eliminate critical paths caused by high fan-out nets
- Networked licenses on both UNIX and PC
- Integrated schematic viewing and timing analysis
- Full TCL scripting
- ROM inference.

Upgrading to FPGA Compiler II

FPGA Compiler II is the choice for synthesis of high-performance FPGAs such as the Virtex-II PRO pf1.

To upgrade to FPGA Compiler II, contact your Synopsys account manager or visit *www.synopsys.com/fpga*.

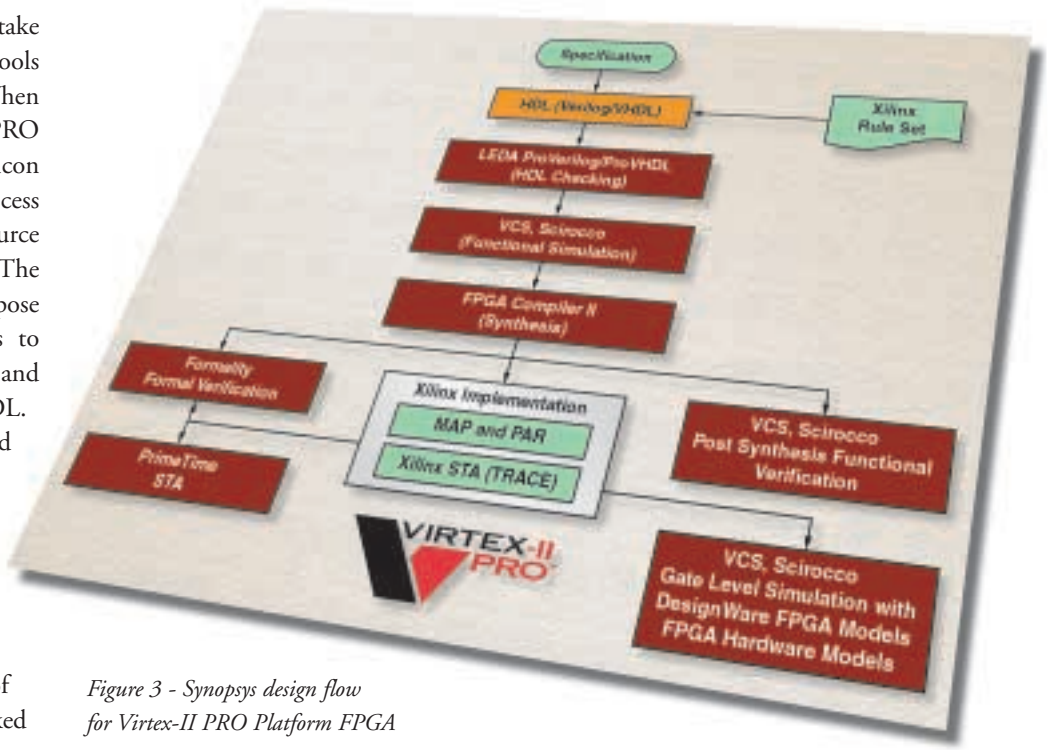

Figure 3 - Synopsys design flow for Virtex-II PRO Platform FPGA