CoolRunner-II CPLDs Go All Digital

Xilinx CoolRunner-II RealDigital CPLDs consume less power and offer reprogrammable flexibility with unprecedented design security – without a price premium.

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When Xilinx asked design engineers what they expected from the new generation of complex programmable logic devices (CPLDs), their responses showed they pretty much wanted it all:

- Advantages derived from state-of-the-art fabrication processes
- More industry standard I/O features
- System security
- Lower power operation
- Higher performance.

Designers required the next generation of CPLDs to increase performance of battery-powered devices. And, they stipulated that the next generation of CPLDs must improve performance without power penalties – and with the features and functions that would meet the expectations of today's discriminating designers and cost-conscious consumers.

In response to the high expectations of top design engineers, Xilinx has created the CoolRunner™-II RealDigital CPLD. The CoolRunner-II CPLD architecture introduces, for the first time, the advantage of both high performance and low power operation. The CoolRunner-II RealDigital CPLD reprogrammable logic solution just may be the defining element of a new era of CPLD-based applications – small form factor, high performance, power sensitive products that are feature rich and protected by multiple levels of security.

CoolRunner-II RealDigital CPLDs

Evolutions of the XPLA (extended programmable logic array) CPLD architecture have led to this ultra low power, ultra high speed, reprogrammable CMOS logic that offers significant improvements over earlier generations. (See sidebar "The Evolution of Low-Power CPLDs.") These capabilities are aiding in dramatic device size reductions and performance increases that are enhancing the look and feel of both handheld and high performance products.

The CoolRunner-II RealDigital CPLD delivers on several design fronts: low power, high performance, design flexibility, and security. Today, designers can choose high performance devices that do not require extra power for speed.

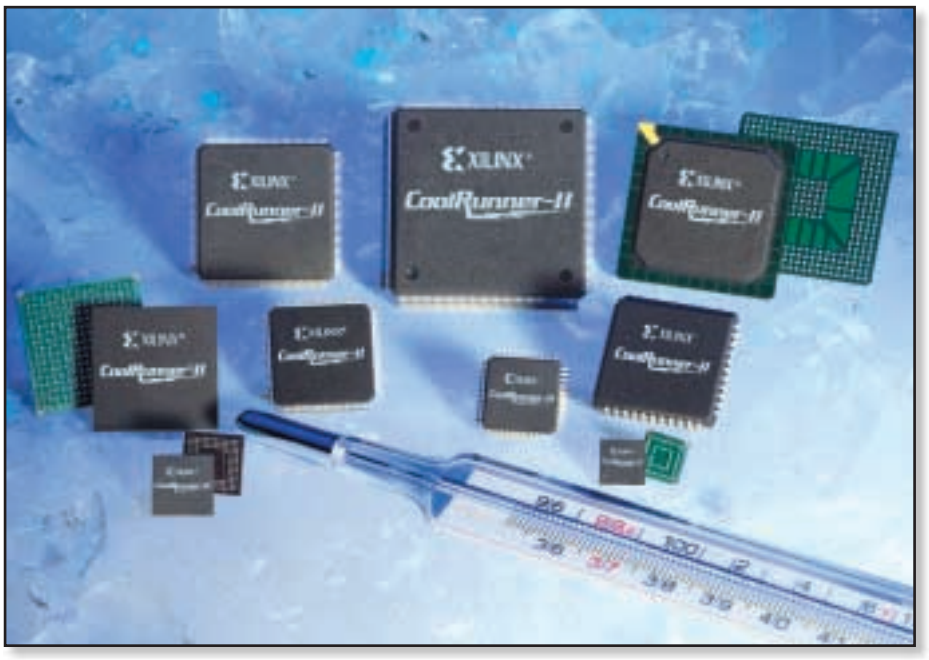

Figure 1 - Xilinx CoolRunner-II CPLD product family

Process Technology

The CoolRunner-II family of CPLDs has benefited from the leading edge of Xilinx FPGA (field programmable gate array) process technology. The original CoolRunner CPLD architecture began on a 0.5-micron process and then migrated to 0.35 micron.

Today, the CoolRunner-II CPLD family is manufactured using a 0.18-micron process technology – the same as the high-end Xilinx Virtex™-II FPGAs. With this ultra high density process technology, and scalable CMOS architecture, it is now possible to lower power consumption even further than before.

Multiple I/O Features

To facilitate its use in multiple system architectures, various input/output (I/O) standards have been incorporated in the CoolRunner-II interface. These include:

- LVTTL
- LVCMOS 33, 25, 18
- SSTL2-1, SSTL3-1
- HSTL-1
- 1.5V I/O.

High-speed transceiver logic (HSTL) I/O standards are common in high-speed memory interfaces. Stub-series terminated logic (SSTL) is associated with circuit designs where buses must be isolated from relatively large stubs. With these added I/O standards, CoolRunner-II CPLDs can easily adapt to a variety of interfaces that other low power processors might not be able to handle. This makes CoolRunner-II CPLDs a great system integration solution for microprocessor-based applications.

100% Digital Core

CoolRunner-II RealDigital CPLDs do not use traditional sense amplifier technology – and that means the historical tradeoff between speed and power has been eliminated. RealDigital technology has enabled Xilinx to offer the industry's lowest power consumption and highest performance on a single device with no price premium.

Low Power Enhancements

Learning that designers of portable products wanted even lower power than CoolRunner XPLA3 CPLDs, Xilinx added architectural features to accommodate tight power budgets. Even with FZP (Fast Zero Power™) technology and voltage reduction, we still had to add two new architectural features to lower overall power consumption in designs for power sensitive applications. Those features are DataGATE and CoolCLOCK.

DataGATE makes it possible to reduce power consumption by reducing unnecessary toggling of inputs when they are not in use. A prime example of this would be a bus interface. These input signals would become active only when information is passed to the CPLD. This eliminates the unnecessary switching from high to low/low to high. As bus interfaces grow, so will the power demand from needless switching of input signals.

CoolCLOCK, another CoolRunner-II low power enhancement, is implemented by dividing, then doubling, a clock signal. Using Global Clock 2 (GCK2) clock input and dividing by 2, then doubling the clock at the macrocell, performance can be maintained while lowering power consumption. The CoolCLOCK method is easily synthesized and is available on 128 macrocell and larger devices.

Schmitt Trigger

When communicating with CPLD design engineers, we discovered they were looking for an easy method to interface to noisy analog components. Thus, CoolRunner-II CPLDs incorporate Schmitt trigger inputs, which are helpful by delaying the switching time on slow rising or falling signals. Schmitt trigger inputs also help eliminate

false switching due to noise spikes. The possibility also exists to form a simple oscillator circuit from these inputs. You must exercise care to assure reliability, but it can save component costs on simple circuit designs.

Security

The loss of intellectual property is always a concern for electronic equipment manufacturers. With CoolRunner-II RealDigital CPLDs, security was enhanced to eliminate the possibility of code theft. The security bits are scattered and affect different modes of operation. If any tampering of the security chain is detected, the device automatically locks down and is erased. Even if the device is de-capped, buried interconnects make it almost impossible to trace security connections without destroying the device. Security details cannot be discussed even under non-disclosure agreements, thus ensuring ultimate protection.

User-Defined Grounds

As voltage levels decrease, noise and ground bounce become larger factors in signal integrity. Now, a few hundred millivolts is the difference between on and off, versus a few volts in legacy devices. We had to take extra care in design and layout to shorten signal paths and minimize potential interference.

Differential signaling (SSTL and HSTL) serves as a good method to reduce noise and increase signal integrity – with the provision that extra pins are available for differential I/O and reference voltage sources.

To simplify the elimination of noise and ground bounce, CoolRunner-II CPLDs also employ software-definable ground pins. These programmable ground pins are an ideal way to reduce noise and ground bounce effects. By using neighboring I/Os as ground pins, CoolRunner-II devices can tolerate a larger amount of potential signal noise.

Voltage Translator Clearinghouse

Due to the availability of various specialty electronic devices, it may be necessary to interface with multiple component voltage levels. With CoolRunner-II RealDigital CPLDs, I/O banking is an easy way to eliminate voltage level translators. "Banking" is the ability to separate function blocks within the CPLD so that these blocks can operate independently at different voltage levels.

For instance, one function block could be I/O compatible with 3.3V devices, and another function block could interface with 1.8V devices. This saves board space and eases voltage level design issues.

Conclusion

From process technology to a 100% digital core to added power reduction features, CoolRunner-II RealDigital devices mark the beginning of a new era for CPLD applications. Many system design concerns – including speed, power, I/O interfaces, clock management, and security – have been consolidated into one reprogrammable logic solution: CoolRunner-II RealDigital CPLDS from Xilinx.

For more information, please visit *www.xilinx.com* > *Products* > *CPLDs* > *Introducing CoolRunner-II RealDigital CPLDs*, or *www.xilinx.com/xlnx/xil_prodcat_product.jsp?title=coolrunner2_page*.

A Short History of Low Power CPLDs

The first reprogrammable logic devices have their roots in bipolar PROM (programmable read-only memory) technology, with added logic capacity and features. The first company to generate customer interest was Signetics, with their introduction of the 82S100 FPLA (field programmable logic array).

Monolithic Memories Inc. attempted to be a second source supplier to the 82S100, but failed due to a process technology mismatch. They instead developed the now famous PAL (programmable array logic). This development by MMI led to aggressive process technology shrinks and increased speeds as logic designers pushed for faster state machine operation.

Philips Semiconductors purchased Signetics, and in 1977, acquired a second source license for the PAL from MMI. Philips continued to work on different architectural enhancements and migrated to a BiCMOS (bipolar CMOS) process. When the first 22V10 PAL from AMD hit the market, it was a greater success than anyone anticipated. From this beginning, devices matured into what are now known as CPLDs. Xilinx entered the CPLD market in the early 1990s by acquiring Plus Logic and introduced the 7200 family of CPLDs.

CMOS CPLD products use power for speed improvements by partially turning on (biasing) transistors and by using sense amp technology. In the past, this was an easy way to promote devices and claim a speed advantage. The by-product, however, was heat.

In 1994, Philips Semiconductors made the move to CMOS CPLDs. With this decision, CPLDs broke away from their BiCMOS PROM roots and entered into the scalable process technology arena. These products reflected innovative approaches in circuit design with an awareness of power consumption by removing the old bipolar style sense amplifier from the circuitry.

Xilinx purchased the CoolRunner line of CPLDs from Philips Semiconductors in 1999 to penetrate the low power CPLD market segment. Today, ultra high density CMOS processes (0.18 micron) make possible reduced size and lower power consumption, which directly reduces heat dissipation.

Consumers' demands for smaller, faster, cheaper, better products are the driving forces in today's competitive markets – and the state-of-the-art CoolRunner-II RealDigital CPLDs meet these demands.