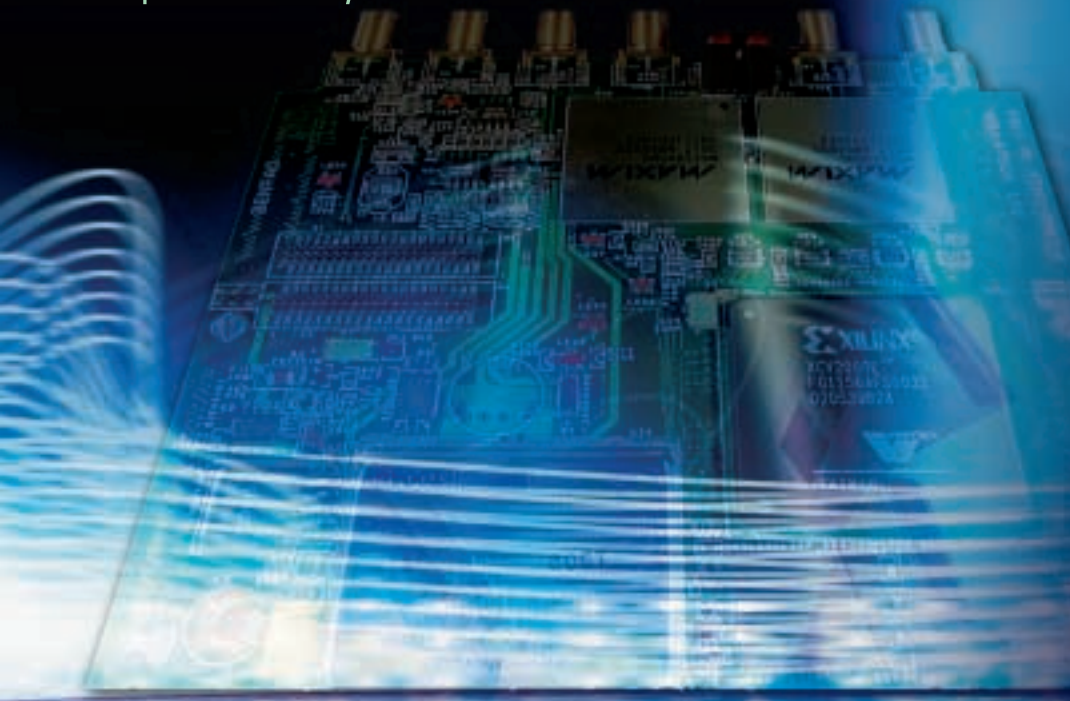
Giga-Sample DSP Board Using Virtex-E FPGAs

Central Research Laboratories Limited (CRL) uses off-the-shelf FPGAs to create a wideband RF pulse capture and analysis board.



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CRL considers Xilinx FPGA technology a key element for creating very wideband digital signal processing systems, bringing new capabilities to applications such as radar, spectral analysis, very broadband wireless communications, vibration analysis, and ultrasonics. To facilitate the development of these systems, CRL developed a high speed digitizer module in collaboration with Xilinx Xpert partner, Nallatech.

Using Virtex™-E FPGAs in conjunction with state of the art analog to digital (ADC) technology, CRL has combined the processing power conventionally associated with full custom ASICs, with data sampling rates normally associated only with fast sampling digital storage oscilloscopes. Key to the success of this program were:

- The advanced I/O capabilities of the Virtex-E FPGAs
- The System Generator tools for rapid DSP algorithm development
- The use of DIME-II™ FPGA platform from Nallatech.

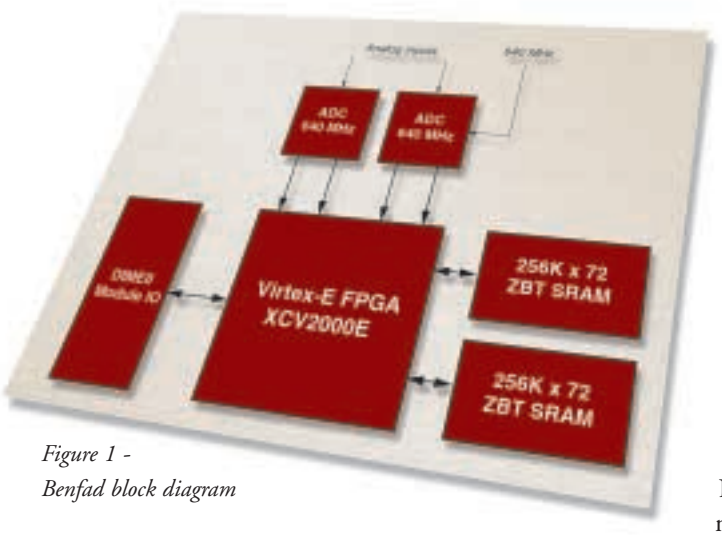

Figure 1 - Benfad block diagram

The "Benfad" DSP Module

The architecture of the CRL Benfad™ module, shown in Figure 1, relies heavily upon a number of advanced Virtex-E FPGA features. The primary advantage of these FPGAs is their support for LVPECL I/O capability. This enables the two 640 MHz ADC chips to be connected directly to the FPGA. Other key FPGA features include the 320 MHz DLLs, the high-speed on-chip RAM, and the high performance DSP capability of the extensive logic resources. These FPGA features, and the power of Nallatech's DIME-II module architecture, have resulted in the highly compact design shown in Figure 2.

Figure 2 - Benfad module

Giga-Sample DSP Algorithm Development

To get 640 MHz performance, you must broaden and slow down the data, and process it in parallel within the FPGA. However, care must be taken to use optimal DSP implementations to prevent the design from expanding and using excessive logic capacity.

Figure 3 illustrates how the data is broadened and processed using multiple parallel data paths at a practical clock rate. This design shows a broadband down converter and demodulator suitable for receiving broadband RF pulses. Two instances of this design readily fit into the 2 million-gate Virtex-E FPGA on the Benfad module, processing a total of 1.2 giga-samples per second.

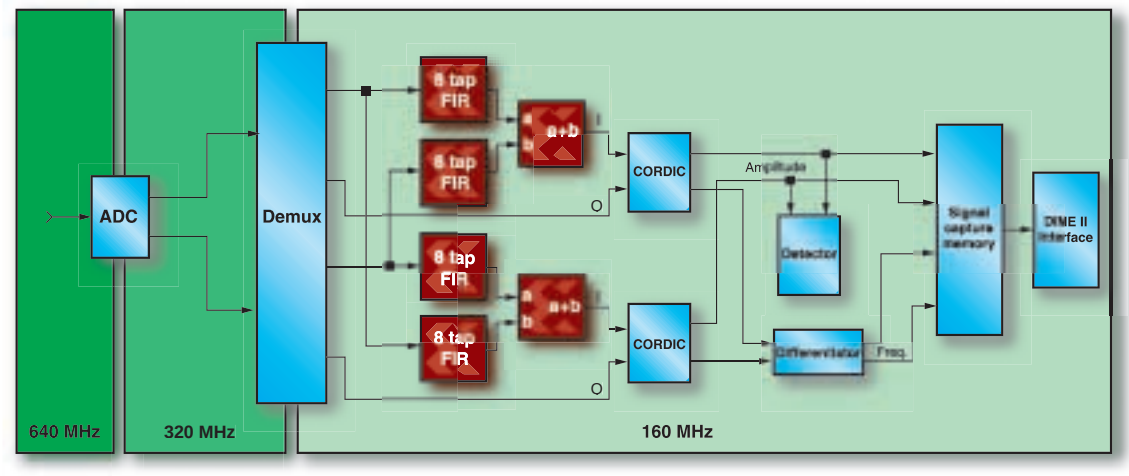

Figure 3 - Wideband down converter

Figure 4 shows how a simple chirped RF burst of 125 ns duration is processed by the system to yield its amplitude and frequency characteristics. Circuits may then be added to measure statistics of the pulse, such as time of arrival, duration, mean amplitude, and frequency. These statistics may then either be passed to the user or used as trigger events to pick out specific signals of interest in complex signal environments for further analysis.

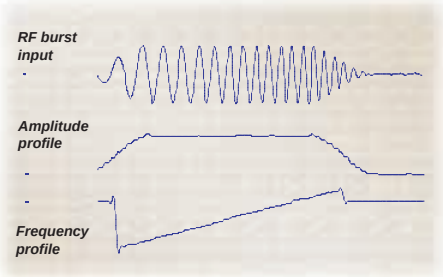

Figure 4 - RF pulse analysis

Tools such as the Mathworks' Simulink™, the Xilinx System Generator, and Nallatech's DIME environment, significantly reduce the time to design and implement such powerful DSP solutions. These tools unlock the potential of platforms such as Benfad for the real-time capture and analysis of a wide range of broadband signals.

Conclusion

Virtex-E FPGAs are a key technology for implementing sophisticated giga-sample data capture and analysis systems such as Benfad. In the future, migration to Virtex-II FPGAs will permit the ADC sample rate to be raised to 1.3 GHz, doubling the instantaneous bandwidth that can be processed. Pushing digital signal processing technology to these limits, using off-the-shelf boards, offers exciting prospects for the rapid development of new application areas.

For more information on the Benfad DSP module, e-mail CRL at: *sking@crl.co.uk,* or call +44 (0)20 8848 6452.