Design Embedded Programmable Systems Without Compromise

With the new Xilinx Embedded Design Kit, you can easily develop programmable, embedded, hardware/software solutions that deliver optimum results — and you can do it faster than ever.

by Ravi Pragasam Marketing Manager, Embedded Processor Solutions Xilinx Inc. ravi.pragasam@xilinx.com

The trouble with embedded design up to now has been that neither ASICs nor ASSPs – the traditional choices for embedded solutions – offer an ideal fit. In an ASIC flow, hardware (HW) limitation problems discovered late in the design cycle must be dealt with in the software (SW). This drawback is becoming increasingly critical now as physical geometries shrink, and as design rules and chip fabrication processes evolve.

Likewise, ASSPs are also less than perfect because you must design your solution around standard elements, which often impose limitations. In addition, the nonstandard elements of the ASSP usually don't add enough functionality to deliver a solution that sets it apart from the competition. Typically, the resulting design has too much functionality here, and not enough there.

Long design cycles involving extensive simulation, on the one hand, and narrow

market windows and changing industry standards, on the other, often necessitate compromises in performance. The result is often failure to meet original specification goals. What has been lacking is a fast, effective way to integrate HW and SW flows to produce a solution that brings out the full advantage of embedded design.

The new Xilinx Embedded Development Kit (EDK) bridges the gap between HW and SW flows by providing a single HW/SW design environment. Fusing the two early in the design flow enables you to deliver an embedded programmable system that meets your design specifications on time – without compromising performance.

A New Era of System Design

The EDK allows you to define the hardware and software platforms of your system using powerful tools based on the Platform Specification Format (PSF). PSF is an open format that provides an abstraction layer between the HW and SW sections so they can be tightly integrated during the definition and development process. This coupling ensures that the hardware platform you create will be one a software platform can match.

The EDK also enables you to rapidly match the programming environment and software capability to available hardware resources.

For the software designer, the greatest advantage afforded by PSF is access to an embedded tool that allows HW/SW codesign, and which also interfaces with industry standard software tools, such as RTOS support from Wind River Systems, Linux support from MontaVista Software, and popular open source embedded tools like GNU.

PSF Benefits

• The PSF overcomes many of the most common problems of the traditional "over-the-wall" approach to HW/SW interface definition and integration. With the PSF, you can give a hardware platform specification to a firmware or software engineer without having to wait until the hardware is available. The

O Xcell Journal Spring 2003

firmware and software developer can then configure the SW platform with full knowledge of the HW platform – with which devices are attached, memory maps, register definitions, and so on.

- Offering a single-environment approach for HW/SW platform configuration, PSF enables a rapid re-architecture of the embedded programmable systems design. This enables you to add to, or subtract from, HW resources with matching SW in the modified architecture easily.
- The unified environment, common bus structure, and common core libraries enable you to easily use a Xilinx MicroBlazeTM core, IBM PowerPCTM processor in a Virtex-II ProTM FPGA, or both, in a single design.
- Multi-core, homogeneous (multiple MicroBlaze cores or multiple PowerPC processors), or heterogeneous (mixed PowerPC and MicroBlaze cores) in a single design (multiple bus masters), are also supported.

The PSF is a one-of-a-kind specification format for both HW and SW. Because it is an open format, it is available for adoption by customers and third parties, enabling them to integrate custom peripherals, third-party IP cores, and tools. PSF provides a common tool chain for the HW/SW platform specification, generation, development, and debug, while supporting multimaster and mixed architecture designs.

The Xilinx EDK and ISE 5.1i logic design tools provide you with the technology to help you achieve your performance requirements – faster and better than ever.

EDK Contents

The EDK includes the Xilinx Platform Studio (XPS), an all-encompassing design environment that permits you to define, configure, and generate a custom hardware and matching software/programming environment for either a stand-alone or RTOS-enabled programmable system. Hardware, software, and firmware developers who need to work in both domains can use the XPS integrated design environment.

- Embedded system tools
 - Xilinx Platform Studio
 - Tools for specifying the hardware and software platforms based on PSF
 - Xilinx microprocessor debug (XMD)
 - GNU tools for MicroBlaze and hard embedded PowerPC cores in Virtex-II Pro FPGAs (compiler and debugger)
 - Support for simulation tools
 - System generator for processors (beta version)
 - Board Support Package (BSP) generator
- Interface and infrastructure IP cores
 - Arbiters
 - Memory controllers for external memory interfaces
 - More than 40 standard IP cores (such as UART, GPIO, and timer/counter)
 - Evaluation version of high-value cores (such as 10/100 EMAC, single channel HDLC controller, and serial ATA L2)
- MicroBlaze 32-bit soft processor core
- Reference designs and examples
- Evaluation versions of Wind River and ISE 5.1i software tools.

Conclusion

With key products, such as MicroBlaze 32-bit soft processor cores and Virtex-II Pro FPGAs, Xilinx offers a complete solution that resolves many of the design challenges presented by more traditional tools and technology. With the Virtex-II Pro device, Xilinx has ushered in a new era of system design in which SW/HW flows blend to take advantage of programmability and high-performance features — such as the multi-gigabit serial transceivers available in the silicon — in a way that enables solution providers to get ahead in their markets without making performance compromises.

Working within a common HW/SW tool environment, you can rapidly construct a custom processor system consisting of processor, peripheral cores, and interconnect bus in a Xilinx FPGA. You can also integrate your own custom IP cores into the processor system.

And now, with the EDK, Xilinx has enabled the process of HW/SW co-design that has long been a dream of embedded system designers everywhere. The EDK (Part No. DO-EDK) is available now. For more information and updates to the EDK, visit www.xilinx.com/edk/.

For more information about Xilinx embedded processor solutions, visit Processor Central at www.xilinx.com/processor/.



Spring 2003 Xcell Journal $oldsymbol{00}$