*Flex*Bench Tool Suite Relies on Xilinx Silicon and Software

Improve your time to market with rapid prototyping and system verification enabled by Virtex-II FPGAs and ChipScope Integrated Logic Analyzer.

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System verification is the major bottleneck in the development of contemporary and future system-on-a-chip (SoC) designs. Increasing numbers of applications that process large quantities of data in real time (such as telecom and video) require verification techniques that run at or near real-time speeds. Delaying your software development until working devices are available is not a viable option in the face of enormous competitive time-to-market pressures.

Thus, early hardware/software (HW/SW) co-verification is not just practical – it's essential. At Italtel SpA, we and our partners have developed a superior method of improving system verification confidence through high-speed register transfer level (RTL) prototyping and the Virtex™ family of FPGAs.

Prototyping at Real Time Speeds

RTL prototyping allows you to run system hardware and software at speeds high enough to hunt and find hidden bugs. Just as important, you can confidently evaluate subjective characteristics, such as audio and video quality.

RTL prototyping uses off-the-shelf FPGAs to implement SoC custom logic, as well as test physical, real devices like memories, interfaces, and processors that comprise the other parts of the system to be verified. This strategy enables us to create, in effect, a clone of the SoC and all the parts of system that it interfaces with. We call this

assembling a "demonstrator." With a demonstrator, we can map the hardware and run the application software. RTL prototyping can be roughly divided in two types, custom and modular:

- Custom prototyping is the fastest technique, in terms of frequency. FPGAs and other devices are assembled on a board expressly designed for the demonstrator to be verified. Such a demonstrator may reach speeds as high as 200 MHz – but it requires several months from initial system design to the end of the verification process because of the intrinsic delay of the board fabrication process.
- Modular prototyping is not quite as fast as custom prototyping for verification – but when it comes to giving you the time-to-market advantage, it is, by far, the better solution. With modular prototyping, you can assemble FPGAs and other devices on general-purpose daughterboards that allow you to create a wide range of different demonstrators. Modular prototyping is a HW/SW co-development scheme based on a set of configurable carrier boards where daughterboards can be inserted and interconnected as necessary during the co-design process.

Avoiding the FPIC Dead End

Modular RTL prototyping platforms have intrinsic speed limitations related to modularity, accessibility, and routability. Field programmable interconnect chips (FPICs) have been the traditional solution for routability problems. Unfortunately, the existing technology trends for FPICs are insignificant (in terms of speed and the number of I/Os) compared to the skyrocketing speed and size of Virtex-II and Virtex-II PRO™ FPGAs. In short, no modular rapid prototyping platform based on FPIC technology can meet your customers' need for speed and time to market.

To approach real-time system speeds, a modular rapid prototyping tool with new interconnection technologies and a novel topology had to be developed. Such a tool – with single-ended, point-to-point signals – would have a physical speed limit ranging from 80 MHz to 100 MHz.

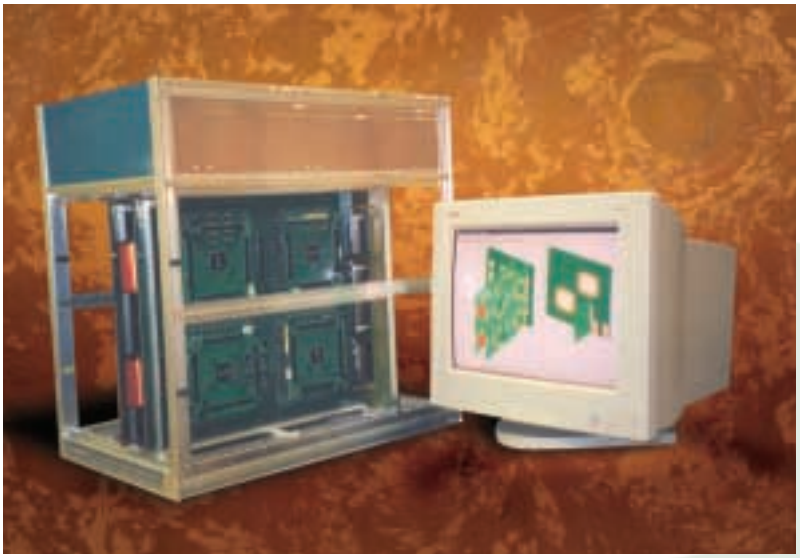

Figure 1 - Co-verification solution: Italtel FlexBench hardware with Temento Diaflex software

Given these parameters, three European companies collaborated for two years to design and develop the *Flex*Bench™ modular rapid prototyping tool suite:

- Italtel SpA, the largest Italian telecom manufacturer, is the leader for hardware development.
- Mistel SpA, another Italian telecom manufacturer, supports the hardware effort.
- Temento Systems, based in France, is dedicating its electronic test automation (ETA) software resources to the testing of SoCs and electronic boards.

Moreover, Oktet Ltd., a design service company based in St. Petersburg, Russia, was also deeply involved in the development the *Flex*Bench verification system.

Putting Together *Flex*Bench Hardware

As the *Flex*Bench project leader, I had been searching for a practical means of modular rapid prototyping in a HW/SW co-design environment. In 1999, two new technologies emerged that enabled our team to create and patent the *Flex*Bench concept:

1. QuickSwitch™ bus switches from Integrated Device Technology (IDT), Inc.
2. Mictor™ high-speed connectors from Tyco Electronics.

These two technological innovations gave our team the means of reconfiguring multiple printed circuit boards (PCBs) as needed during the HW/SW co-design process. Employing the reliable and fast-growing Xilinx FPGA technology, we envisaged it was possible to design the unique *Flex*Bench HW/SW tool suite.

The *Flex*Bench challenge was to create a rapid prototyping tool so general in purpose as to become the industry standard. Taking such a concept and turning it into a high-powered tool, however, is quite an undertaking that requires strategic alliances and adequate funding.

We applied for – and received – start-up funding from the European Commission. With that funding, we worked in a frenetic manner for two years to gather the expertise and to execute the rapid prototyping tool we envisioned.

At the hardware level, the *Flex*Bench rapid prototyping platform was to be basically a set of complex board designs. Fortunately, we had the PCB know-how and related resources in-house at Italtel – and valuable contributions from Mistel.

On the software side, the development of the computer assisted engineering (CAE) software we needed was not our area of competency. Therefore, we entered into a partnership with Temento Systems, a company known for its excellent ETA software. Temento developed the DiaFlex™ software tool we needed to monitor the *Flex*Bench system in action. See Figure 1.

Our acquisition of Certify™ RTL partitioning software from industry-leading Synplicity™ Inc. completed our primary software tool set.

Now that we had the boards and the software, we had to find the best programmable logic devices. It was a short search. In a class by themselves, Virtex-II Platform FPGAs from Xilinx perfectly fit the needs of our verification engineers: high speed, fast and simple compilation, and high capacity.

You can see the *Flex*Bench design chain in Figure 2.

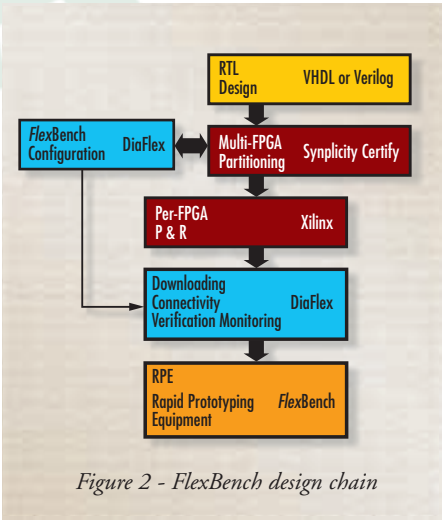

Figure 2 - FlexBench design chain

*Flex*Bench Rapid Prototyping at 100 MHz

As we said earlier, to achieve the speed edge in RTL prototyping with a modular tool, the FPIC approach is simply not suitable. A novel technology had to be introduced, based on the speed of IDT's QuickSwitch bus switches. By using pass-transistors, you can select interconnections among neighboring HW modules on multipurpose panels.

We built QuickSwitch bus switches and receptacles into the *Flex*Bench motherboards, which are populated by daughterboards named FlexPlugs. These modules are based on an open standard form factor. Using advanced, off-the-shelf interconnect technology, FlexPlug modules make available up to 888 functional signals. FlexPlugs host active devices, such as the leading edge Virtex-II 6000 Platform FPGA. The FlexPlugs also host power converters. Memories are allocated on small modules, named MiniPlugs, directly inserted into FlexPlugs in order to minimize interconnect delays.

We obtained the *Flex*Bench speed characteristics by interconnecting different FlexPlug modules through the distributed network of pass-transistors. Each side of a FlexPlug contacts the side of the nearest other FlexPlugs by means of channels. Channel size is configurable, through the JTAG port, from 0 to 222 functional wires with 8-bit granularity. Trace length minimization is achieved through a clever three-dimensional architecture.

The relatively short trace length of QuickSwitch delays (0.1 nanosecond) and the best-in-class set-up and clock-to-output parameters of Virtex-II FPGAs permits us to achieve 100 MHz clock speed (and over) on modular systems populated by up to 18 FPGAs.

The *Flex*Bench rapid prototyping equipment (RPE) is composed of a rack, a backplane (FlexPanel), a software-controlled clock generator (FlexClock), some carrier boards (FlexMothers), and several modules (FlexPlugs and MiniPlugs). FlexMother boards are connected through flexible printed circuits (FlexCable) and through the FlexPanel. See Figure 3 to see how the whole Flex hardware family interacts to form the *Flex*Bench verification system. Figure 4 shows a populated FlexMother.

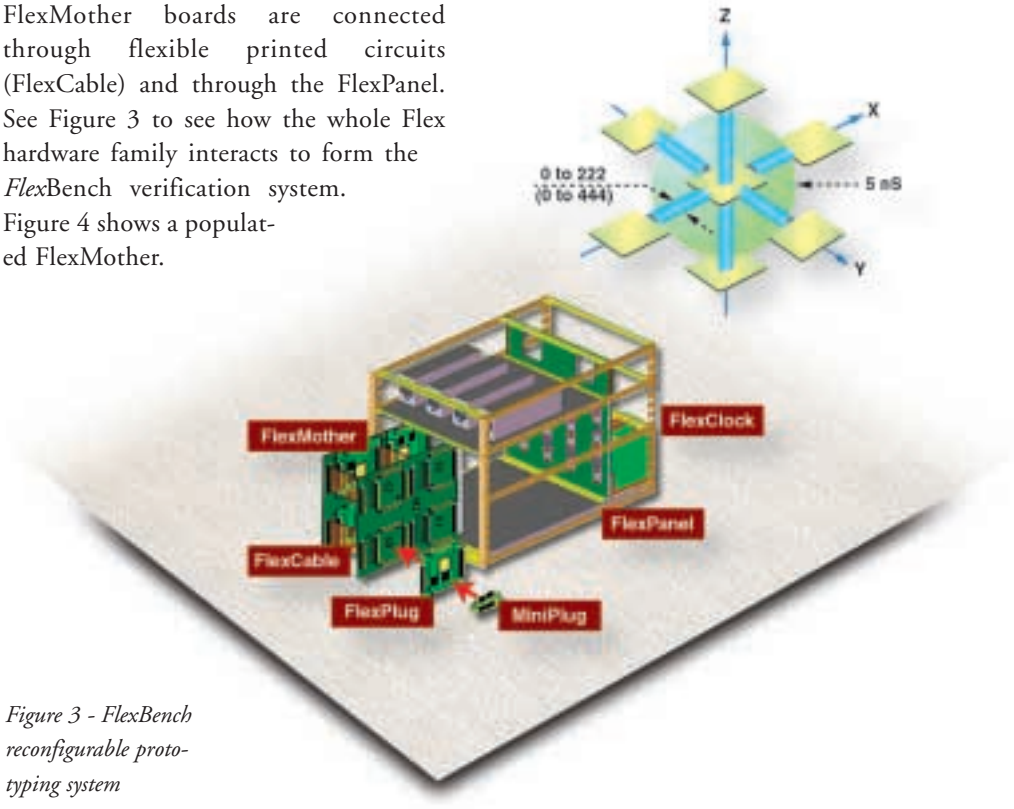

Figure 3 - FlexBench reconfigurable prototyping system

Integrating DiaFlex Software

Complementing the *Flex*Bench hardware is the DiaFlex software tool developed by Temento Systems. Dedicated to configuring, downloading, verifying, and controlling the *Flex*Bench RPE, the DiaFlex program suite allows you to design the RPE configuration through an intuitive, three-dimensional graphical user interface. Starting from RPE configuration, the DiaFlex application generates a flattened description of the platform definition into a Verilog format, called a VB

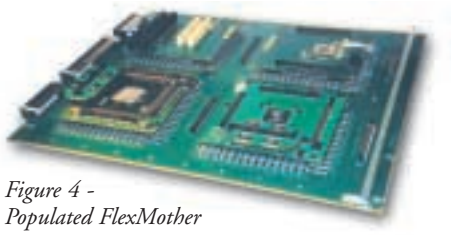

Figure 4 - Populated FlexMother

file. The VB file provides the Certify verification software with an easy view of the RPE resources and connectivity. Moreover, it provides direct channel configuration bitstreams .

The Certify program compiles RTL code, and spreads it according to the VB file description of the RPE. The Certify tool also

synthesizes all FPGAs. The FPGAs are then placed-and-routed via proprietary tools to produce FPGA configuration bitstreams.

The DiaFlex application downloads all bitstreams to the RPE and provides interactive debugging through a TemTag™ JTAG PCI board. Moreover, the DiaFlex software provides diagnostics, reports errors, and analyzes test results. This allows debugging at the signal name level, functional testing, and automatic management of IEEE 1149.1 test bench generation. Additionally, the DiaFlex program takes complete control of the FlexClock board. This enables you to configure FlexClock parameters: the frequency of clock synthesizers, the selection of global clock sources, and the control of other timing functions.

A Flexible Prototyping Library

To perform effective rapid prototyping, you must have a set of FlexPlugs and MiniPlugs. These plugs enable you to interconnect state-of-the-art FPGAs, memories, I/Os, processors, design platforms, and other components of your design.

While Italtel and our affiliates have designed general-purpose *Flex*Bench modules, design-specific modules must developed by final OEM customer. This is where the services of a company like Oktet Systems can become essential.

Sixteen general-purpose modules currently comprise the *Flex*Bench library. Some of the modules are displayed in Figure 5.

A Matter of Observability

Compared with the "observability" you can get with emulators, the classic argument against rapid prototyping has been that you can't "see" what's going on inside the design, because invasive physical probing is difficult, if not impossible, to accomplish in modular equipment.

Figure 5 - FlexBench library

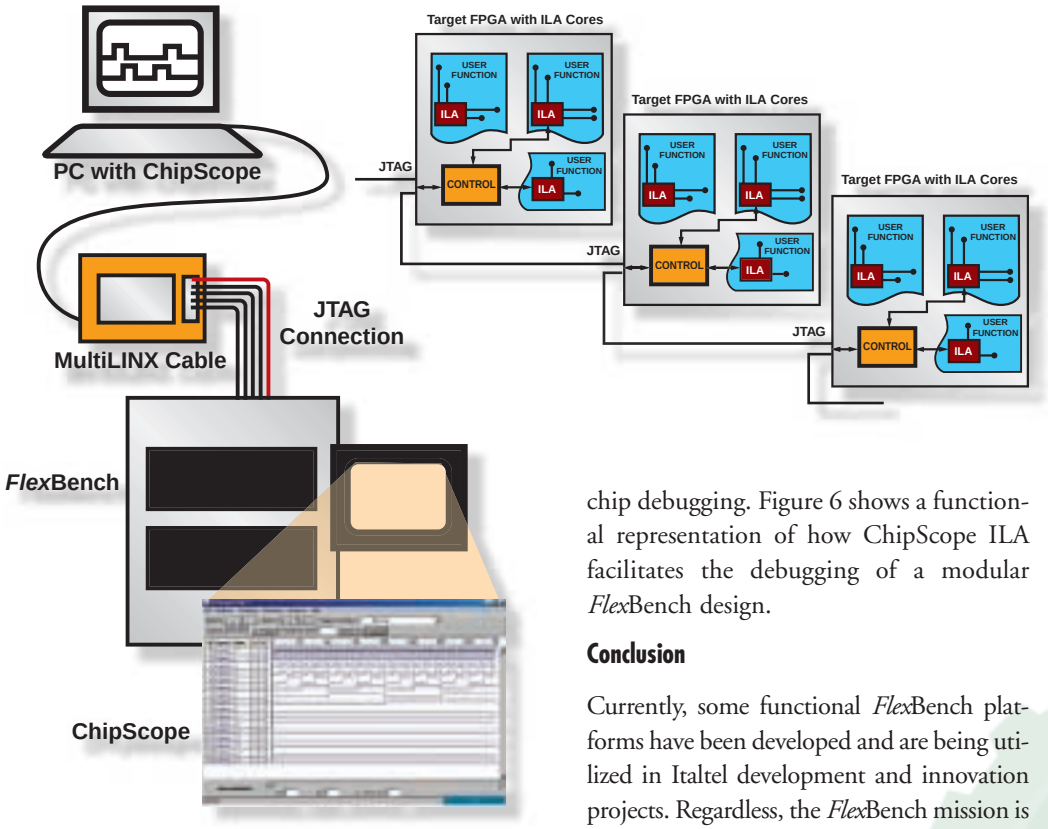

Figure 6 - ChipScope and FlexBench solution

Xilinx has removed this weakness thanks to its Integrated Logic Analysis (ILA) core, a solution that provides trigger and trace capture capability within the FPGA itself. Implemented by the Xilinx ChipScope™ Analyzer, the ILA core allows real-time access to any node in the *Flex*Bench chips. An easy-to-use graphical user interface provides the same functional controls of a sophisticated logic analyzer. With ChipScope ILA, you spend less time verifying chip functionality, and therefore, speed up your time to market.

By means of the ChipScope ILA, you get full visibility into the *Flex*Bench RPE. ChipScope ILA lets you see every selected node in every FPGA used in your design. This virtually eliminates the need for invasive physical probing of the *Flex*Bench RPE. With the Xilinx ChipScope ILA solution, you can perform real-time, on-chip debugging. Figure 6 shows a functional representation of how ChipScope ILA facilitates the debugging of a modular *Flex*Bench design.

Conclusion

Currently, some functional *Flex*Bench platforms have been developed and are being utilized in Italtel development and innovation projects. Regardless, the *Flex*Bench mission is not to become a proprietary tool, but to become an industrial standard.

Italtel/Temento are and will be engaged in trials with major silicon vendors to demonstrate and to prove the *Flex*Bench technology. We believe the versatile *Flex*Bench model is a major step in rapid prototyping and system verification. We are proud to have designed it. To ensure best diffusion of this tool, we are now researching the best sales channel.