Add Internet Connectivity with Spartan-II FPGAs and the UDP Stack Core

Insight's new VoIP Development Kit demonstrates the UDP stack core for Internet-based, point-to-point data applications.

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In the past, if you needed to connect your application to a LAN or the Internet, you were forced to design-in additional circuits, which added complexity and increased cost. Often, these off-the-shelf networking solutions provided more functionality than you needed, and their cost was often a problem. The requirement for simple data transmission from one point to another via the Internet was further complicated by the need for processors and protocol stack software. Now however, the inherent advantages of programmable logic and the advanced architectural features of the Spartan™-II family have resulted in Internet connectivity inside a single chip.

The VoIP Development Kit

User Datagram Protocol (UDP)

Analysis of the OSI (Open Systems Interconnection) Seven Layer Model (application, presentation, session, transport, network, data link, and physical layers) resulted in the identification and implementation of an optimized set of protocols and processes. Nonessential functions were eliminated and exhaustive protocol options were streamlined. The resulting User Datagram Protocol (UDP) stack core was created, providing simple point-to-point communication and data streaming over a LAN or Internet connection. Figure 1 shows an example of the basic networking applications possible.

Building on the UDP stack core, Insight created a VoIP (Voice over Internet Protocol) Development Kit that demonstrates the UDP core in a simple voice over IP (Internet Protocol) application. Targeting the Spartan-II family, the VoIP application illustrates how basic networking capabilities can be cost effectively integrated into FPGA solutions. In addition to VoIP audio data, other data formats such as digital video or sensor data can also be implemented with minor modification.

VoIP Application Kit

The Insight VoIP Development Kit was created as an evaluation platform for the UDP stack core and the networking applications it targets. The kit provides two, identical Spartan-II based demonstration boards, so you can experiment with point-to-point communications over a LAN connection. And, the kit includes everything required to be up and running in minutes.

The VoIP demonstration board is based on the 150K gate Spartan-II FPGA. Figure 2 shows the block diagram of the board. On the application side, the FPGA interfaces to the Silicon Labs CODEC (COder/DECoder) device to receive and transmit digital voice data to and from the connected headset. On the network side, the FPGA connects to the LSI 10/100 Ethernet PHY. The other functions on the board include an XC18V01 ISP PROM to store FPGA configuration data, a JTAG port, a 50 MHz oscillator, an RS-232 port, two FPGA I/O expansion connectors, on-board power regulation for 2.5V and 3.3V, a serial EEPROM, a serial number ID chip, eight user-definable DIP switches, and a user LED.

The VoIP kit also includes a single project license for the UDP stack core. Although the UDP stack core comes as a netlist only, source code for the VoIP function is provided and allows for customization at the application level.

How It Works

The VoIP application uses the UDP/IP process to transmit voice data packets over the Internet. The CODEC device digitizes the analog voice signal from the headset, groups the data into packets, and then transmits it across the network. The packets are routed through the network as specified by the packet headers and undergo the reverse process at the receiving end. The UDP stack core plays a key role in this processing. Both the UDP core and the VoIP application are implemented in Xilinx Spartan-II FPGAs. The FPGAs provide the necessary functions in optimized hardware,

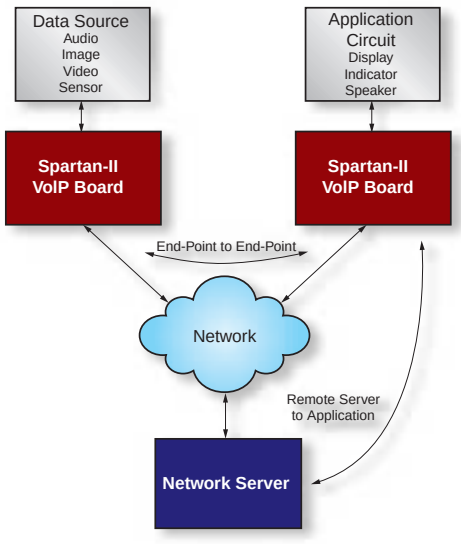

Figure 1 - UDP Stack Core Applications

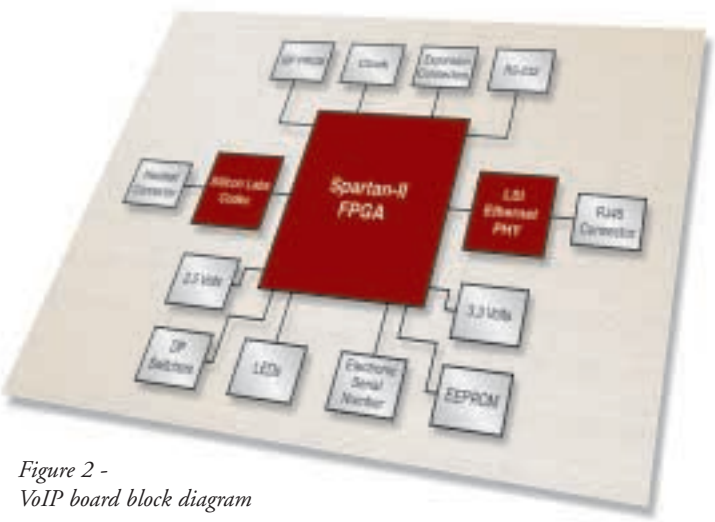

Figure 2 - VoIP board block diagram

making software unnecessary. The entire VoIP application and UDP stack consume less than 1,230 slices and six block RAMs.

Figure 3 shows the protocol layers implemented in the VoIP example. The application layer includes a serial interface to the CODEC chip, along with independent transmit and receive FIFOs for buffering data between the application layer and transport layer. The transport layer uses the Real-time Transport Protocol (RTP) to assemble/disassemble the audio payload and interface to the UDP.

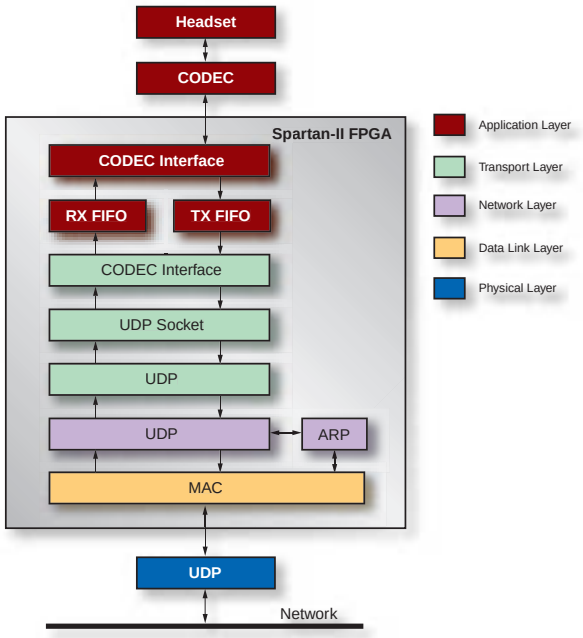

Figure 3 - VoIP protocol layers

The UDP Stack Core

The Xilinx XCoNet team developed the UDP stack core with MemecCore, the IP division of Insight Electronics. Unlike the more familiar TCP/IP stack, the UDP/IP stack is streamlined for simple point-to-point network connections and data streaming. As Figure 3 shows, the UDP stack spans the transport, network, and data link layers and includes the UDP, IP, and MAC (Media Access Control) functions.

The MAC implements the RFC894 Ethernet standard and manages the interface between the LSI physical interface chip and the UDP stack. Following the MAC is the IP function, which validates datagrams on the receive side and combines IP headers with UDP packets on the transmit side. If received data packets do not have valid source or destination IP addresses, the IP simply drops the packets. The included Address Resolution Protocol (ARP) translates the IP addresses to hardware addresses and responds to remote node ARP requests.

The UDP makes up the transport layer and has a receive section and a transmit section. On the receive side, the UDP checks for a valid destination port number and checksum, discarding packets that do not pass the criteria. For transmission, the UDP prepares the UDP header and combines it with the payload, writing the UDP packet to a buffer to wait for transmission.

The UDP stack core requires 1,000 slices, six block RAMs, and 166 I/Os. The majority of the I/Os reside on the design backend and are eliminated once the top-level application is integrated. In the case of the VoIP application, the total I/Os were reduced from 166 to just 28.

Conclusion

The VoIP Development Kit and the UDP stack core demonstrate cost effective networking solutions in a single chip FPGA. Both the UDP stack core and the VoIP reference kit are available from Insight Electronics. The VoIP reference kit is priced at $995 and includes a single project license for the UDP netlist core; the UDP stack core can be purchased separately for only $695. Both are available now.

Some applications that utilize the UDP stack may require UDP core customization. Insight Design Services can provide protocol enhancements or core modifications as needed. Call 888-488-4133 ext. 227 or go to *www.insight-electronics.com/spartan_IIVoIP* for more information or to order the VoIP kit.