Even as Designs Grow More Complex, Xilinx Software Improves Your Productivity

Xilinx Integrated Software Environment (ISE) design tools promise to manage design complexity and, at the same time, ensure your logic design flow is easy to use.

by Lee Hansen
Product Marketing Manager
Xilinx, Inc.
lee.hansen@xilinx.com

Your Xilinx programmable logic device offers you more capabilities than ever before, and coming releases of the ISE design tools will help you to handle the pressure that comes from using these complex new features. Come along for a glimpse into the future of ISE.

ISE Delivers a Wealth of Device Features

The most compelling pressure on the logic design flow comes from the added complexity of new capabilities and tool features. Embedded systems, increased clock speeds, verification of high-density designs, new device capabilities, high-speed I/O, a variety of IP (intellectual property) sources, and design reuse – all of these logic trends force more requirements into the design flow.

In 2001, the Virtex™-II FPGA introduced a revolution in clock capabilities with Digital Clock Manager (DCM), and this year, the Virtex-II Pro™ Platform FPGA broke new ground by delivering 3.125-gigabit serial I/O transceivers and embedded IBM PowerPC™ microprocessors. As the demand for more device features continues to grow, engineers must learn all the programming attributes for these new features – and the learning curve escalates with the introduction of each new device feature.

To ease the learning curve, Xilinx ISE 5.1i will offer designers even more interactive architecture and design assistance. In addition to quick and easy dialogs, wizards will automatically step you through configuring advanced device features and inserting those configurations directly into your HDL source code. Upcoming releases of ISE will soften your learning curve, helping to speed design completion.

ISE Enables IP Capture and Design Reuse

As design sizes grow, source management and methods to improve source code productivity must keep pace. In a multi-million-gate design, source code can come from multiple resources, including purchased IP, developed code, and "design reuse" – modules of HDL developed and proved in a prior design.

In upcoming releases of ISE, it will be possible to capture proven IP modules at the floorplan level. This captured IP will not be just a module of code, but it will also have attached relative placement and floorplanning area information that will help speed implementation in later uses.

As time-to-market pressures increase, design change impacts late in the design cycle will become an even larger design challenge. Enhancements to ISE will confine late-cycle design changes to only that portion of the design that is required to change. The remainder of the design will be left intact, thus speeding overall design completion. This technology is enabled by new floorplanning capabilities along HDL hierarchy boundaries that make it easier to define areas of logic.

High-Speed Design Will Push Innovation

High-speed design pressures will continue to push more innovation into logic design and into the board design flow.

Timing analysis and timing constraints have – until now – lived under two different analysis domains, separated at the FPGA pin. The logic designer has looked to the specification and timing requirements to define design closure, while the board designer has picked up the signal at the logic pin and attempted to lay out and analyze the effects that the PCB trace will have on that signal.

Now, however, the line between logic designer and board designer functions will begin to blur as timing constraint languages become more uniform across the logic tools and among the logic-level and board-level tools. Trace analysis packages also will increasingly use more complex pin models provided by the logic tools, but these complex analyses will also become much faster, dumping slower general analog simulation in favor of specialized transmission line trace simulations.

A Higher Level of Abstraction Is Coming

While high-level languages (HLLs) have been explored in logic and systems design, the pain of existing logic design methodologies hasn't been great enough to force a high-level language or associated methodology into common use.

Verilog and VHDL have served the logic design space well for the last two decades, but now logic design sizes are routinely exceeding one million gates. These million-gate-plus designs require large and cumbersome HDL source code and long periods of debugging time. Emerging embedded processor methodologies are also complicating the design process. Moreover, the need to serve two distinct language-driven design flows (hardware and software) is now making HLL design support imperative.

Xilinx is investing time and technology in the industry-wide HLL efforts through partner technologies such as Synopsys® SystemC™ and Celoxica Handel-C – as well as through Forge Compiler, which Xilinx acquired from LavaLogic™ two years ago. The results are leading to optimized performance for FPGA devices, and to better integration of the co-design and co-verification phases of the embedded systems design flow.

Longer-term technology is also being defined to help you "architect" the potential design at the HLL source code level, analyze what modules should be implemented in the logic design flow, and determine what modules are required in the processor design flow to reach optimum system performance.

Conclusion

New device capabilities will continue to push design complexity. The good news is that Xilinx design tools are keeping pace. New releases of ISE software will help you keep your design time down and your time to market fast. For more information on Xilinx ISE logic software, go to *www.xilinx.com/ise* – and watch for the release of ISE 5.1i coming in late summer.