Now Get Faster Timing Closure with ISE 5.1i

ISE Macro Builder, the new timing closure capability available in the latest Xilinx ISE 5.1i release, allows you to reuse design blocks and IP cores easily with assured timing performance.

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As design complexity increases, achieving timing closure becomes more challenging than ever. In an effort to reduce time to market, designers typically reuse as many existing design blocks and IP cores as possible. Of course, you can never be sure that the reused design block will perform at the same speed in the new context, right?

Wrong. Xilinx, the leading provider of timing closure and design reuse solutions since the company's founding, has made another important breakthrough: Now you can easily lock in the design performance of a reused design block. With the new ISE (Integrated Software Environment) Macro Builder, you can easily capture both your HDL design code and the placement information of a "known-good" design block – and maintain the performance of the captured design block for reuse in future designs.

Macro Builder Technology

Macro Builder technology is based on relationally placed macros (RPMs) that enable you to control the placement of components of your design relative to each other. By using RPMs, you not only obtain a high degree of control over the final design performance, but also significantly reduce place-and-route runtimes for functions defined as RPMs.

One of the most important uses of RPMs is the creation of user-defined blocks and IP cores for design reuse. In addition, RPMs also make it possible to instantiate design blocks and IP cores multiple times in a top-level design. The performance of each RPM instance is highly predictable and repeatable. Moreover, place-and-route runtimes for those portions of the design are typically very fast.

Before the 5.1i release, creating an RPM involved manually entering the relative location constraints (RLOCs) of each component in the RPM. For small RPMs with few components, this does not constitute a significant problem. However, for large RPMs containing hundreds or more individual elements, entering RLOCs can be a time-consuming and error-prone task.

ProActive Timing Closure

The Macro Builder works with the ISE 5.1i Floorplanner to further facilitate the creation of RLOCs. The ISE 5.1i Floorplanner can be used to locate the logic of your user-defined IP core and then save the placement information in the form of RPM RLOCs in a netlist constraint file (NCF). The NCF, along with the original EDIF netlist, gives you a complete description of your "known-good" design block.

Simple Steps to Create a Reusable Design Block

The following shows the steps to create a reusable design block with ISE 5.1i:

1. Write HDL description (e.g., core.v or core.vhd) for the design block function.
2. Synthesize the core HDL – without I/O insertion – to get the netlist (e.g., core.edf).
3. Use the ISE Constraint Editor to create and apply timing constraints to the design block via UCF (e.g., core.ucf).
4. ISE Translate and NGDBuild will take EDIF and UCF to generate NGD (e.g., core.ngd).
5. (Optional) Use ISE Floorplanner to define area group to constrain the core in a fixed "shape."
6. ISE Implement via MAP/PAR generates NCD (e.g., core.ncd).
7. Make necessary iterations to meet the timing goals.
8. Open the core design in ISE Floorplanner.
9. Read in "placed" NCD and the physical constraints from the placement to make the floorplan match the post-PAR placement.
10. Save via "Write RPM to NCF ..." command on File menu of ISE 5.1i Floorplanner (e.g., core.ncf).

Figure 1 shows the flow chart of the reusable design block creation process.

Reuse Predefined Design Blocks

Instantiating predefined design blocks (typically, Netlist (core.edf) and NCF (core.ncf) in any of your projects is now very simple. All you have to do is write the top-level HDL description containing one or more instances of the design block, then synthesize and implement your design as usual. ISE NGDBuild automatically searches for the NCF (e.g., core.ncf) when it processes the netlist (e.g., core.edf), and annotates each element of each instance in the top-level design with the RLOCs from the NCF.

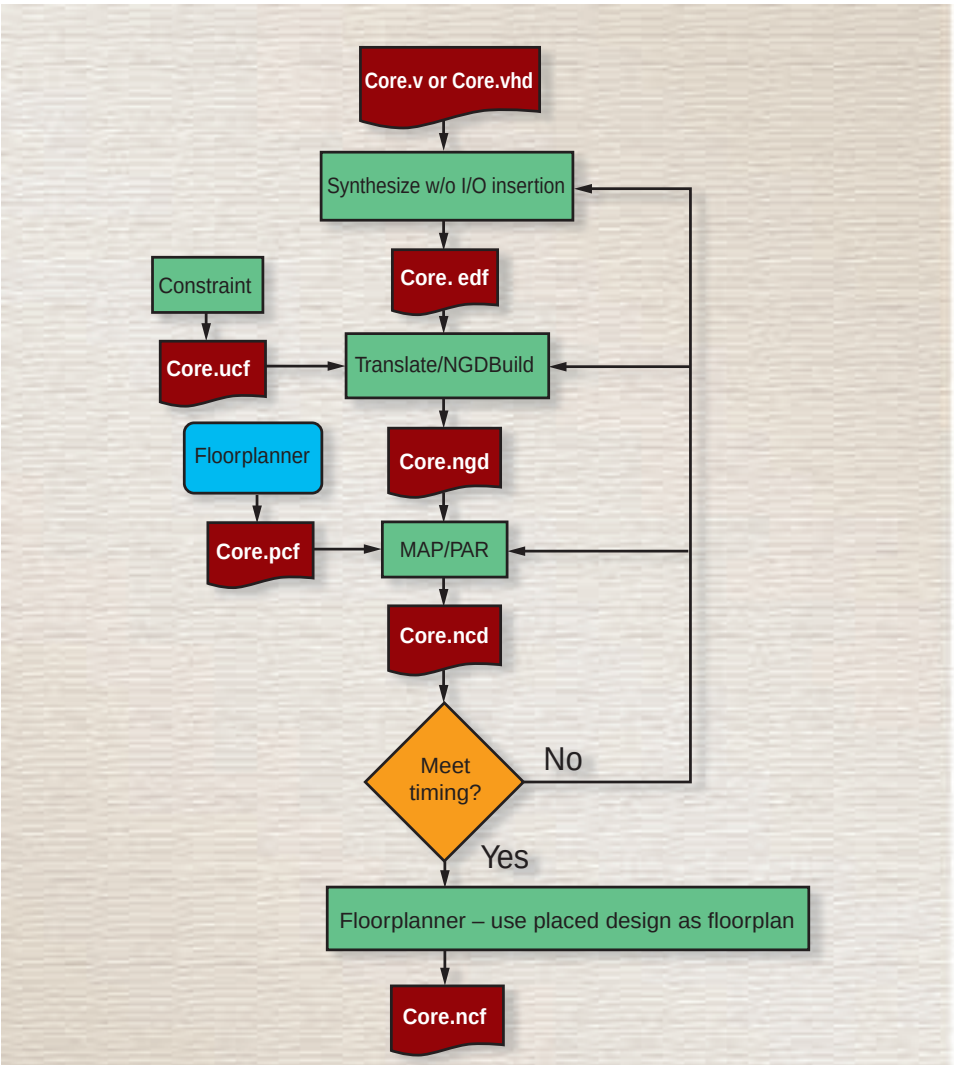

Figure 1 - Macro Builder flow chart

Figure 2 shows the flow chart of the predefined design block reuse process. ISE 5.1i PAR uses the RLOCs during placement, thereby preserving the performance of the original core implementation. Placement runtime of the reused design logic is typically very fast.

Conclusion

We believe that Macro Builder, the new ProActive Timing Closure capability available in ISE 5.1i, will enable you to easily create any large design block or IP core design for reuse with highly repeatable performance. The Macro Builder can help you achieve your timing requirements quickly, significantly shorten the design process, speed up time to market, and reduce development cost. To find out more about ISE 5.1i or to obtain an evaluation copy of ISE 5.1i, visit *www.xilinx.com/ise.*

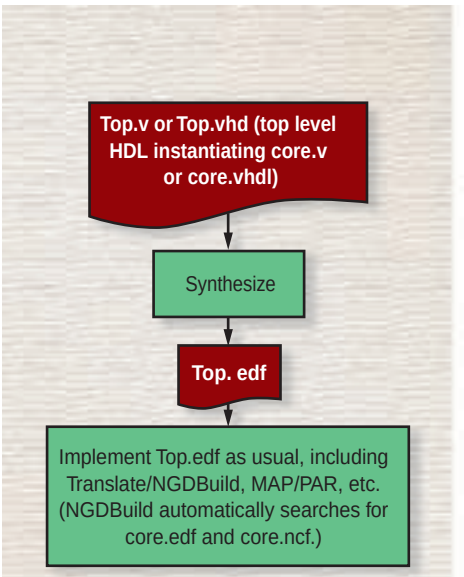

Figure 2 - Design block reuse flow chart