Xilinx ISE 4.1i Delivers the Speed You Need

Xilinx ISE 4.1i presents a new set of features and device support to give you the fastest time to market with the most advanced technologies available for FPGA design today.

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The new version 4.1i of the Xilinx Integrated Software Environment (ISE) design tool suite has hit the streets running. In this special section of Xcell, we will give you a detailed look at ISE 4.1i.

Among the improvements we have made are simplified product configurations and software runtimes up to two times faster than ISE 3.1i. We've added ProActive Timing Closure and expanded your choice of verification strategies to deliver the fastest performance possible and the best design flows available – despite the push towards ever-increasing design complexity and size. ISE 4.1i also includes upgrades of existing tools, such as ModelSim™ and ECS (Engineering Capture System) software.

ASIC designers looking to migrate to Platform FPGAs will be happy to find familiar ASIC tools from Synopsys®, such as PrimeTime™ static timing analysis and LEDA™ HDL analysis. Moreover, the ISE 4.1i release includes XPower – the industry's first power and thermal analysis tool for FPGAs and CPLDs.

With all this improvement and expanded functionality, ISE 4.1i will allow you to reliably get your product to market faster than your competition.

Simplified Configurations – A Single Look and Feel

ISE 4.1i has been simplified to four powerful configurations:

- ISE Alliance Series™ configuration – for EDA design flow integration
- ISE Foundation™ configuration – for the most robust single-vendor programmable logic design platform available
- ISE BaseX configuration – for a cost-effective, full-featured, PC-based programmable logic design environment for the standalone designer, and device size support up to 300K gates
- ISE WebPACK™ configuration – for a free, Web-delivered design environment for CPLD customers and entry-level FPGA designers, with device size support up to 300K gates.

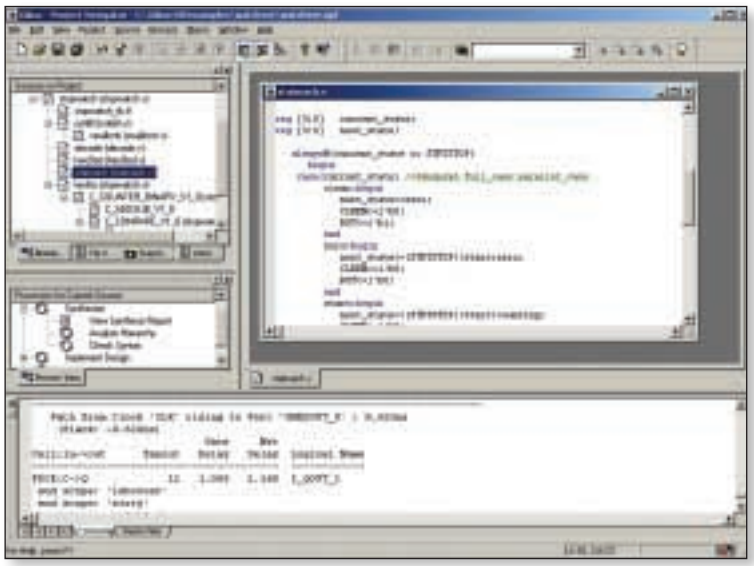


Figure 1 - ISE Project Navigator

Full Device Support in a Single Package

All Xilinx device families can be designed and programmed from the ISE family of products. This includes existing devices as well as those new FPGA and CPLD families scheduled to be released in the coming year.

ISE 4.1i also delivers a new, unified look and feel in the Alliance and Foundation configurations. By combining ISE Alliance and ISE Foundation configurations into a unified development effort, our customers realize the best performance and features in any of the ISE design configurations, and migration or upgrade between ISE packages is quick and easy.

Project Navigator Up Front

As shown in Figure 1, both ISE Alliance and ISE Foundation customers will now see Project Navigator for their design management tool. Project Navigator features several new powerful features, including integration with Exemplar's LeonardoSpectrum™ synthesis environment, Unix platform support, EDIF source support, and more. For Alliance customers who want to transition over the coming year, Design Manager will still be available in ISE 4.1i.

Installs Just Got Easier

ISE 4.1i contains significant improvements to the installation process. Immediately, you will notice ISE 4.1i searches for earlier versions of ISE and offers to remove the older versions of software, helping to free up disk space – or ISE 4.1i allows you to save your older ISE versions.

Adding device support is quick and easy. You can add support for new device families incrementally at a later date simply by re-running the 4.1i install program.

50% Faster Runtimes – Again

The Xilinx Intellectual Property, Services and Software Group operates under a mandate to deliver 2X better software execution with each major release, and ISE 4.1i is no exception. Benchmarks indicate you will see as much as 50% faster design compilation – that means as many as 100,000 gates compiled per minute. And that translates to millions of gates compiled per hour. This blazing design speed outperforms all other logic vendors.

Maximum Performance Through ProActive Timing Closure

If you take a design compiled in ISE 3.1i and run it on ISE 4.1i, you will see impressive gains in device performance (Fmax) through a new collection of timing technologies known as ProActive Timing Closure. Collectively, the advances in ProActive Timing Closure technology can deliver as much as 133% better Quality of Results (QoR) than our previous major software version:

- As the industry's most advanced timing-driven, place-and-route technology available, ProActive Timing Closure brings a new level of active control to design timing. Placement algorithms scan the design data paths and place critical paths first, helping to reduce timing delays. A new extra-effort routing mode remembers which paths in

an implementation pass successfully met timing requirements, and then transparently "re-places" and "re-routes" unsuccessful areas to attempt to meet overall timing goals. And our new Directed Routing brings predictable and repeatable place-and-route capabilities to IP cores.

- ProActive Timing Closure further expands physical synthesis for programmable logic by using physical timing information to ensure that optimization during synthesis is focused on the critical paths. ISE 4.1i works with Synplicity® Inc.'s Amplify™ software and new TOPS™ (Total Optimization Physical Synthesis) capability to further source this physical timing information. [See "ProActive Timing Closure Delivers up to 133% Better Device Performance" in this issue of *Xcell* for more information on ISE physical synthesis.]
- Timing and HDL interaction now occur at several levels of implementation, offering design-specific tips that suggest modifications to the design, constraints, or source code, to help meet the design's timing requirements.
- ISE 4.1i offers timing cross-probing from the timing analysis report to either the Xilinx Floorplanner or to third party synthesis "technology viewers." Cross-probing displays exactly where the problems are in the design in the physical floorplan of the FPGA, the logic gates which were created during synthesis, and even the specific HDL source code itself, significantly reducing debug time.

Expanded Verification Strategies

As designs grown in complexity and size, verification becomes a greater challenge. ISE 4.1i has been designed to expand the options you have for checkpoint verification. At each stage of the design cycle, you can check your design for accuracy.

First Formal Verification Capability for Programmable Logic

ISE 4.1i offers integration with Synopsys Inc.'s Formality™ and Verplex Systems Inc.'s Conformal™-LEC equivalency checkers, leveraging the same technology that was adopted in past years to check high-density ASICs. In the equivalence method of testing, design passes can be checked in "blocks of logic" against a previous known-good version. This can occur at any point in the design cycle, particularly in post-synthesis and place-and-route passes. This strategy offers a rapid checking method that is proving invaluable to high-density design work. For Virtex-II designers moving to 1-million gate designs and above, this new formal verification integration provides a valuable step in the Platform FPGA initiative. [See "High-Performance Platform FPGAs Now Need Formal Verification" in this issue of *Xcell*.]

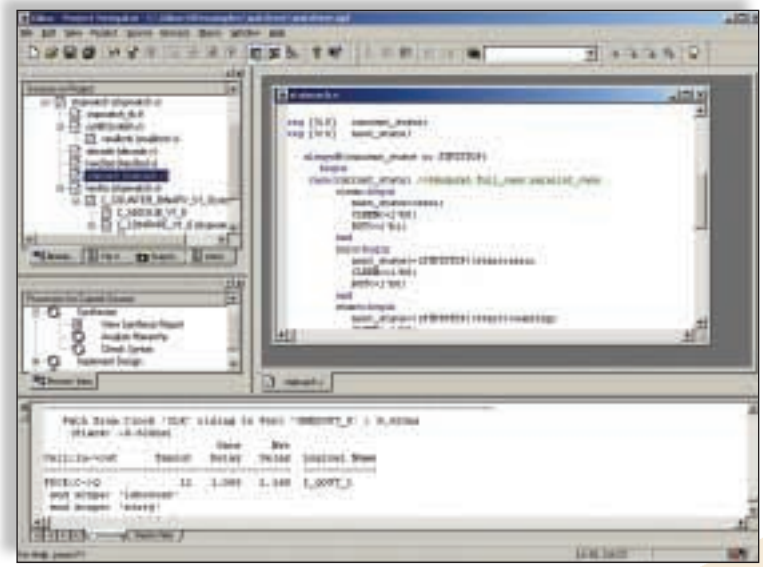


Figure 2 - ISE Engineering Capture System (ECS)

ISE 4.1i Supports ModelSim Version 5.5

ISE 4.1i also includes support for the 5.5 family of ModelSim HDL simulators from Model Technology, a subsidiary of Mentor Graphics Inc. The ModelSim Xilinx Edition (XE) simulator, has been upgraded to version 5.5 as well. These new versions of ModelSim software add valuable library updates, and they feature support to keep Xilinx ISE 4.1i at the forefront of HDL simulation use with:

- Library importer wizard
- New library view window
- An array of bug fixes.

For convenience, the HDL simulation libraries are now broken out as either CPLD- or FPGA-centric, based on either VHDL or Verilog hardware description languages. This separation of libraries allows the smallest possible download size for the desired design application.

ECS Schematic Capture

When upgrading to the ISE Foundation 4.1i software from Foundation Series, customers will notice a new change in their schematic capture and block diagram editor. Shown in Figure 2, ECS is now the schematic capture product for all software configurations. The Xilinx ECS application provides the designer with a powerful graphical input tool for creating schematics and block diagrams. Block diagrams can be created and used as the "top level" description of an HDL design. The designer can describe logic modules in the HDL editor, using VHDL or Verilog, and then use ECS to auto-generate graphical block symbols for each module. Designers can then instantiate and connect the symbols to create a block diagram representation of the design. Prior to synthesis and implementation, the diagram is converted into an HDL netlist that describes the blocks' interconnectivity, which (along with the HDL modules) will be used for subsequent synthesis and implementation in the target Xilinx device.

ECS also supports traditional schematic-based PLD design. Symbol libraries are provided for each Xilinx device architec-

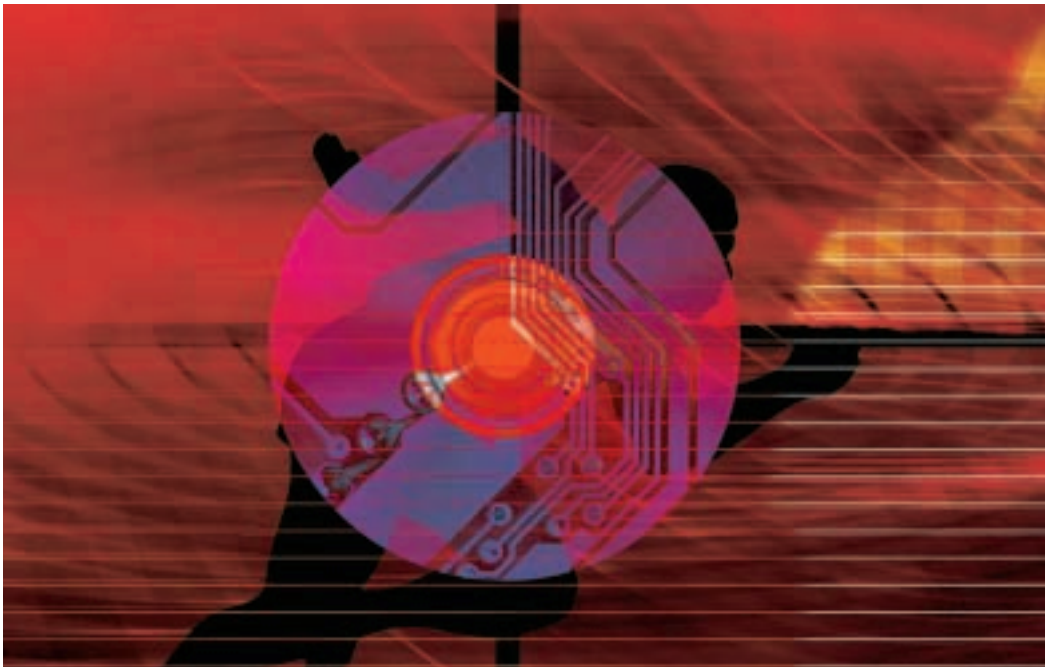
ture, which allows the designer to define a design using flip-flops, counters, gates, and other mechanisms. Symbols come in two varieties – "primitive" components such as a two-input AND gate, and "macro" symbols for more complex functionality, such as counters. ECS now not only provides enhanced functionality and user friendliness, but it will also serve as a framework for future graphics-intensive features in ISE Foundation software.

Some of the new features in ECS include:

- **Multi-window interface** – Multiple schematic and/or symbol windows can be open simultaneously.
- **Enhanced object attribute handling system** – The designer can now arbitrarily and easily create custom attributes for objects (e.g. wires or symbols). Also, attributes for all currently selected objects can be viewed/edited at the same time.
- **Right mouse button menu support** – You can accelerate design tasks by making editing actions immediately available for currently selected object(s).
- **Enhanced design rule checking** – Objects that result in warnings or errors are highlighted on the schematic sheet so they can be easily found.
- **Preferences menu** – Rather than editing a text initialization file, you can now choose application settings and user preferences from a menu.
- **Customization** – Now you can create sheet sizes to your exact specifications.
- **Support for Windows® Clipboard** – For design documentation, you can cut-and-paste diagrams and schematics (or portions thereof) into other applications such as Microsoft Word.
- **Print Preview** – Now you can see – and adjust – how a printout will look before you print it out.

FPGA Tools Powerful Enough for ASIC Users

As the Platform FPGA initiative has reached full steam in the industry, we have seen an influx of ASIC designers converting to FPGAs – both for prototyping and for full-production logic. In order to facilitate the migration of ASIC designers to FPGAs, we have provided additional tools that ASIC designers have come to know and love.



XPower

This release of ISE 4.1i includes the XPower power analysis product – the industry's first power analysis tool with thermal analysis and reporting capability. XPower lets you see early on in the design cycle how the logic activity will affect the thermal characteristics of Xilinx FPGAs and CPLDs. XPower software is proving invaluable in the high-density design world of Virtex-II devices where multiple FPGAs may be operating at 90% capacity or higher on a single board. Likewise, XPower excels in the low-power world of CoolRunner™ CPLDs where battery life and low power consumption are critical to product success.

Synopsys PrimeTime Support

ASIC designers who are more familiar with the Synopsys PrimeTime™ tool for static timing analysis can now use it for their FPGA designs in ISE 4.1i. The Xilinx Timing Analyzer, also delivered in ISE 4.1i, remains the golden signoff for static timing analysis of Xilinx FPGA designs.

Synopsys LEDA-HDL Analysis

ProActive Timing Closure includes HDL analysis capabilities from within XST (Xilinx Synthesis Technology) reports, and ASIC designers can use the Synopsys LEDA™ family of HDL products with ISE 4.1i if they prefer. The LEDA design analyzers not only provide HDL analysis and suggestions on how to improve HDL source code, but they also offer the flexibility of customization to support corporate design standards. Customers can use the ProActive Timing Closure HDL analysis capabilities and the Synopsys LEDA tools together to deliver programmable synthesis-ready source code earlier, reduce extraneous logic cells, and get to timing closure faster with better overall results.

Conclusion

If speed is what you need, Xilinx ISE 4.1i will put you on the fast track for time to market. Simply put, the ISE 4.1i design tool suite will enable you to realize the fastest device speeds and highest design performance available in the industry for both low-density and high-density designs – and that's not all. To learn even more about the enhanced capabilities of ISE 4.1i, or the software upgrade process, go to *www.xilinx.com/ise/xcell/*. Upgrade to ISE 4.1i before your competition does.