Mentor Graphics Offers Seamless Integration for Virtex-II Pro Developers

Working with Xilinx, Mentor Graphics has enhanced its Seamless hardware/software co-verification solution specifically for developers using the Virtex-II Pro family of FPGAs with embedded IBM PowerPC 405 processor cores.

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Perhaps you've been slaving in the lab for two weeks now, and you still can't get your first prototype running. More complex than previous projects, you're dealing with a new processor, a lot more code, and a substantial increase in logic content. Verifying the software on the target hardware requires that the board design be complete and that boards are fabricated and available. Errors uncovered in hardware on "finished" boards carry the risk of having to schedule a board respin, or compromising the software design to work around problems in the hardware.

What's the answer? A virtual system prototype – a prototype in which system designers can integrate their embedded software and hardware before committing to silicon. Working together, Xilinx and Mentor Graphics have developed a custom Seamless® hardware/software co-verification solution targeted specifically for use with the Virtex-II Pro™ family of FPGAs with embedded IBM® PowerPC™ 405 processor cores.

With both hardware and software readily changeable in a virtual prototype, you can perform comprehensive validation and analysis in a safe environment. And because a virtual system prototype incorporates both a logic simulator and debugging environment for the processors, it's possible to get full simultaneous control and visibility into the logic and internals of the processor.

Furthermore, many design problems exposed during system integration are attributable not to software or hardware but to the complex interaction between the two. Thus, you can gain substantial benefits from validating the design at the system level. Exercising the boot ROM code, hardware diagnostics, device drivers, and the RTOS (real-time operating system) will expose most hardware/software interface errors – eliminating hardware prototype iterations and significantly reducing system integration time.

Seamless Hardware/Software Co-Verification

The Seamless co-verification tool combines logic simulation environments used by hardware designers with debugging environments used by software engineers. Seamless co-verification controls the flow of data between the environments and synchronizes the simulations. The patented Seamless Coherent Memory Server allows you to switch dynamically between detailed hardware verification and high-speed software execution without requiring any changes to the design setup, or even halting the simulation.

A single processor system is illustrated in Figure 1. However, the Seamless solution also works in multi-processor environments. For example, the Virtex-II Pro FPGA may be used on a board (in this case, the system would be composed of one or more boards) with one or more standard CPUs, DSPs, or processors embedded into ASICs. There are currently more than 110 Seamless Processor Support Packages (PSPs) available for a comprehensive range of CPUs and DSPs.

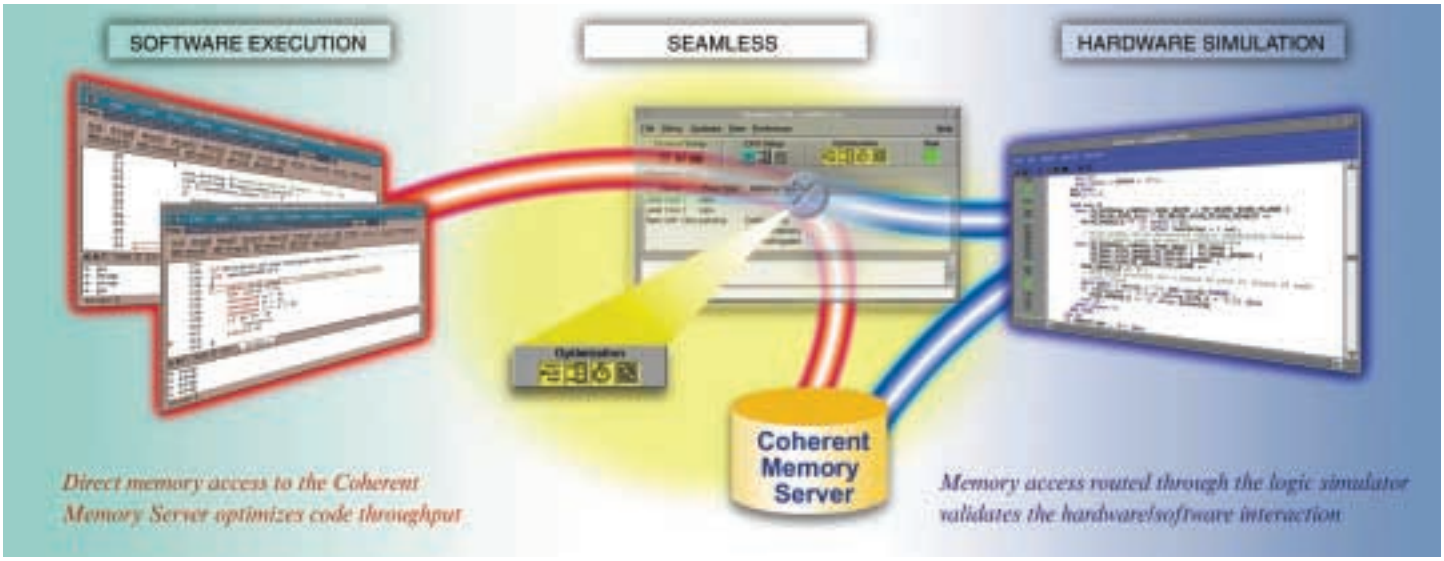

Figure 1 - The Seamless solution links hardware and software verification environments efficiently.

A Custom Solution for Virtex-II Pro FPGAs

The Seamless co-verification tool is a very flexible solution supporting a wide range of design styles, processor types, and memory system architectures. One caveat, however, is that system designers should make no assumptions about the processor used, the memories used, or how the processor interfaces to the rest of the design. Thus, there's a configuration process before you can start using the solution.

Although we cannot entirely eliminate this configuration process for Virtex-II Pro designers, we have made it simpler in several ways:

- We know that the PowerPC 405 core is the embedded processor.
- In Virtex-II Pro FPGAs, the PowerPC 405 core is interfaced to the logic fabric through a fixed block known as the "gasket." By expanding the boundary of the existing cycle-accurate Seamless PowerPC 405 model to include gasket logic, we simplify the task of bringing the Seamless tool into the design flow and raise the performance of the co-verification environment (Figure 2).
- Virtex-II Pro devices incorporate memory blocks known as BRAM (buffer random access memory). To use the Seamless optimization feature, memory models must be Seamless-aware. The solution for Virtex-II Pro FPGAs includes Seamless-ready models for Xilinx BRAM blocks (Figure 2).
- Virtex-II Pro design kits contain several reference designs. We at Mentor Graphics have created and verified Seamless-ready netlists of three of these designs (including creation of the relevant memory maps) to provide you with a jumping-off point for incorporating the Seamless solution into your particular design.

The Seamless solution works with the complete range of logic simulation solutions supported by Xilinx design kits, and has been verified with the software tool chains recommended and supported by Xilinx.

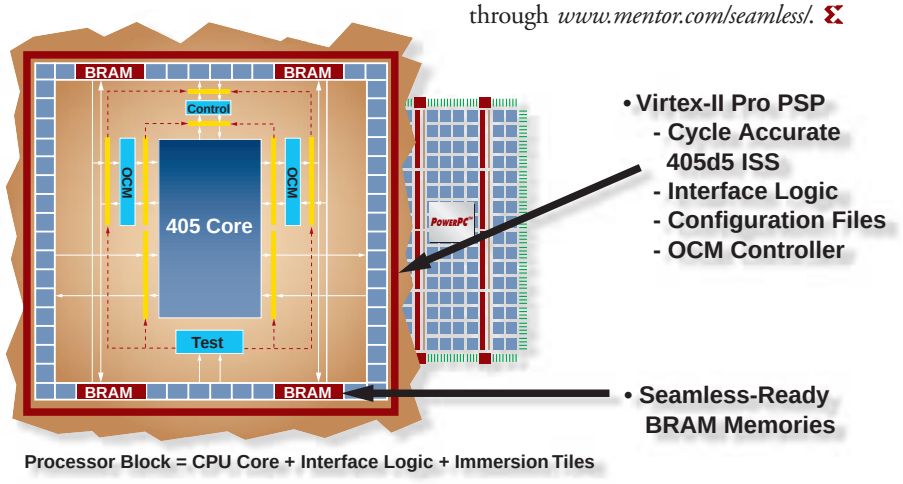

Figure 2 - The Seamless solution for Virtex-II Pro FPGAs includes a custom PowerPC 405 model and Seamless-ready BRAM memory models.

Conclusion

The Seamless design tool is an industry proven solution for co-verification of hardware and software across a wide range of embedded system applications and design styles.

The customized Seamless package for Virtex-II Pro FPGAs was presented at a live Web seminar co-hosted by Xilinx and Mentor Graphics on October 23, 2002. The seminar demonstrated and described how Seamless hardware/software co-verification specifically worked with Virtex-II Pro FPGAs. An archive of this Web seminar may be viewed at *www.mentor.com/seamless/seminars/xilinx/*.

Additionally, application notes and technical papers on how the Seamless solution has been applied in different environments are available through *www.mentor.com/seamless/*.