Check Out the New ModelSim SE 5.6 Simulator

The ModelSim SE simulator, release 5.6, meets all the challenges associated with designing for multimillion-gate Virtex-II and Virtex-II Pro FPGAs.

by Anna Leef
Product Marketing Manager
Model Technology
annal@model.com

True to its origins, every feature of the newest member of the ModelSim® family from Model Technology is integrated into its Single Kernel Simulation (SKS) technology. SKS provides the highest capacity and performance, regardless of the languages or platform you choose.

- It excels in all types of design environments.
- Its performance is equal to the most demanding simulations.
- It provides VHDL, Verilog™, and mixed-language support.
- Its powerful debugging capabilities can solve the most difficult problems.

Multimillion-Gate FPGA Designs

Multimillion-gate designs require high performance for all simulations, as well as the capacity to handle the demands of gate-level timing simulation. Today, the ModelSim SE tool is used on designs exceeding 25 million gates. The ModelSim 5.6 tool offers a number of new performance-enhancing optimizations.

With 60% of the market, the 5.6 release accelerates the industry's leading VHDL simulator. The release also delivers ModelSim's third-generation Verilog global optimization technology and includes new optimizations for mixed-language designs. ModelSim VHDL has been updated with improved memory management, IEEE library performance optimizations, and other intelligent compiler advances that facilitate a broad range of designs. ModelSim's third-generation global optimization technology continues to improve Verilog RTL (Register Transfer Language) and gate-level performance across many design styles. For maximum Verilog performance, you should compile your top-level modules with "+opt." This turns on the optimizations. (As with all Verilog simulators, ModelSim's performance mode affords less visibility into the design than the debug mode, so debug your design first and then enable +opt for regression tests.)

Tuning Your Design For Performance

Larger designs mean more tests. Typically, billions of vectors are simulated against large designs, so any drag on simulator performance can dramatically increase the amount of time you spend on verification.

The ModelSim 5.6 release includes a new option that significantly improves simulation throughput. After a design is compiled, it must be loaded into the simulator. This process is called "elaboration." Elaboration, especially for large gate-level simulations with timing, can consume a significant part of the overall simulation run time.

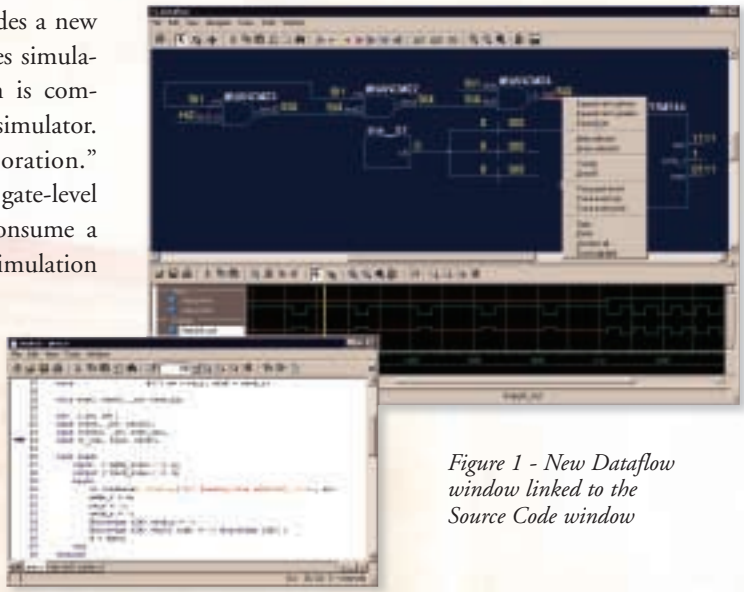

Figure 1 - New Dataflow window linked to the Source Code window

ModelSim's new elaboration option loads the design into a reusable file so that multiple simulations can be run off the same file using different stimuli – eliminating the need to reload the design. As an example, a ModelSim customer had a 5 million-gate design. It took an hour to load the design and SDF (Standard Delay Format) file. His test suite contained thousands of tests. Adding an hour to each run would have created a drastic performance penalty, but with the new elaboration option, he only had to load the design once.

By analyzing your entire design flow, ModelSim SE's integrated Performance Analyzer can uncover bottlenecks such as the impact of testbench tools, .vcd file generation, or inefficient HDL coding styles – often identifying additional opportunities for better throughput. Measuring the performance impact of all areas of your environment gives you the power to make better technology decisions.

In addition, larger designs are also much more likely to include simulation models and testbenches written in languages other than VHDL or Verilog, which also can have a negative impact on performance. Many users unknowingly decrease performance by creating many events through the testbench interface. But with ModelSim, your productivity does not have to be hobbled by your testbench – or other tools. Many users have identified performance bottlenecks and have either modified their environment coding style or found replacement tools that can be easily integrated into the ModelSim tool.

To better understand how to optimize the ModelSim simulator for performance, please refer to the performance application note at *www.model.com/resources/pdf/improving_performance.pdf*. This document provides performance flow details for Verilog, VHDL, and mixed-language simulations.

Best User Interface and Debug Tools

The complexity of multimillion-gate designs makes it no longer feasible to debug errors on the lab bench. What you need is an integrated debug environment with full access to the internal components of the design. The ModelSim SE 5.6 simulation tool delivers the industry's most tightly integrated and feature-rich solution for debugging. Source code debugging, waveform generation and comparison, an enhanced Dataflow window, and code coverage are some of the features already available in the ModelSim SE 5.6 release.

With the ModelSim 5.6 edition, a completely revamped Dataflow window enables you to view and debug your design graphically. The window depicts the physical connectivity of your design and lets you easily investigate unexpected values.

In addition, because all of the ModelSim windows are cross-linked (Figure 1), you can simply drag-and-drop design elements from the Structure or Signal windows to the Dataflow window. The visual trace engine then generates a graphical representation of that portion of the design. From there you can expand to any level by sprouting inputs or outputs.

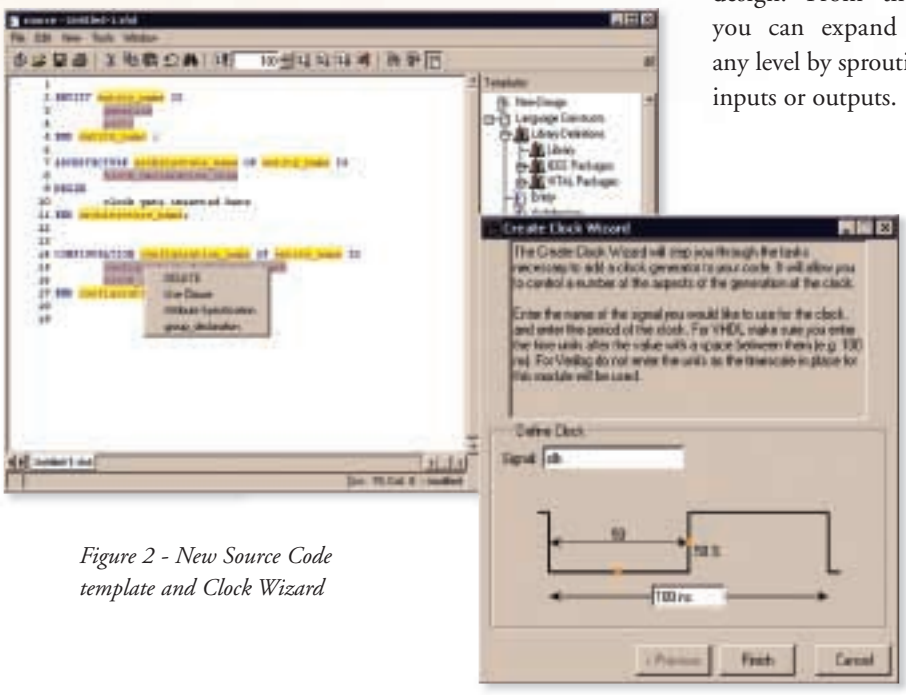

Figure 2 - New Source Code template and Clock Wizard

To identify a signal with an unknown value in the Dataflow window, simply place the cursor in the Wave window at the time of the unknown, then use ModelSim's new ChaseX™ feature to draw a path to the source of the unknown. The underlying HDL code will appear in the Source window.

To simplify design entry and editing, the Source window has new code templates and design wizards to help you create VHDL and Verilog code. All language constructs are available with a click of the mouse. Context-sensitive expansion of templates means you don't have to know which constructs go where. The design wizards walk you through building more complex HDL blocks, including parameterizable logic blocks, testbench stimuli, and new design objects. Advanced developers can use the code templates as an interactive language reference manual.

Saving simulation data is easier with waveform viewing and exporting. These features allow you to save simulation data for viewing or comparing, even while the simulation is still running.

Project management was also improved significantly in the ModelSim SE 5.6 release. The new version further enhances these improvements with a streamlined interface, an automatic compile-order function, and support for reusable design views that run different configurations of the simulation. Project management enables efficient debug, source modifications, recompiling, and resimulation without any scripting knowledge.

Conclusion

With fast performance, the most comprehensive set of integrated debug tools, and proven success on multimillion-gate designs, ModelSim SE 5.6 is a natural choice for Virtex™-II and Virtex-II Pro™ designs. To download an evaluation copy of ModelSim 5.6, go to *www.model.com/evaluations/default.asp.* Σ

ModelSim SE 5.6 Easily Simulates 6 Million-Gate FPGA Design

Dillon Engineering, Inc., of Edina, Minnesota, recently developed a two-dimensional Fast Fourier Transform (FFT) for an image processing application. Among the many complex aspects of the project, the Dillon Engineering team had to contend with two different sizes of the same RTL (Register Transfer Language) design. One of the benchmarks required by Dillon's customer was a physical simulation of the whole design.

"We were able to simulate the smaller design with our existing tool, but we couldn't run the big, fast version because it exceeded the capabilities of the simulator we were using," said company President Tom Dillon.

Simulation Required for Large Designs

The larger of the two designs the Dillon team had to simulate was a 6 million-gate design with nearly 18 MB of external memory. The design targeted two Virtex-II XC2V6000 FPGAs. "This system had enormous processing requirements," said Dillon. "A huge amount of raw data had to undergo extensive processing to convert it into the final 2D FFT. The combination of 16-bit pixel data, a resolution of 2K x 2K pixels, and a required frame rate of 120 fps resulted in 480 megasamples of 16-bit data per second."

Existing Simulator Couldn't Handle the Design

Because the 6 million-gate design kept crashing their existing simulation tool, the engineers decided to try a 30-day evaluation of the ModelSim simulation tool. "We knew we were in trouble if we stuck with our existing simulation tool. If you can't simulate the full design, you can't be sure it's going to fit and actually work. We had to produce simulation results of the full image in the specified number of clock cycles, so we didn't have a choice: we couldn't 'get by' with the smaller simulation," Dillon said.

ModelSim successfully completed the FFT simulation of the full design – meeting the required benchmark.

By upgrading to ModelSim, Dillon Engineering reaped a 30% increase in simulation performance on a million-gate FFT design. They were able to simulate an entire 6 million-gate design for the first time. And they had better language coverage than they had with their old tool.

Summary

"We are growing, and as we do, we are getting better and bigger projects. That means we need bigger and better tools," said Dillon. "As a custom design firm, we have to move up a class in tools to support the projects we want to bring in. The bigger the design, the more ModelSim stands out as the tool to use."