New Spartan-IIE FPGA Family for Digital Consumer Convergence Applications

Spartan-IIE FPGAs offer significant performance improvements for next-generation consumer products.

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The new Spartan™-IIE family is the latest generation of the highly successful Spartan series of programmable logic devices. It is targeted at digital consumer convergence applications where video, audio, communication, and data technologies converge to add more functionality and capability to the end product. The Spartan-IIE family supports system performance beyond 200 MHz and offers features that include distributed RAM, block RAM, 19 selectable I/O standards (including high-speed differential LVDS), and four DLLs, as shown in Table 1.

Distributed RAM

Distributed RAM is an ideal solution for designs that require multiple, small, fast, and flexible memories situated close to the logic. As with all other Xilinx FPGA families, the 4-input look-up table (LUT) in Spartan-IIE devices can be also used as memory, where it can be configured as ROM, and single-port or dual-port synchronous RAM. Each LUT is equal to 16 locations x1-bit wide, as shown in Figure 1. These memories can even be cascaded for various data widths or depths. The competing FPGA families do not have this feature.

Block RAM

In addition to the distributed RAM, Spartan-IIE devices offer dedicated blocks of synchronous RAM for designs requiring larger memory functions, as illustrated in Table 2. The memory block can be used as 4096x1, 2048x2, 1024x4, 512x8, or 256x16. These blocks can also be cascaded for a different configuration or to form larger memory functions.

True Dual-Port Operation

The memory block is dual-port with independent control signals for each port. Hence, these ports can be read from and written to simultaneously, independent of each other. All the control logic is implemented within the RAM block. The competing FPGA families have only 2-port RAM – one read port and one write port. To emulate Xilinx dual port capability, they would need twice the number of memory blocks and additional control logic – and our competitors would still operate with relatively lower performance.

Clock Management

As FPGA density grows, quality on-chip clock distribution becomes increasingly important. Clock skew and clock delay impact device performance. The Spartan-IIE family resolves this potential problem by providing four fully digital dedicated on-chip Delay-Locked Loops (DLL) in each device. These DLLs are used to remove on-chip and off-chip clock delays (de-skew), and to perform clock multiplication, division, and phase shifting.

As a fully digital implementation, the Spartan-IIE DLLs do not have the typical problems encountered with analog phase-locked loops (PLLs), which are extremely sensitive to noise and are difficult to migrate between process technologies. The Spartan-IIE DLLs are not sensitive to noise and process variations. Xilinx DLLS are a standard feature in all densities and all speed grades of the Spartan-IIE family.

Device	XC2S50E	XC2S100E	XC2S150E	XC2S200E	XC2S300E
System Gates	50K	100K	150K	200K	300K
Logic Cells	1,728	2,700	3,888	5,292	6,912
Distributed RAM Bits	24,576	38,400	55,296	75,264	98,304
Block RAM Bits	32,768	40,960	49,152	57,344	65,536
DLLs	4	4	4	4	4
Max I/Os	182	202	263	289	329

Table 1- Spartan-IIE Family Product Matrix

Device	No. of Blocks	Block RAM Bits
XC2S50E	8	32,768
XC2S100E	10	40,960
XC2S150E	12	49,152
XC2S200E	14	57,344
XC2S300E	16	65,536

Table 2 - Block RAM Amount

Flexible Logic Resources

The Spartan-IIE family provides flexible configurable logic blocks (CLBs), allowing implementation of simple or complex logic functions. Each CLB contains two slices. Each slice contains two 4-input Look-up Tables (LUTs), one carry logic chain, two

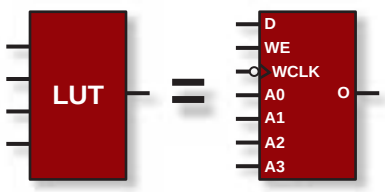

Figure 1- Distributed RAM

storage elements, and control logic (see Figure 2). In addition, each CLB has two dedicated 3-state buffers. These buffers can be used to implement on-chip bussing. The competing FPGA families do not have dedicated 3-state buffers; they emulate this functionality at the expense of logic resources.

Look-Up Table Flexibility

- **Wide input functions** – Multiple LUTs can be cascaded to implement functions of more than four inputs. Furthermore, each CLB has dedicated resources to implement 5-input and 6-input functions in just a single logic (LUT) level of delay. For example, you can implement an 8-to-1 multiplexer within a CLB with one logic level of delay, versus the competing FPGA solution with at least two logic levels of delay.
- **Shift Register** – The LUT can also be configured as a 16x1 single-port RAM, or as a 16-bit shift register. This functionality can be used to implement high-speed Linear Feedback Shift Register (LFSR) counters and other DSP applications.

Versatile I/O

The Spartan-IIE family provides 19 I/O standards that include differential standards such as LVDS, Bus LVDS, and LVPECL, allowing a single FPGA to interface with any other device without using external converters or translators (see Table 3). Differential signaling provides higher performance while reducing power, reducing noise, and lowering EMI emissions.

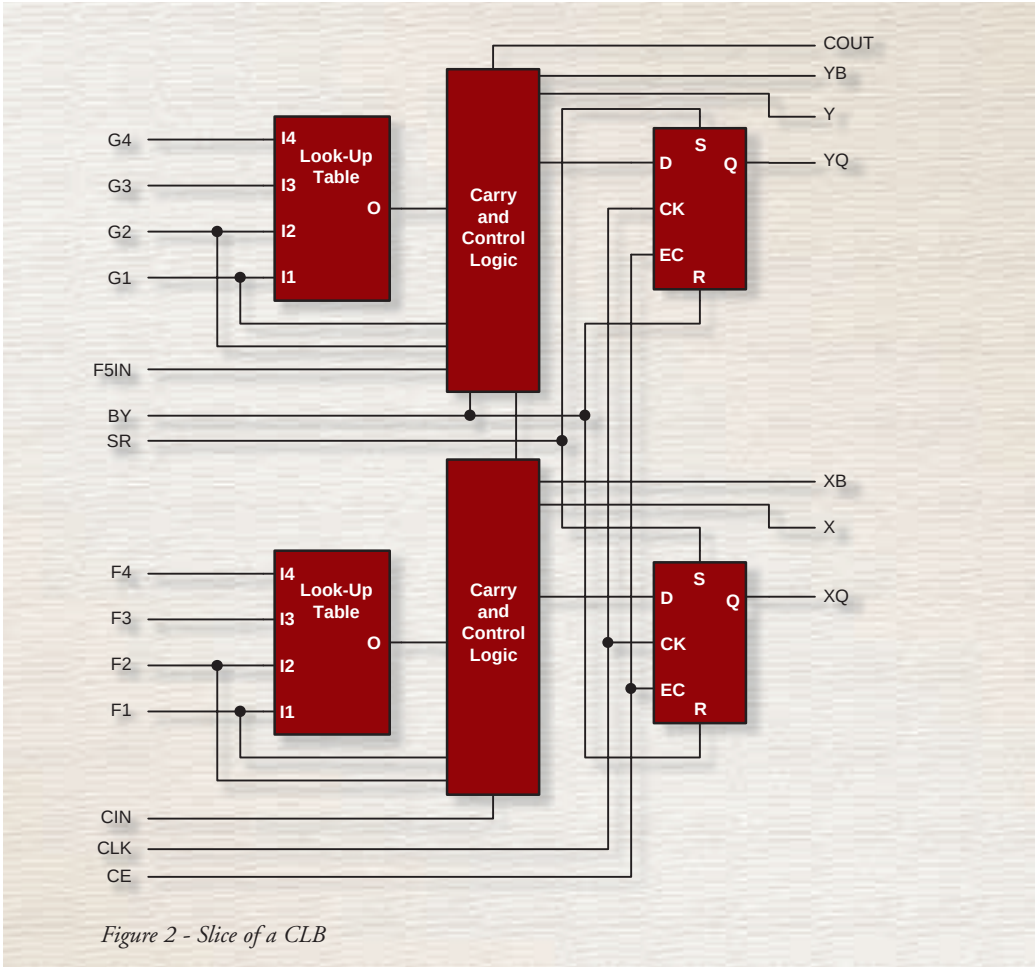

Figure 2 - Slice of a CLB

- **LVDS and Bus LVDS** – The Low-Voltage Differential Signaling (LVDS) standard exists in two implementations: LVDS and Bus LVDS. LVDS is used for unidirectional data transfer, and is optimized for high-speed point-to-point links. Bus LVDS is for bi-directional communication between two or more devices, and is optimized for multi-drop configurations. You can use up to 120 pairs of LVDS and Bus LVDS I/O pins on the largest Spartan-IIE device.
- **LVPECL** – The Low Voltage Positive Emitter Coupled Logic standard is used in 100+ MHz chip-to-chip interfaces. It is also used for transmission of clocks at frequencies over 100 MHz.

Chip to Chip Interface	Backplane Interface	Memory Interface
LVTTL	PCI 33/66 MHz, 3.3V	HSTL-I
LVCMOS2	GTL	HSTL-III & IV
LVCMOS18	GTL+	SSTL3-I & II
LVDS	AGP-2X	SSTL2-I & II
LVPECL	Bus LVDS	CTT

Table 3 - Spartan-IIE I/O standards and typical applications

Software and IP Cores

The Spartan-IIE family is supported in ISE WebPACK™ 4.1i and all other configurations of the ISE 4.1i software. ISE WebPACK is free software that can be downloaded from the Xilinx website. Xilinx also provides the most comprehensive set of IP Core solutions to assist you in reducing your design cycle time.

Conclusion

The new Spartan-IIE FPGA family helps you meet the requirements of digital consumer convergence systems. It gives significant performance and flexibility enhancements by providing on-chip features such as true dual-port memory for system integration, flexible logic resources for simple to complex logic implementation, DLLs for clock management, and single-ended and high speed differential I/Os for faster chip-to-chip speeds. For more information, please see the complete article on Xcell Online at: *www.xilinx.com/publications/xcellonline/.*