# Get up to Multi-Gigabit Speed with the SPECCTRAQuest Design Kit

## Learn how to implement Rocket I/O multi-gigabit serial transceivers in the new Virtex-II Pro Platform FPGA.

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With the introduction of the new Virtex-II Pro™ FPGAs, high-speed Rocket I/O™ serial transceivers are ready to find their way into hundreds of new applications. Are you ready? What used to be confined to a few exotic chips, laden with pages and pages of design and implementation guidelines, is now available to everyone. Xilinx has made it possible to integrate multi-gigabit transceivers (MGTs) into your FPGA, but how will you integrate that high-speed FPGA into your system of printed circuit boards (PCBs)?

In an effort to avoid multi-gigabit headaches, Xilinx and Cadence Design Systems have assembled SPECCTRAQuest™ MGT Design Kits to help you implement the new Rocket I/O MGTs effectively in your system. Whether you need to craft a custom MGT interface and develop your own PCB/backplane/cabling guidelines, or you simply need to apply your MGTs in a standard configuration, the kit gets you moving towards a solution within minutes.

### SPECCTRAQuest MGT Design Kit

Pre-configured circuits in the design kits are ready to simulate for both typical MGT chip-to-chip and backplane PCB interfaces. There's no time wasted hunting for models, testing and correlating them, or figuring out how to connect them together. It has all been done for you. And because the simulation environment is graphical, adapting the circuits for your unique application is as simple as dragging and dropping.

Better yet, the models of the active Rocket I/O MGT circuitry are transistor-level silicon models that have been correlated by Xilinx to match both the actual silicon design and empirical data. This ensures that your system implementation is designed with the most advanced and accurate models available. Add to that fully coupled frequency-dependent lossy package, PCB trace, and connector models, and you're ready to carefully characterize the signal integrity and degradation issues that are inherent in this type of design.

Figure 1 shows a pre-configured simulation drawing for chip-to-chip applications. Although this is actually a 500+ node simulation, it has been simplified through the use of subcircuits and black box models so it can be more easily modified. Just point and click to change trace parameters, physical connections, or other aspects of the circuit.

When your simulations are done and it's time to layout your PCB, the MGT kit has sample footprints and constraint files to ensure a successful layout. It is essential to bind all high-speed constraints into your

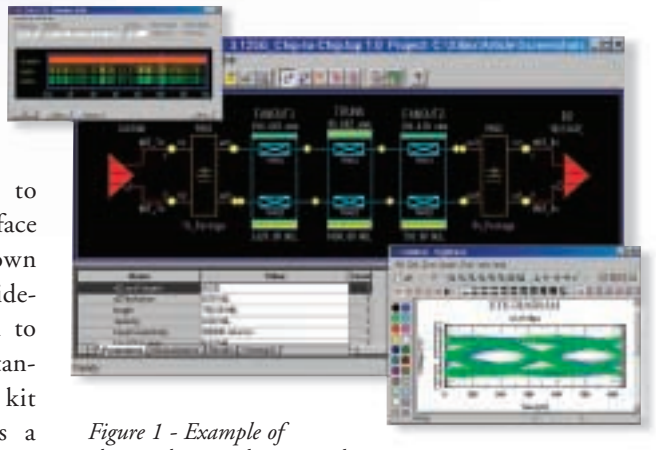

*Figure 1 - Example of chip-to-chip simulation topology*

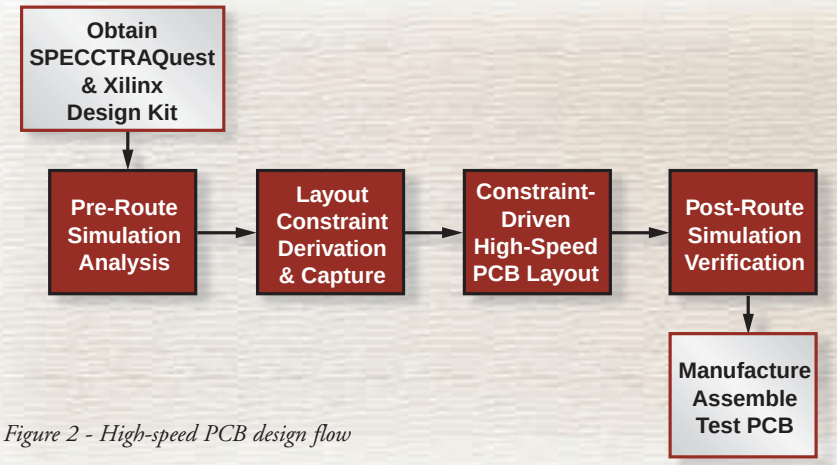


*Figure 2 - High-speed PCB design flow*

PCB database to automate and properly constrain the layout process. If you don't bind your constraints, your layout, post-layout simulation, and actual system behavior will not be as clean as you would want.

To help you along the learning curve associated with designing multi-gigabit links, the kits also contain tutorial "movies" you can run on your PC to clearly illustrate how to use the various aspects of the kit throughout your design process.

### SPECCTRAQuest's Features

SPECCTRAQuest is an integrated design tool that allows you to include both your MGT silicon models and PCB databases in one simulation. You can easily set up extensive "sweep" simulations to sweep circuit variables through a range of values to test out different implementation options.

Simulation of trace parameter variations (such as loss tangents, skin effect, dielectric constant, and other variations), crosstalk, power noise, deterministic/random jitter, and other effects are all included.

Stimulate your circuit with pre-coded 8b/10b pseudo-random bit sequence (PRBS) patterns to create inter-symbol interference (ISI) and study its effect on signal integrity. With the push of a button, you can plot the resulting waveform as an eye diagram so you can quickly quantify the signal degradation from transmitter to receiver. SPECCTRAQuest also provides automated measurements of each circuit's performance. These measurements can be sorted so you can quickly select the best configuration.

After you have determined the best implementation configuration, you can use Cadence's powerful constraint management (CM) tool to electronically capture and manage your layout constraints. The CM tool interacts with the other Connected Team Design Tools (including Concept HDL, Allegro, SPECCTRA™, and SPECCTRAQuest) to enable your whole design team to work concurrently and share data.

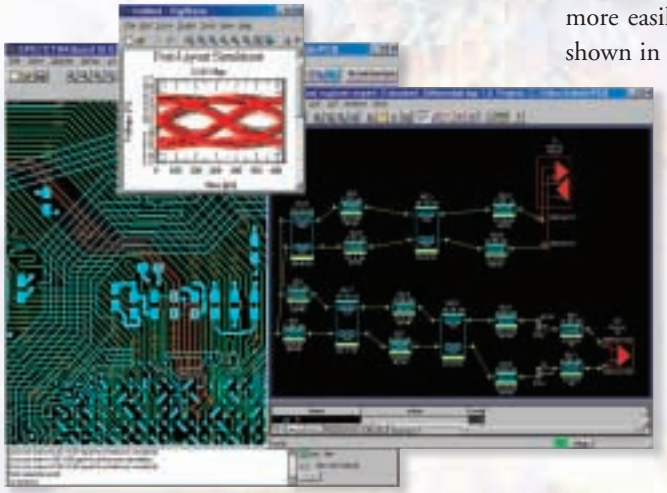

*Figure 3 - Simulation from layout and extracting a differential net*

SPECCTRAQuest has a unique way of superimposing advanced simulation on top of high-speed PCB layout. For more information on the features available in SPECCTRAQuest and other Cadence PCB tools, please refer to *www.specctraquest.com* and *pcb.cadence.com*.

### MGT Design & Implementation Flow

With both the SPECCTRAQuest software and MGT design kit in place, you're ready to exercise the advanced, high-speed design flow shown in Figure 2 to ensure your MGTs are implemented correctly.

The flow begins by configuring a simulation of your unique application. Use the pre-configured topologies in the design kit as a starting point. Simulate your application pre-route by sweeping through all the implementation options and manufacturing tolerances to ensure that the multi-gigabit signals are transmitted and received within tolerances. Use the test patterns and post-processing tools in the kit to help with this phase.

Once an acceptable solution is found, capture the layout constraints in electronic topologies that can be bound into the layout process. Once again, you can use the kit examples to learn how. Perform constraint-driven layout, and then do post-layout simulation on the routed nets to verify that signal transmission is still within tolerance. If the layout constraints were applied and followed, this will be a simple verification step. If a problem is found, the differential net can be extracted to an electrical view to more easily identify the cause of failure, as shown in Figure 3.

### Conclusion

Although using MGTs in your high-speed design can bring higher performance to your FPGA application, you must be careful in performing the implementation. By correctly using the SPECCTRAQuest MGT Design Kit assembled for this task, you can avoid common problems and shorten your design cycle. The kit includes layout guidelines, constraints, topologies, scripts, and utilities that will help you integrate Rocket I/O MGTs into your high-speed Virtex-II Pro designs.

The MGT design kit is available for free download from the Spice Suite at www.xilinx.com. Registration is required if you are not already a Xilinx customer