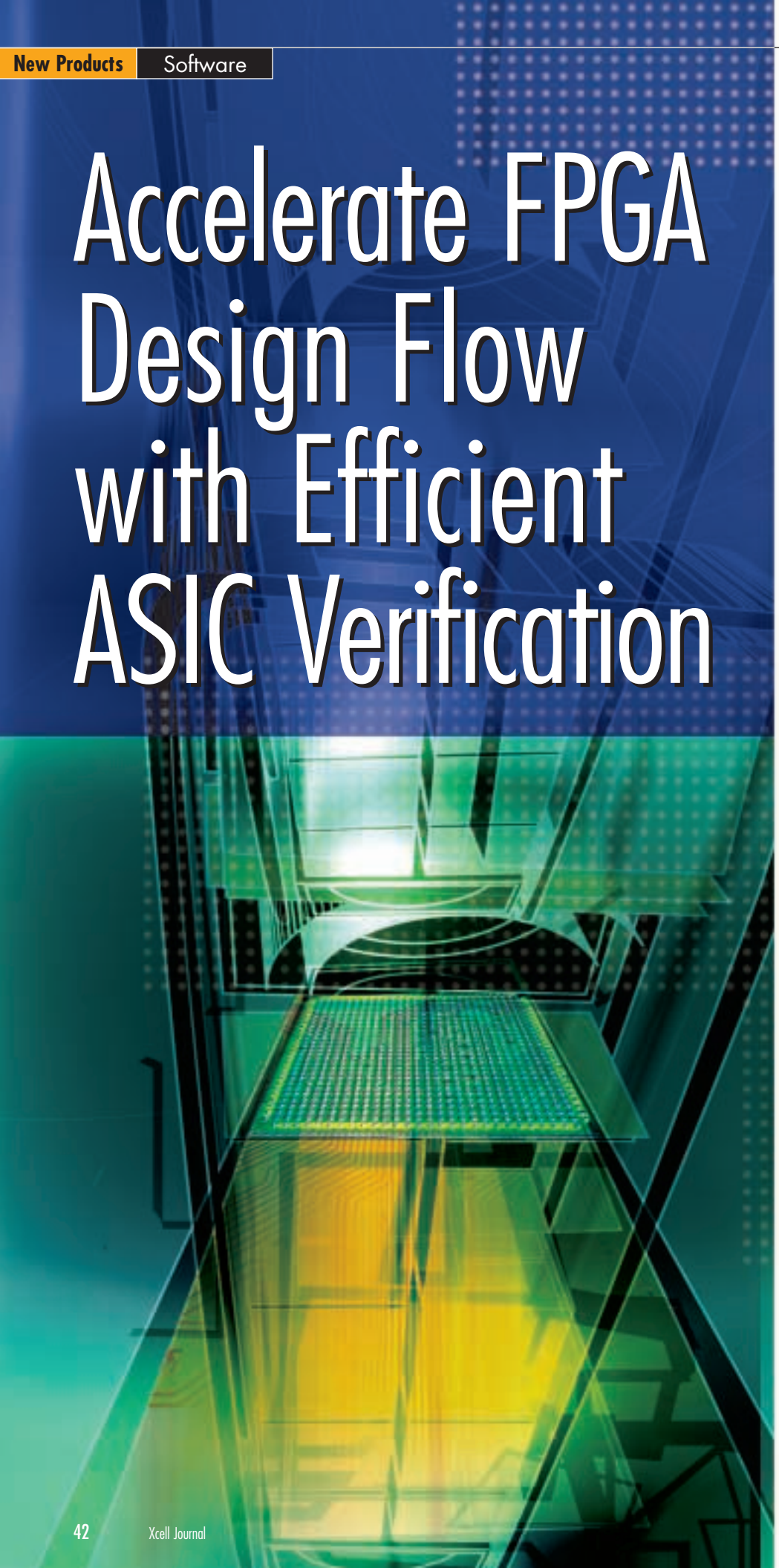
Accelerate FPGA Design Flow with Efficient ASIC Verification



The integration of Mentor Graphics' SpeedGate DSV tool with Sun Microsystems' Sun ONE Grid Engine software enables dramatically reduced synthesis run times.

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Synthesis is one of many compute-intensive operations that can heavily affect the overall design process. To distribute these operations in parallel and accelerate the chip design flow, Mentor Graphics® SpeedGate DSV™ (Direct System Verification) software tool now has integrated support for Sun Microsystems' Sun™ ONE Grid Engine software.

SpeedGate DSV – also known as prototyping, rapid prototyping, or open system emulation – is an advanced methodology for verifying application-specific integrated circuit (ASIC) and system-on-chip (SoC) prototypes using off-the-shelf FPGAs in one or more custom or predefined printed circuit boards (PCBs). As a comprehensive and extensible solution for all aspects of prototype design flow, the SpeedGate DSV product includes partitioning and debugging support, with links to board creation and analysis tools. Currently, the SpeedGate DSV tool supports the Xilinx Virtex™, Virtex-E and Virtex-II families of FPGAs.

The SpeedGate DSV tool consists of an interactive design cockpit that launches partitioning and synthesis tools. It features a completely scriptable interface that plugs into any ASIC design environment – working hand-in-hand with emulation and gate-level simulation. The tool also includes patent-pending advanced partitioning technology that enables designers to maximize FPGA design prototypes. Furthermore, it fully supports the prototyping process within a team design environment, including sophisticated check-in/check-out features that track source code changes and manage version control.

Sun ONE Grid Engine by Sun Microsystems is a full-featured distributed resource management tool that controls very large numbers or groups of compute jobs. Compute jobs are submitted to the "Master Host," which matches job requirements to available resources for maximum throughput of the entire workload. This results in a nearly full utilization of all compute resources (systems, tool licenses, and so on). and an overall reduction in time-to-market, because engineers can focus on other design tasks while their jobs are queued and run automatically.

The SpeedGate DSV Flow Advantage

Today, ASIC verification consumes 30 to 70 percent of total ASIC design time. With costs for a 0.18-micron ASIC mask set exceeding $500,000, the financial impact of a silicon re-spin is substantial, if not prohibitive. Thus, budgetary and time-to-market pressures require a solution that reduces the verification effort, maintains a high level of accuracy, and delivers the product at or under budget.

The objective of Mentor Graphics' SpeedGate DSV tool is to convert an ASIC or SoC design to a functionally equivalent hardware prototype that can operate at a speed comparable to testing within the actual operating environment. Many observers consider such hardware-assisted verification the only emerging technology that can realistically impact the verification bottleneck. The availability of high-capacity, high-performance Xilinx FPGAs makes the SpeedGate DSV methodology a valid approach. Combined with other hardware such as bonded-out cores or memory, Xilinx FPGAs are interconnected on a PCB with other specialized hardware to duplicate the functionality of the ASIC or SoC at orders of magnitude faster than virtual simulations.

Multiple Distributed Processing of Compute-Intensive Operations

Unlike other prototyping development systems, the SpeedGate DSV flow allows design modules and processes to be synthesized independently of each other, in any order (Figure 1), rather than synthesizing the complete design as a single job. Consequently, this methodology allows synthesis jobs to be simultaneously spread among several workstations and/or servers, as well as licenses.

To utilize these distributed processing capabilities, the SpeedGate DSV software tool includes integrated support for Sun ONE Grid Engine software, which allows compute-intensive operations such as synthesis to be distributed across clusters of workstations and servers. This offers a number of additional benefits, such as job history tracking, simple resubmission of jobs, and job progress monitoring. Additionally, the SpeedGate DSV product's interface to Sun ONE Grid Engine software is easily expandable to other compute-intensive tasks, such as place and route. As a result, productivity is greatly increased, because the total time spent on compute-intensive tasks is significantly reduced.

Integrated Support, Job Grouping, and Automatic Prioritizing

The SpeedGate DSV tool interfaces to Sun ONE Grid Engine software via a Perl script named submit2grid. Developed by the SpeedGate DSV developers, submit2grid is included with all releases of SpeedGate DSV software, and can run from the command line or from the SpeedGate DSV GUI.

The submit2grid script takes an input file with executable commands (such as the .scr file exported for synthesis by the SpeedGate

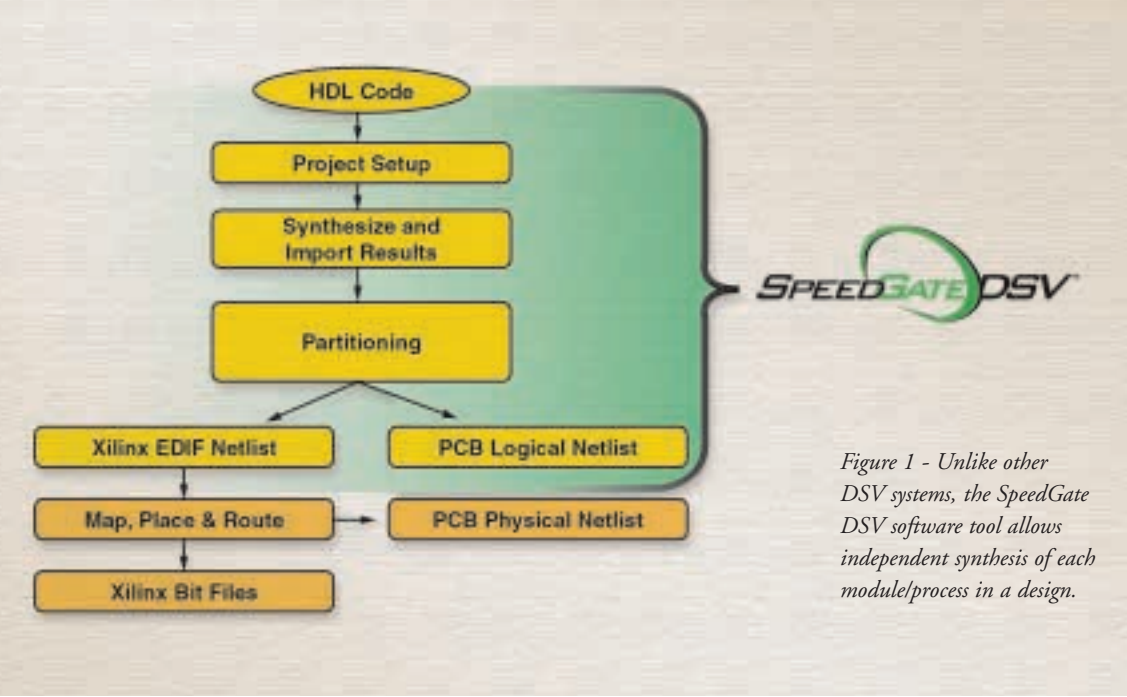

Figure 1 - Unlike other DSV systems, the SpeedGate DSV software tool allows independent synthesis of each module/process in a design.

METHOD	NUMBER OF JOBS	COMPLETION TIME (minutes:seconds)
One Sun Fire 280R Server (2x750MHz, 4GB RAM)	Submitted as one single top-level job	64:00
One Sun Blade 1000 Workstation (2x750MHz, 1GB RAM)	352 jobs serially run on one workstation	48:53
submit2grid (no grouping)	352 individual Sun ONE Grid Engine jobs	21:27
submit2grid -group 8	44 grouped Sun ONE Grid Engine jobs (eight jobs/group)	07:22
submit2grid -gen_opt 20 -group 9	40 Sun ONE Grid Engine jobs: three standalone jobs submitted first 37 grouped jobs (eight jobs/group)	04:26

Table 1: Benchmark Results/Performance Improvements

DSV tool) and then distributes the commands within that file among the execution hosts defined in a grid network using the Sun ONE Grid Engine software qsub command. submit2grid supports many arguments, including any valid qsub options, which allow for different submission conditions. In addition, submit2grid creates a log file that records such job submission details as submission start time, the name of the temp directory in which command files are stored, output log filename, ID number, and completion time.

A powerful feature of the submit2grid script is that it allows several jobs to be grouped into a single job. This feature, invoked with the -group flag, is particularly useful when a design contains many modules that synthesize individually very quickly (less than three seconds each). Submitting these fast-running jobs in groups improves the turnaround time for a design's complete synthesis because the number of submitted jobs is reduced; therefore, the job setup procedures for Sun ONE Grid Engine software are not constantly repeated over a short period of time.

SpeedGate DSV's submit2grid has a related flag, -gen_opt, which provides an advanced level of job grouping control. The -gen_opt flag creates a groups_options file that lists all jobs and specifies whether they are to be submitted individually or as part of a group. This groups_options file can be automatically generated or user-created and modified. When automatically generated, a job's previous run time history is compared to a user-defined time threshold to determine whether it should be grouped or not. If a job's previous run time exceeds this threshold, it will be individually submitted before grouped jobs. Prohibiting long-running jobs from being included in groups results in significant performance improvements for the synthesis turnaround time of a complete design.

Benchmark Results/Performance Improvements

For benchmarking purposes, the modules from Sun Microsystems' picoJava™ CPU design were synthesized in a relatively small Sun ONE Grid Engine cluster grid. The cluster grid comprised seven Sun Workstations configured to run a total of ten Sun ONE Grid Engine job slots with running ten simultaneous tool licenses.

Those results were then compared to results obtained by synthesizing the same design without distributed processing. Results are dependent on many factors and will most likely vary from run to run. Some of the basic factors that can influence the execution time of a job include compute grid design and set up; the number of CPUs allocated to the compute grid; the amount of physical memory available to the CPUs; the loading of grid resources at execution time; and the number of available tool licenses.

If SpeedGate DSV's flow did not allow for individual module synthesis, the entire design would have to be synthesized as a single job. The first row of Table 1 records how long a single job would take to synthesize with our benchmark design. The second row shows a small improvement when running individual module synthesis serially on one workstation, without taking advantage of distributed processing. The third and fourth rows illustrate the difference when taking advantage of the SpeedGate DSV software tool's distributed processing capabilities, while the fifth row shows the performance improvement obtained when using the submit2grid script with all optimizing options.

Using the SpeedGate DSV tool's distributed processing capabilities results in dramatic performance improvements. With the -group and -gen_opt options enabled, run times were almost 15 times faster than running the synthesis as a single top-level job, and more than 10 times faster than running serially on a single workstation.

Conclusion

The SpeedGate DSV tool's flexible synthesis methodology, which allows a design's modules to be synthesized separately and independently, results in great performance improvements when coupled with Sun ONE Grid Engine software. Faster module synthesis leads to an increase in productivity, a decrease in verification costs, and ultimately faster time-to-market because the prototyping flow is accelerated through distributed processing and automation. Combining this interface with the capacity, performance, and flexibility of the latest generation of Xilinx FPGAs creates a powerful environment for a prototyping flow.

For more Information, please visit *www.mentor.com/speedgatedsv/* or *www.sun.com/software/gridware/*.