Platform FPGA SystemIO Solution

Enabling the Emerging High-speed Connectivity Standards

Higher I/O performance to meet the growing demand for communications bandwidth.

by Peggy Abusaidi
Product Marketing Manager
peggy.abusaidi@xilinx.com

Traditional system interfaces, such as the existing PCI and VME parallel bus schemes, cannot keep up with today's bandwidth requirements. Therefore many new I/O and communications standards, including RapidIO, HyperTransport™, InfiniBand™, 3GIO and others, have been developed to solve the I/O bottleneck challenges. Figure 1 illustrates the variety of applications that drive the need for more bandwidth.

How do you choose the right I/O interface standards for your systems, and how do you keep current with the evolving I/O standards? In addition, how do you meet your time-to-market and cost goals with minimal risk, while the interface standards rapidly evolve? The Xilinx® Platform FPGA SystemIO solution solves the I/O bottleneck problem by giving you the ability to implement designs using the latest I/O standards. You can accelerate your time to market and be assured that your designs will remain current as the I/O standards evolve. The Xilinx Platform FPGA SystemIO solution fully addresses all aspects of system connectivity in high-performance designs.

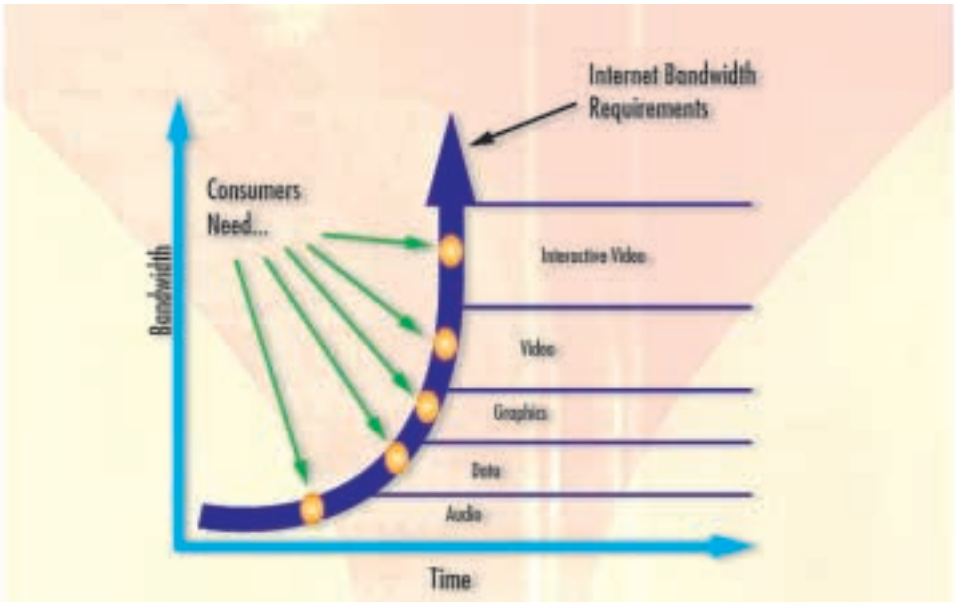

Figure 1- Internet bandwidth trend

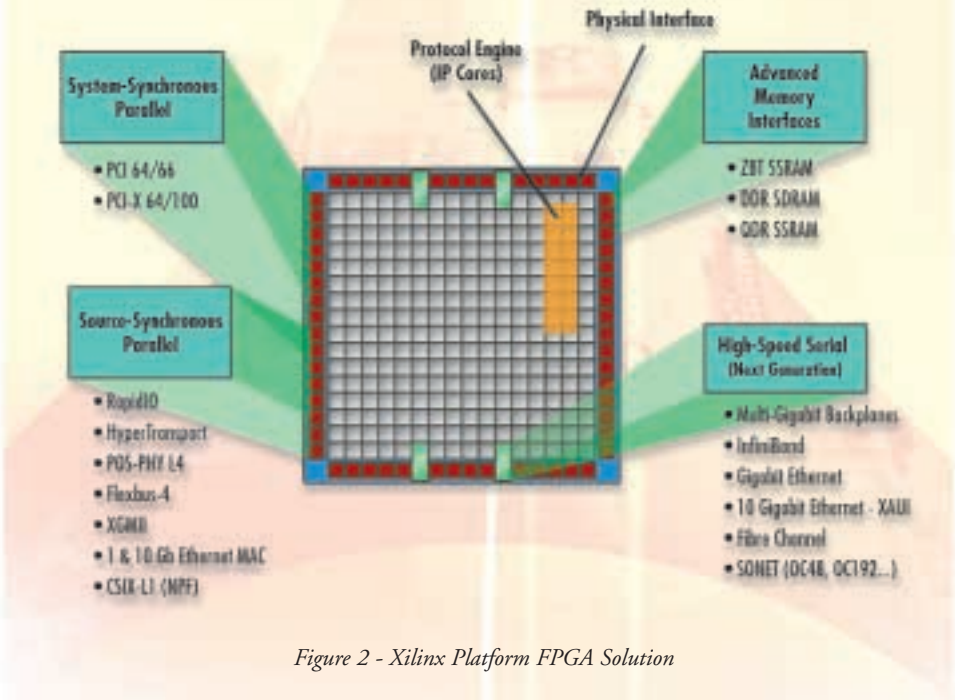

Figure 2 - Xilinx Platform FPGA Solution

The Bandwidth Problem

Today, most computer, embedded processing, and telecommunications equipment is parallel-bus oriented. However, as device performance increases, and demand for bandwidth rises, these multi-drop bus structures are reaching their performance limitations. Plus, in most cases, only a single module can use these buses at a time, with the obvious result that other subsystems on the bus are temporarily idle, waiting for bus access.

The industry's response has been the development of a host of new interconnection schemes; some with data transfer rates exceeding 10 Gbps. The new proposed standards have backers like Intel, AMD, Microsoft, Compaq, Dell, HP, Xilinx, and Sun Microsystems. They have names like RapidIO, XAUI, HyperTransport, and InfiniBand. Other standards already in use, or evolving toward higher levels of performance, include POS-PHY4, Ethernet, and various optical ATM formats like OC-12, OC-48, and OC-192. These new or evolving standards cover all architectural environments such as motherboards in chip to chip communication, backplanes for communications between subsystems, and Storage-, Local-, and Wide-Area Networks (SANs, LANs, and WANs).

The parallel standards are divided into two general categories:

- System-Synchronous Parallel – the venerable PCI family of buses, including PCI-X and Compact PCI.
- Source-Synchronous Parallel – RapidIO, HyperTransport, SPI-4 / Flexbus-4, POS-PHY 3, and others.

Because these standards are new and subject to change, FPGAs are the ideal way to ship a product without fear of obsolescence. Plus, the ability to use IP cores that implement these complex and timing-critical busses gives you a fast, risk-free method to address a rapidly changing market.

Clearly, the challenges you face are greater than ever. Not only are product life cycles shorter, simple evolutionary product steps are no longer sufficient with the multitude of standards hitting the market. When you consider that most of these standards are not final, the challenge to get your product right on the first iteration is daunting. That's why the ability to rapidly change your design to meet changes in the standards and markets is incredibly valuable. Further, the ability to leverage your design efforts with pre-engineered, supported IP Cores allows you to create more functionality in less time that ever before.

The SystemIO Solution

The Xilinx Platform FPGA SystemIO solution uses the unique Virtex-II SelectI/O™ Ultra to provide the fastest and most flexible electrical interfaces available. Each user I/O pin is individually programmable for 19

single-ended I/O standards or six differential I/O standards, including LVDS, SSTL, HSTL, and GTL+. The SystemIO solution is capable of delivering 840 Mbps LVDS performance using dedicated Double Data Rate (DDR) registers. Furthermore, any two I/O pins can be used as a differential pair, providing maximum board layout flexibility.

Using Virtex-II 840 Mbps LVDS performance and an abundance of memory and logic resources, you can easily create designs using 1GE and 10GE MAC, PCI and PCI-X, POS-PHY Level 3 and 4, RapidIO, HyperTransport, and Flexbus-4. Free reference designs for implementing interfaces such as LVDS and CSIX are available from the Xilinx website.

Table 1 shows the SystemI/O summary.

With the variety of interface reference designs and cores available in the SystemIO solution, you can easily customize your application. Figure 3 shows a 10 Gigabit Ethernet LAN/WAN line card example in which several Platform FPGA SystemIO solutions are used to provide seamless interfaces to external PHYs and Network processors. All of these interfaces are pre-engineered by Xilinx for easy drop-in functionality, enabling you to reduce your design cycle time.

Core	Standard Compliance	Aggregate Bandwidth	I/O Bus	Availability
POS-PHY L3	OIF-SPI3-01.0 Saturn POS-PHY L3	2.48 Mbps 104 MHz	32b	Now
POS-PHY L4	OIF-SPI4-02.0 Saturn POS-PHY L4	11.2 Gbps	16b LVDS 700 Mbps per LVDS pair 350 MHz DDR	Now
Flexbus-4	OIF-SPI4-01.0 AMCC Flexbus-4	12.8 Gbps	64b HSTL 200MHz	Now
10 Gb Ethernet MAC w/ XGMII	IEEE P802.3ae draft D3.1	10 Gbps	32b XGMII HSTL 312.5 MHz DDR	Now
XGMII Reference Design	IEEE P802.3ae draft D3.1	10 Gbps	32b XGMII HSTL 312.5 MHz DDR	Now
RapidIO PHY	RapidIO Interconnect Specification v1.1	8 Gbps	8b LVDS 500 Mbps per LVDS pair 250 MHz DDR	Now
PCI 64/66	PCI Spec V2.2	528 Mbps	64b 3.3V PCI	Now
PCI-X 64/100	PCI-X Spec V1.1	800 Mbps	64b 3.3V PCI-X	Now
CSIX Reference Design	CSIX-L1	6.4 Gbps	32b HSTL 200 MHz	Now
HyperTransport Single-Ended Slave	HyperTransport V1.01a	3.2 Gbps	8b LVDS 400 Mbps per LVDS pair 200 MHz DDR	Q1 '02
1 Gb Ethernet MAC	IEEE 802.3z	1 Gbps	GMII	Now

Table 1 - Platform FPGA SystemIO solution summary

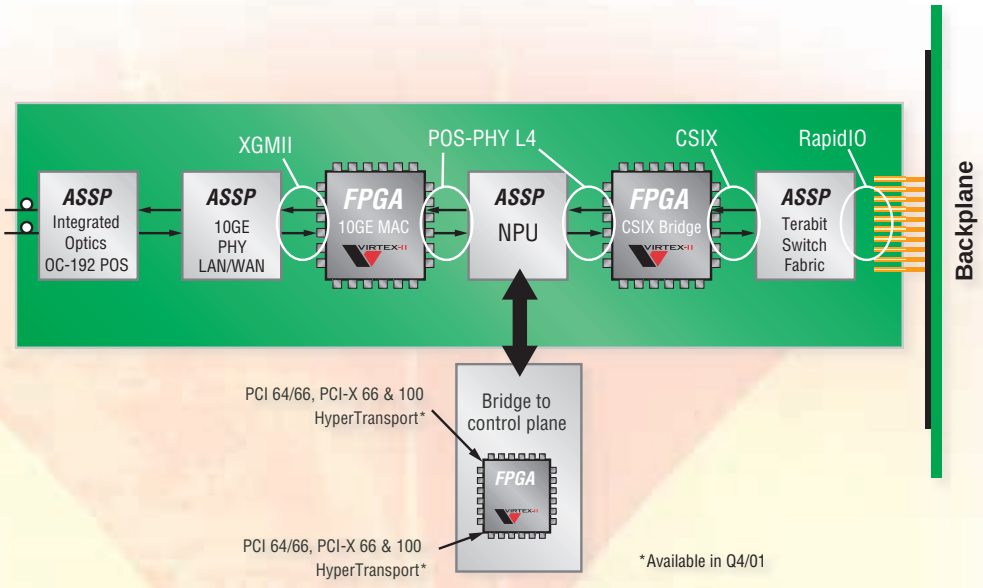

Figure 3 - 10-Gigabit Ethernet LAN/WAN card application example

In the future, we will incorporate Mindspeed's Skyrail™ 3.125 Gbps IO technology into our next generation Virtex-II family to provide support for Gbps interfaces such as 10GE, 3rd Generation IO (3GIO), Infiniband, XAUI and Fibre Channel.

Conclusion

The flexibility and high performance of the Virtex-II SelectI/O Ultra technology combined with the proven pre-engineered LogiCORE™ cores provide the complete connectivity solution to address the high speed challenges of tomorrow's networking and telecom systems. For more information go to: *www.xilinx.com*