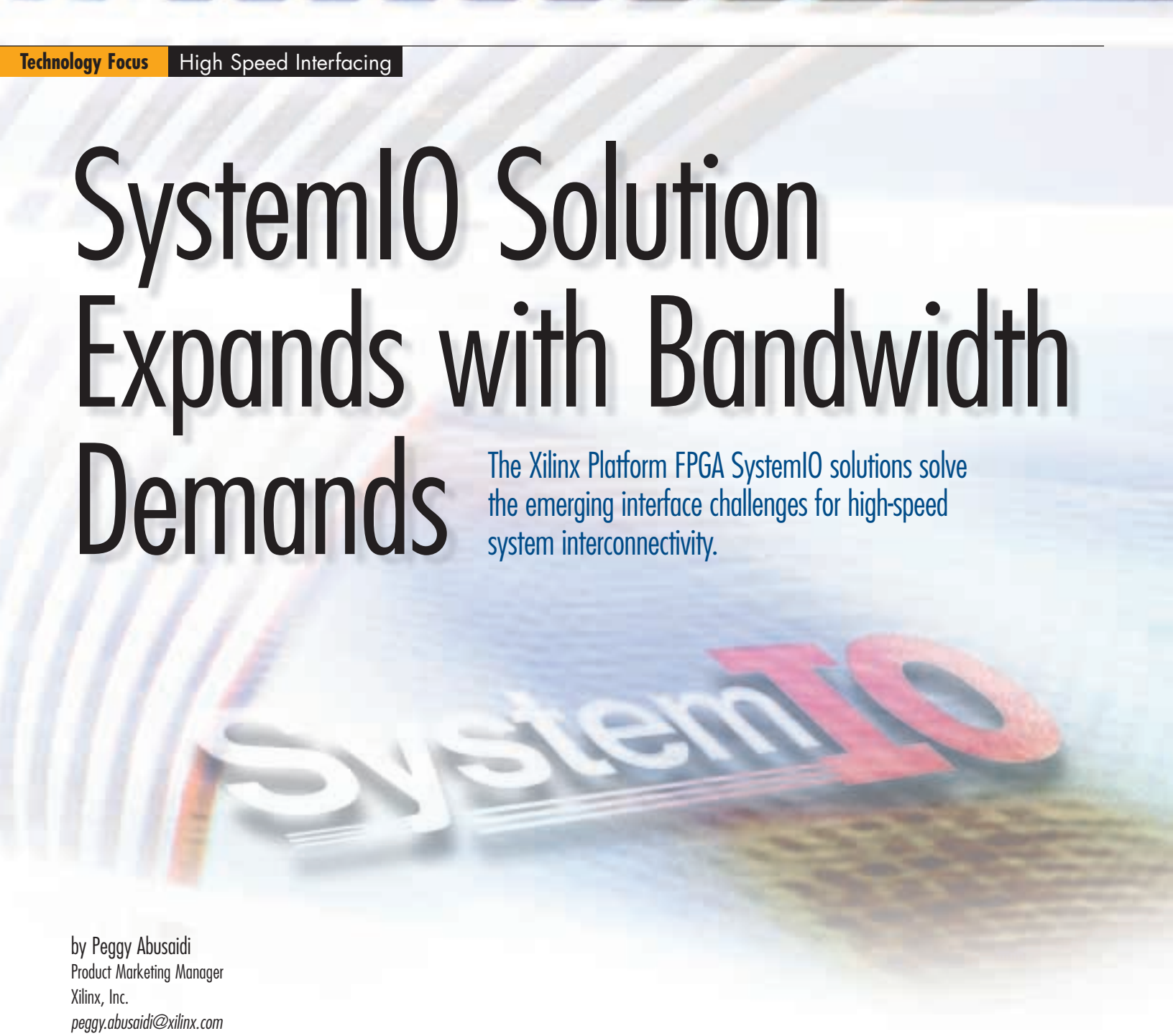
SystemIO Solution Expands with Bandwidth Demands

The Xilinx Platform FPGA SystemIO solutions solve the emerging interface challenges for high-speed system interconnectivity.



by Peggy Abusaidi
Product Marketing Manager
Xilinx, Inc.
peggy.abusaidi@xilinx.com

Traditional system interfaces, such as the existing PCI and VME parallel bus schemes, cannot keep up with today's ever-growing bandwidth requirements. Therefore, RapidIO™, HyperTransport™, InfiniBand™, PCI Express™ (aka 3GIO), and other high-speed bus interconnect technologies have been developed to open the I/O bottleneck. Figure 1 illustrates the variety of Internet applications that drive the need for more bandwidth.

How do you choose the right I/O interface standards for your systems now – and how do you keep current with the evolving I/O standards in the future? Moreover, how do you meet your time-to-market and cost goals with minimal risk when the interface standards keep changing?

As shown in Figure 2, Xilinx provides a comprehensive list of Platform FPGA SystemIO Solutions to help you solve the I/O bottleneck problem. SystemIO gives you the ability to implement designs using any of the latest I/O standards. By using a Xilinx Platform FPGA with a SystemIO solution, you can accelerate your time to market and be assured that your designs will remain current even as I/O standards evolve and specifications change. In addition, SystemIO solutions enable you to "future-proof" your products by allowing to you update the code in the FPGA to bring your product up to compliance – even after the product has been deployed in the field.

Solving the Bandwidth Problem

Today, most computer, embedded processing, and telecommunications equipment are parallel bus-oriented. However, as device performance increases, and demand for bandwidth rises, these multi-drop bus structures are reaching their performance limits. In most cases, these buses can only process one module at a time. This results in idle time for the subsystems waiting for bus access, thus decreasing overall system performance.

The industry's response has been the development of a host of new interconnection schemes, some with data transfer rates exceeding 10 Gbps. The new proposed standards have backers like Intel, AMD, Microsoft, Hewlett-Packard (Compaq), Dell, Xilinx, and Sun Microsystems. In addition to the aforementioned RapidIO, PCI Express, HyperTransport, and InfiniBand technologies, other standards already in use, or evolving toward higher levels of performance, include 10-gigabit attachment unit interface (XAUI), POS-PHY Level 4, Gigabit Ethernet, and various optical ATM formats like OC-12, OC-48, and OC-192. These new or evolving standards cover all architectural environments, such as motherboards in chip-to-chip communication; backplanes for communications between subsystems; and storage, local, and wide area networks (SANs, LANs, and WANs).

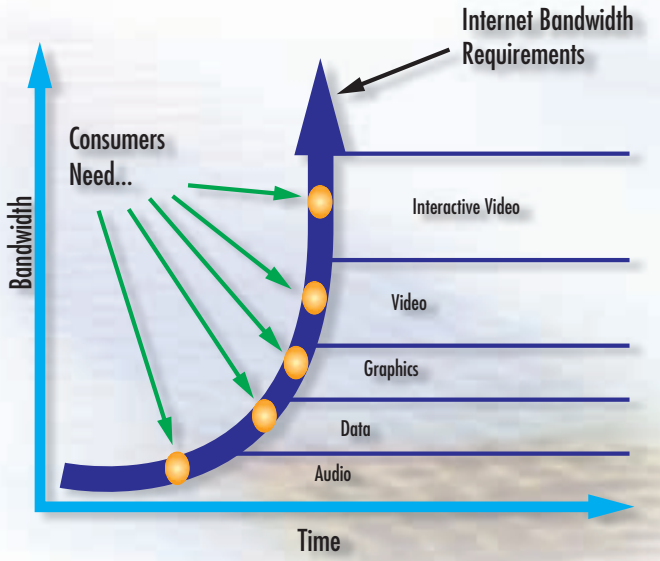


Figure 1- Internet bandwidth trend

Parallel bus standards are divided into two general categories:

- System-Synchronous Parallel – the venerable PCI family of buses, including PCI-X and Compact PCI.
- Source-Synchronous Parallel – RapidIO, HyperTransport, Flexbus 4, POS-PHY Level 3/4, and other protocols.

Because these standards are new and subject to change, FPGAs are the ideal way to ship a product without fear of obsolescence. Plus, the ability to use Xilinx LogiCORE™ intellectual property (IP) cores that implement these complex and timing-critical buses gives you a fast, risk-free method to address a rapidly changing market.

Clearly, the challenges you face are greater than ever. Not only are product life cycles shorter, simple evolutionary product steps are no longer sufficient with the multitude of standards hitting the market. When you consider that most of these standards are not final, the challenge to get your product right on the first iteration is daunting. That's why the ability to rapidly change your design to meet changes in the standards and markets is incredibly valuable. Further, the ability to leverage your design efforts with pre-engineered, pre-verified, and supported LogiCORE IP cores allows you to create more functionality in less time than ever before.

The SystemIO Solution

The Xilinx Platform FPGA SystemIO Solution uses the unique Virtex™-II SelectI/O™-Ultra blocks to provide the fastest and most flexible electrical interfaces available. Each user I/O pin is individually programmable for 19 single-ended I/O standards or six differential I/O standards, including LVDS, SSTL, HSTL, and GTL+. The SystemIO solution is capable of delivering 840 Mbps double data rate (DDR) and 644 MHz single data rate (SDR) LVDS performance. Furthermore, any two I/O pins can be used as a differential pair, providing maximum board layout flexibility and reducing overall system cost by saving both component and board layer costs.

Using Virtex-II 840 Mbps LVDS performance and an abundance of memory and logic resources, you can easily create designs using 1GE (Gigabit Ethernet) and 10GE MAC, PCI and PCI-X, POS-PHY Levels 3 and 4, RapidIO, HyperTransport, and Flexbus 4 protocols. Free reference designs for implementing interfaces, such as SFI-4, XSBI, XGMII, and CSIX are available from the Xilinx website. Table 1 shows the Platform FPGA SystemIO Solutions Summary, including both IP cores and reference designs.

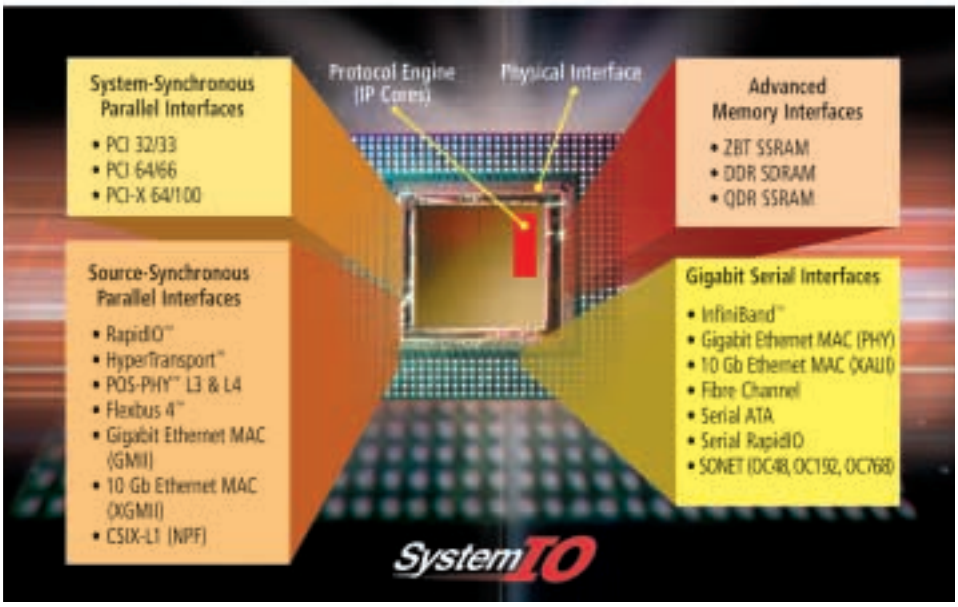


Figure 2 - Xilinx Platform FPGA SystemIO Solutions

With the variety of interface reference designs and cores available in the SystemIO solution, you can easily customize your application. Figure 3 shows a 10 Gigabit Ethernet LAN/WAN line card example in which several Platform FPGA SystemIO solutions are used to provide seamless interfaces to external PHYs and network processors. All of these interfaces are pre-engineered by Xilinx for easy drop-in functionality, enabling you to reduce your design cycle time.

With our recent introduction of the Virtex-II Pro™ Platform FPGA, we have incorporated Mindspeed's SkyRail™ architecture to embed up to 16 Rocket I/O™ 3.125 Gbps multi-gigabit transceivers (MGTs), the highest number of MGTs in a single programmable device. This breakthrough technology supports all the popular emerging serial I/O standards, including the PCI Express, InfiniBand, XAUI, and Fibre Channel protocols.

The combination of SkyRail architecture and SelectI/O-Ultra technology supplies a comprehensive list of popular parallel and serial interface IP cores in the overall SystemIO solution. Additionally, both 1GE and 10GE MAC IP cores are available with both parallel and serial interface options.

Conclusion

Platform FPGA SystemIO solutions enable Xilinx to provide you with the ultimate connectivity platform to connect and bridge interface requirements for your next-generation data communication systems.

A terabit system can simultaneously contain multiple interface requirements, including both emerging serial I/O protocols, as well as established parallel I/O standards. The new Virtex-II Pro Platform FPGA is ideally suited to help you address interface challenges by providing Rocket I/O MGTs for serial connectivity and SelectI/O-Ultra technology for parallel connectivity.

Combining LogiCORE IP cores for protocols and data processing, along with design tools and third-party partnerships, Xilinx provides the complete system connectivity solution for today's – and tomorrow's – high speed designs.

IP Core	Standard Compliance	Aggregate Bandwidth	Performance	SelectI/O Bus	Availability
POS-PHY L3	OIF-SPI3-01.0 Saturn POS-PHY L3	2.48 Gbps	104 MHz	32b 3.3V CMOS	Now
POS-PHY L4	OIF-SPI4-02.0 Saturn POS-PHY L4	12.8 Gbps	800 Mbps per pair 400 MHz DDR	16b LVDS	Now
Flexbus 4	OIF-SPI4-01.0 AMCC Flexbus 4	12.8 Gbps	200 MHz	64b HSTL	Now
Flexbus 4 to POS-PHY L4 Bridge	OIF-SPI4-01.0 AMCC Flexbus 4 OIF-SPI4-02.0 Saturn POS-PHY L4	11.2 Gbps	200 MHz (Flexbus 4 side) 350 MHz DDR (PL4 side)	64b HSTL (Flexbus 4 side) 16b LVDS (PL4 side)	Now
1GE MAC w/ GMII	IEEE 802.3-2000	1 Gbps	125 MHz	8b 3.3V GMII	Now
1GE MAC w/ PCS-PMA	IEEE 802.3-2000	1.25 Gbps	1.25 Gbps	1 channel of Rocket I/O Transceiver	Now
10GE MAC w/ XGMII	Designed to IEEE P802.3ae draft 4.1	10 Gbps	156.25 MHz DDR	32b XGMII HSTL	Now
10GE MAC w/ XAUI	Designed to IEEE P802.3ae draft 4.1	12.5 Gbps	3.125 Gbps per channel	4 channels of 3.125 Gbps Rocket I/O Transceivers	Now
RapidIO PHY	RapidIO Interconnect Specification v1.1	8 Gbps	500 Mbps per pair 250 MHz DDR	8b LVDS	Now
PCI64	PCI Spec V2.3	264 -528 MBps	33/66 MHz	64b 5/3.3V PCI	Now
PCI32	PCI Spec V2.3	132 -264 MBps	33/66 MHz	32b 5/3.3V PCI	Now
PCI-X 64/100	PCI-X Spec V1.0a	800 MBps	66/100 MHz	64b 3.3V PCI-X	Now
HyperTransport Single-Ended Slave	HyperTransport V1.01a	6.4 Gbps	800 Mbps per pair 400 MHz DDR	8b HT I/O	Q3 '02
CSIX Reference Design	CSIX-L1	6.4 Gbps	200 MHz	32b HSTL	Now
XGMII Reference Design	Designed to IEEE P802.3ae draft 4.1	10 Gbps	156.25 MHz DDR	32b XGMII HSTL	Now

Table 1 - Summary of Platform FPGA SystemIO solutions

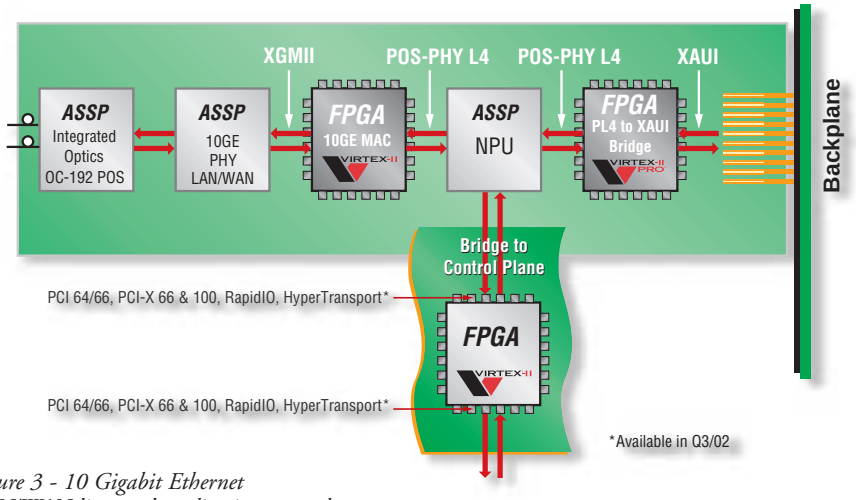


Figure 3 - 10 Gigabit Ethernet LAN/WAN line card application example