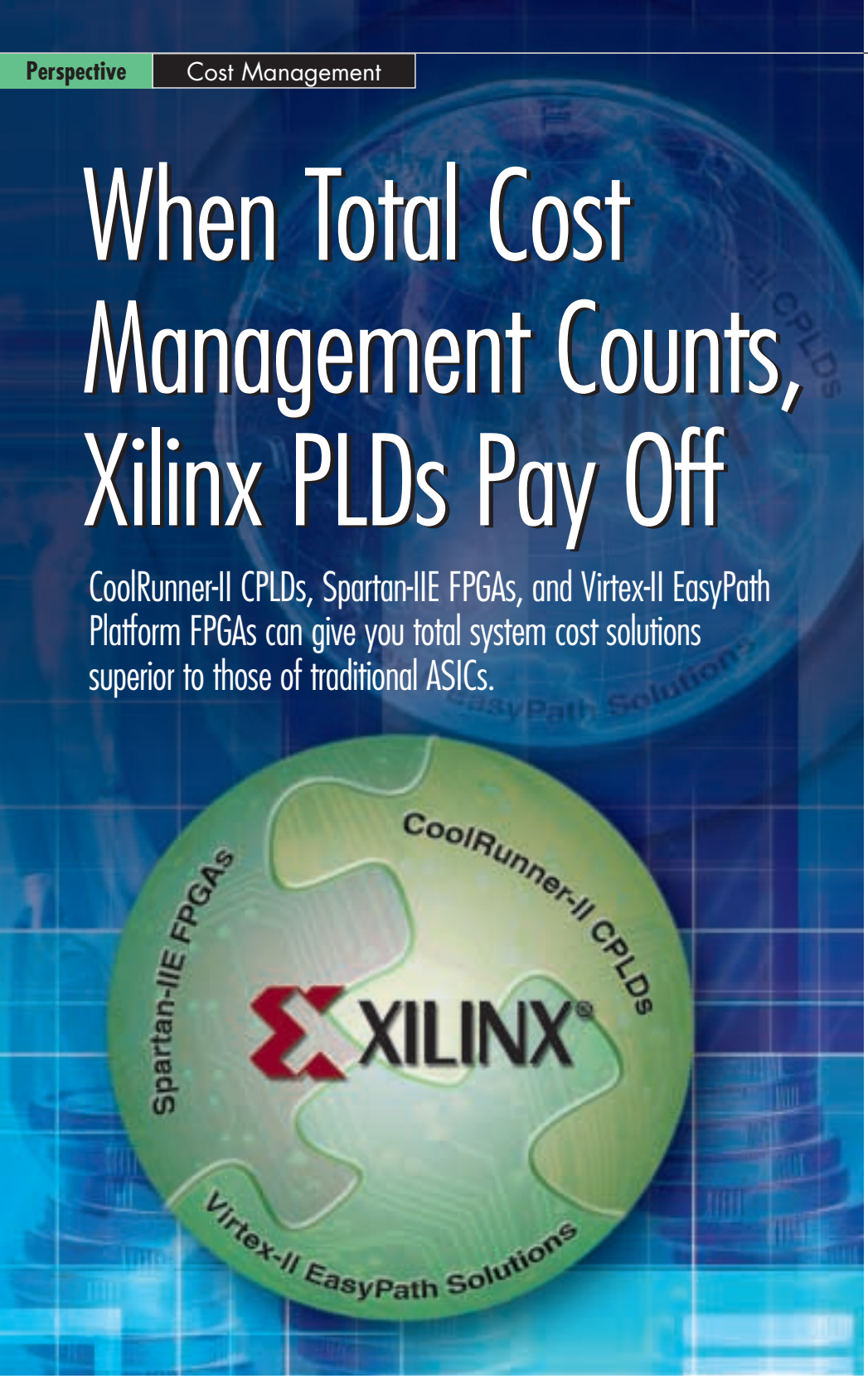
When Total Cost Management Counts, Xilinx PLDs Pay Off

CoolRunner-II CPLDs, Spartan-IIE FPGAs, and Virtex-II EasyPath Platform FPGAs can give you total system cost solutions superior to those of traditional ASICs.



by Eric Thacker
Manager, Product Solutions Marketing
Xilinx, Inc.
eric.thacker@xilinx.com

Rapidly changing markets and new technologies are subverting traditional system design paradigms. Historically, in electronic systems development, the standard design procedure was to prototype a system using programmable logic devices (PLDs), and then redesign the system using ASICs as soon as possible for cost reduction. The idea was to leverage the flexibility and development time advantage of programmable logic until the design stabilized and then to convert the design to a lower-unit-cost ASIC to reduce overall system cost.

In the past, programmable logic was lower density, lower performance, and more limited in capabilities. When systems followed traditional product life cycle behavior, the PLD-to-ASIC design strategy worked quite well. In fact, in some market segments, characterized by relatively mature technologies, established standards, and a stable competitive environment, this strategy is still optimal today.

In dynamic, rapidly changing markets, however, this strategy becomes questionable. For many advanced electronic products – such as plasma televisions, home networking hardware, and digital audio/video equipment – the market is anything but stable. Baseline standards for advanced products are ever-changing, features demanded by customers shift constantly, new technological capabilities are continually being introduced, and competitors are always trying to gain a better market position – resulting in many short-lived products.

These volatile market pressures give a significant competitive advantage to flexible and first-to-market products. In these markets, ASICs – with their long lead times, high initial costs, high minimum order quantities, higher risks, and inflexibility – are not a compelling solution.

Therefore, many designers are tapping into programmable logic's benefits of instant reprogrammability, short lead times, greatly improved performance, expanded densities, and overall flexibility. Indeed, today's programmable logic devices offer many of the same features found in ASICs. Clock management, embedded processors, high-performance DSP, advanced interfacing, and a plethora of intellectual property (IP) cores all make today's PLDs strong candidates for a system's core logic.

With their emphasis on cost-optimization, the CoolRunner™-II CPLDs, Spartan™-IIE FPGAs, and Virtex-II EasyPath™ Solutions families from Xilinx bring these advanced benefits to your high volume applications.

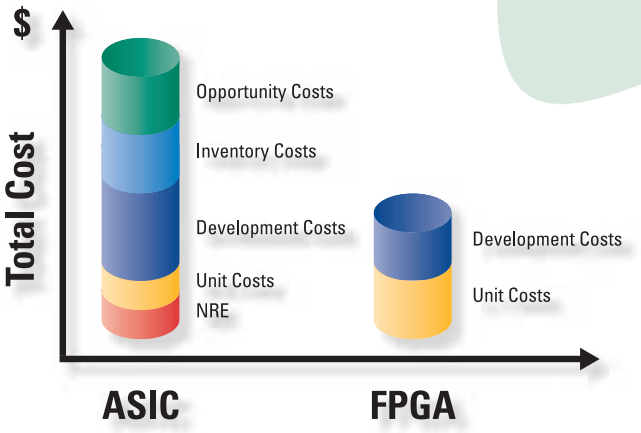


Figure 1 - Cost comparison of ASICs and FPGAs

Total Cost Solution

In the past, the primary motivation in converting a PLD design to one based on an ASIC was unit cost. ASICs, in general, are available at lower unit cost than PLDs. But looking at unit costs alone could actually lead to an overall higher cost solution. That is because unit costs are only one of the factors that contribute to total system cost. Total system costs can be broken down into three broad categories – design and development, production, and life cycle.

Design and Development

Design costs are primarily worker-hour and non-recurring engineering (NRE) costs. PLD designs require fewer worker hours, because design/debug changes can be made instantly, hardware and software can be developed concurrently, test vector generation is unnecessary, and product lead times are practically zero compared to ASICs. PLDs have no NRE costs, which can be a very important consideration as production volumes per design revision are much lower in rapidly evolving markets. In many cases, Xilinx offers free PLD design tools, thus increasing the PLD cost advantage.

There are also lost opportunity costs associated with ASICs. Systems using ASICS lose market penetration due to long development times. Furthermore, the inflexibility of ASIC-based systems prevents upgrading products to meet changing market needs. Overall, PLD design cost advantages alone can often outweigh any ASIC unit cost advantage.

Production

Unit cost is the most obvious cost in this category. ASICs usually do hold the unit cost advantage over PLDs, but this cost differential is shrinking.

Today's PLDs have aggressively driven down both die size and package costs to provide a persuasive ASIC alternative. The advanced system capabilities of modern PLDs allow designers to integrate discrete component functions into the PLD – reducing board and total component costs.

Finally, unlike an inflexible ASIC, one line of PLDs can be inventoried to supply multiple applications. You can reprogram and redeploy PLDs as needed. Combined with much lower minimum order quantities, PLDs reduce inventory costs, as well as the risk of obsolescence, further offsetting PLDs' unit cost disadvantage. See Figure 1.

Life Cycle

Life cycle costs are probably the least considered costs when designing an electronic system, but they can have a significant impact on the total return from a given design. Using PLDs instead of ASICs means practically no risk of obsolete inventory, because standard-product PLDs can be redeployed to different applications as needed. Unlike ASICs, PLDs do not have to be scrapped if a specific product is cancelled.

In addition, because PLDs can be reprogrammed, it is possible to upgrade products in the field simply by downloading a new hardware configuration file to the PLD. Bug fixes and feature upgrades can be performed remotely without changing any hardware.

Finally, long-lived legacy products using ASICs can face the need for board redesign should the ASIC product or process be discontinued. PLD reprogrammability avoids this problem. Thus, legacy products with PLDs do not siphon design resources from next-generation products, and this presents a significant market cost savings.

As illustrated in the discussion of these three cost categories, we must look beyond unit cost when deciding on logic solutions based on cost. In many applications, the unit cost savings of ASICs are more than offset by the lower risks, design, production, and life cycle costs of PLDs.

Xilinx Solutions for Total Cost Management

Xilinx has taken the lead among PLD suppliers in providing low risk, low cost, high performance logic solutions for today's rapidly changing and highly competitive markets.

Low Power, Low Density: CoolRunner-II CPLDs

CoolRunner-II RealDigital CPLDs combine high performance, ultra low power, low cost, and integration of specialized capabilities to bring you a new class of programmable logic devices. The versatility and low cost of CoolRunner-II CPLDs allow them to serve a multitude of logic, interface, and control functions. See Figure 2.

Figure 2 - CoolRunner-II CPLDs deliver high performance at low cost.

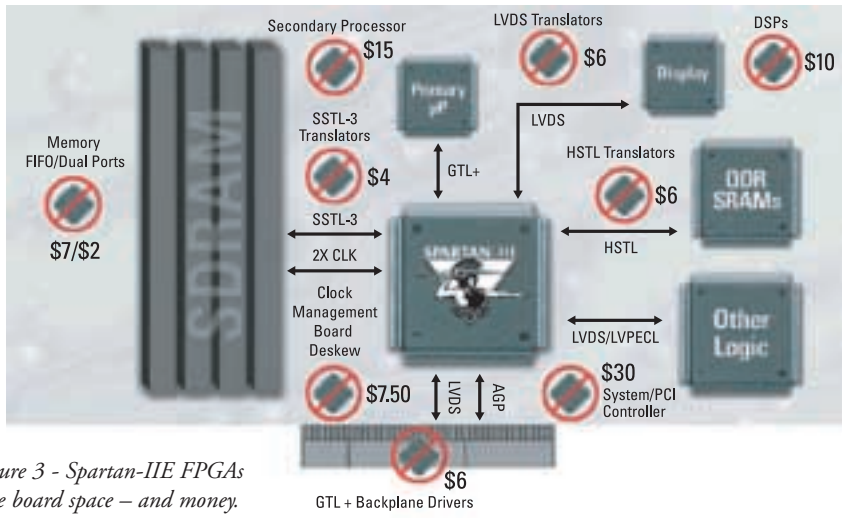


Figure 3 - Spartan-IIE FPGAs save board space – and money.

The 0.18-micron CoolRunner-II family utilizes second-generation Fast Zero Power™ technology for low power, high performance operation. These RealDigital CPLDs feature an all-digital core that eliminates power-hungry analog sense amplifiers. The CPLDs also offer increased capabilities, higher performance, and lower cost – with no performance penalty.

Available in densities from 32 to 512 macrocells, the CoolRunner-II family provides performance over 330 MHz, with standby power consumption of less than 100 µA. CoolRunner-II devices also deliver advanced system features that enable the integration of costly discrete system functions into a single reprogrammable device. This integration results in lower costs, further power reduction, increased reliability, faster time to market, and smaller designs. These system features include superior I/Os, advanced clocking features, and four levels of design security.

The in-system reprogrammable nature of CoolRunner-II CPLDs allows designers to change designs on the fly, correct designs, and test out alternate designs without changing any hardware. This saves significant engineering change orders (ECOs) and NRE charges compared to ASIC solutions.

The CoolRunner-II CPLDs' advanced I/O interface capabilities include DataGATE, a programmable on/off switch for power management; advanced interfaces such as HSTL, and SSTL; and Schmitt trigger inputs for input signal conditioning. All of these features reduce the need for external components, reducing part costs and board space.

To further reduce system costs and the need for additional components, the CoolRunner-II family provides a unique feature called CoolCLOCK. CoolCLOCK is a combination of a clock doubler and clock divider. The incoming clock is divided by two and then doubled at the output to maintain the same performance, while reducing the internal power consumption.

To increase your cost management advantage, Xilinx provides a free Internet-based ISE WebPACK™ design tool suite and a free WebFITTER™ design fitting tool to give you a complete, pushbutton design solution.

The combination of advanced interfacing, integrated system features, and free design tools makes CoolRunner-II CPLDs a compelling choice for logic functions in cost-sensitive applications. For more information, visit *www.xilinx.com/coolrunner2*.

Moderate Density, System Integration: Spartan-IIE FPGAs

Cutting-edge consumer electronics markets demand products that provide performance and flexibility in a cost-optimized format for home networking equipment, home theater systems, and other high-end personal electronic devices. These consumer products must accommodate rapidly evolving standards, shifting demand patterns, highly fluid competitive positioning, and the continuous introduction of new capabilities. Logic requirements for these designs include moderate density, advanced system features, predesigned and verified IP blocks, and high-quality design tools. Spartan-IIE FPGAs meet all of these requirements and more.

Xilinx designed its next-generation Spartan-IIE consumer FPGA with total cost management in mind. Spartan-IIE FPGAs range in density from 50,000 system gates to 300,000 system gates. To reduce FPGA component costs, Spartan-IIE FPGAs are produced by the industry's most advanced foundry process on 300 mm wafers. This process lowers die cost and enables advanced, low-cost packaging.

To reduce board cost and improve system performance, Spartan-IIE FPGAs have a number of built-in advanced system features that allow you to eliminate costly discrete translators and commodity chips from your boards, as shown in Figure 3.

Advanced interfacing – including LVDS, LVPECL, HSTL, and SSTL – remove the need for specialized interface components on the board. Furthermore, Spartan-IIE FPGAs offer four delay-locked loops (DLLs) for advanced clock management. Spartan-IIE FPGAs also contain both parameterizable block RAM (single or dual port) and distributed RAM (scalable and adjacent to logic). All these features can speed the design process, provide design flexibility, reduce design worker hours, deliver very high levels of performance, and accelerate time to market.

As consumer products increase their digital capabilities, digital signal processing (DSP) capability has become a critical performance factor. The Xilinx XtremeDSP™ initiative enables nearly one billion DSP multiply-and-accumulates (MACs) per second per dollar of performance in Spartan-IIE devices – delivering advanced DSP without the need for specialized board components.

Xilinx offers more than 200 Spartan-family IP cores to speed logic design and reduce engineering resources needed to complete the system. These IP cores are also opti-

mized for die area, which may permit the use of smaller density Spartan-IIE parts, resulting in further cost savings.

Additionally, the free ISE WebPACK software provides the industry's most advanced design tool platform to support the entire Spartan series.

Die and packaging, advanced system features, extensive IP offerings, enhanced flexibility – all these Spartan-IIE cost control features give you the performance, features, and time to market advantage necessary to compete in today's rapidly evolving electronics markets. For more information, visit *www.xilinx.com/spartan*.

High Performance, High Density: Virtex-II EasyPath FPGAs

The Virtex-II™ FPGA is the first embodiment of the Platform FPGA concept. Virtex-II devices deliver SystemIO interfaces to bridge emerging standards, XtremeDSP performance up to 100X conventional DSP solutions, multi-gigabit transceivers, and Empower! embedded processor technology. Together with the industry's most advanced design tools, Virtex-II Platform FPGAs offer a feature set that is unparalleled in the industry.

Virtex-II EasyPath FPGAs bring the unprecedented capabilities of the Virtex-II family to cost-sensitive applications by reducing the cost of high-density FPGA designs. Virtex-II EasyPath Solutions use the exact same FPGA silicon as the Virtex-II FPGA family, but Virtex-II EasyPath Solutions make use of a specialized testing program to verify the FPGAs for a specific customer application, resulting in higher yields and significantly lower costs.

Virtex-II EasyPath solutions provide an FPGA volume conversion strategy with no risk, no investment of customer engineering resources, and the fastest conversion time of any competing high-volume strategy for high-density FPGA designs. The main benefits of Virtex-II EasyPath solutions are:

- Lower unit costs: Customers can expect a 30-90% price reduction compared to standard FPGAs.
- Lower up-front costs: These costs can be as low as 30% of the NRE costs of an ASIC or gate array.
- No added engineering resources: Unlike other FPGA conversion strategies, Virtex-II EasyPath FPGAs require no additional engineering resources or tools. Customers are not required to contribute any resources for conversion, verification, qualification, or board redesign.
- No risk: Virtex-II EasyPath Solutions have none of the performance, timing, functionality, or architecture match risks of alternative FPGA conversion strategies, because the conversion FPGA fabric is the same as the standard Virtex-II FPGA.
- Minimal lead times: With Virtex-II EasyPath FPGAs, initial orders are filled within six weeks and restocking orders are filled within days of being placed. Compare that to lead times of multiple months for both initial and follow-on orders for alternative conversion strategies.

Because Virtex-II EasyPath FPGAs are tested for a specific design configuration, testing throughput and yields are significantly higher, thus driving down the unit costs of the FPGA, as shown in Figure 4. You can initially design your system using standard Virtex-II FPGAs. Once the design has stabilized, you can use Virtex-II EasyPath Solutions to convert to a lower-cost platform with none of the risk, lower NRE costs, and none of the additional engineering resources required by conversion to ASICs. For more information, visit *www.xilinx.com/virtex2*.

Conclusion

From low density, ultra low power CoolRunner-II CPLDs to mid-range, low cost Spartan-IIE FPGAs to high density Virtex-II EasyPath Platform FPGA Solutions, Xilinx presents a portfolio of products that can play a critical role in your total cost management of system design. These advantages include:

- Cost-optimized silicon and packaging to minimize unit costs
- Advanced system features to reduce costs through system integration
- Reprogrammability to streamline design and debug
- No-cost system upgrade capabilities
- Reduced risk of obsolete inventory
- An extensive IP library to improve design efficiency and reduce system components
- Free design tools that maximize design efficiency.

Together, Xilinx CPLDs and FPGAs give you cost-optimized for managing system costs while maximizing system performance, functionality, and flexibility. Σ

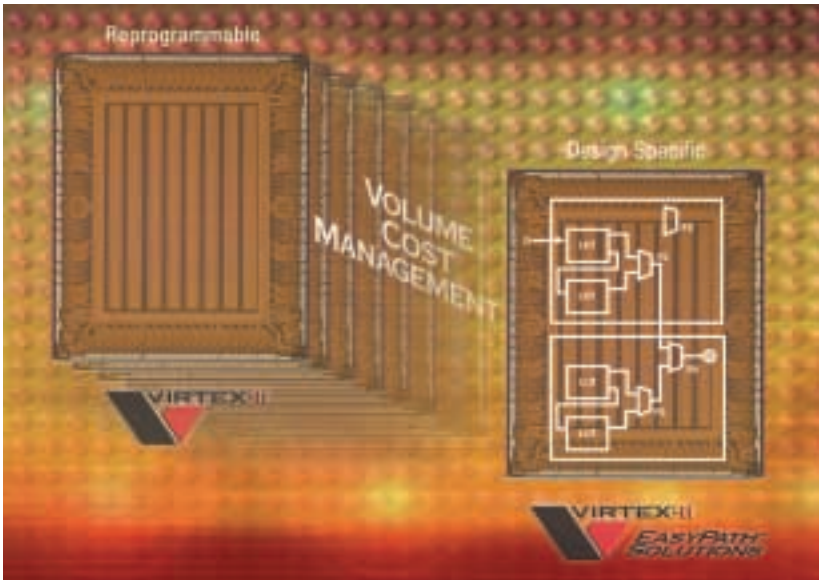


Figure 4 - Virtex-II EasyPath Solutions are design-specific and cost-effective.