New Virtex-II Pro Devices — Increased Capability, Lower Cost

Now you get programmable system features at programmable logic prices.

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In a significant move, Xilinx recently expanded the Virtex-II Pro™ Platform FPGA family two ways:

- Five new devices offering increased capability
- Lower cost versions for the entire family in a new reduced-speed series.

With this, the new Virtex-II Pro family expands to ten devices, and sets industry records in every conceivable category, providing the advanced system-level features and high performance you need, at remarkably low prices.

The new Virtex-II Pro FPGA solution, illustrated in Figure 1, provides everything you need, on a single, reprogrammable device, including:

- The world's highest logic and memory density
- The world's highest I/O capacity
- The world's fastest DSP capability
- The world's fastest multi-gigabit serial I/O connectivity
- The world's most flexible parallel I/O connectivity
- The world's only embedded processing FPGA solution using IBM® PowerPC™ processor cores.

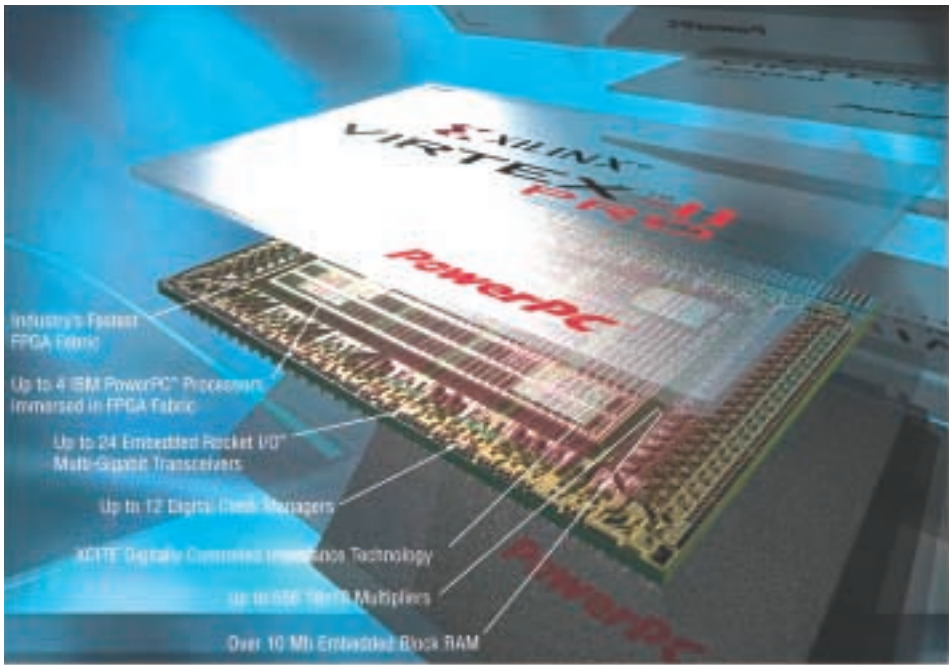

Figure 1 - Virtex-II Pro Platform FPGA

Your demands, both for increased capability as well as lower cost versions of our Virtex-II Pro devices, were made clear at our Programmable World 2002 event. And now, we can deliver the performance and the pricing you need due to the success of our initial devices and development tools, as well as advances in our process technology which includes 300-mm wafers.

These new, lower cost devices not only deliver tremendous cost savings over comparable competing programmable device offerings, but they also bring Virtex-II Pro capabilities within the reach of a much wider range of applications. With the Virtex-II Pro family you now get multiple IBM PowerPC processors and multi-gigabit serial transceivers at about the same cost as our Virtex-II™ FPGAs (which don't offer these features), effectively providing programmable system features at programmable logic prices.

The Highest Performance and the Lowest Cost

The new Virtex-II Pro XC2VP125 FPGA, shown in Table 1, is the world's highest capacity, highest performance, and highest capability programmable logic device, delivering unique system performance such as one trillion MACs/sec DSP performance and 120 Gb/s aggregate payload bandwidth. There is no programmable device in the world that competes with it in features, performance, or cost. With such unparalleled leadership advantage, the Virtex-II Pro Platform FPGAs put you on a platform of success, closer to your design goals.

Expanding the Market and Target Applications

The new -5 speed grade delivers cost-effective 2Gb/s transceiver performance, with over 266 MHz embedded PowerPC processor performance. In comparison, our fastest devices (-7 speed grade) provide up to 3.125 Gb/s transceiver performance, with over 300 MHz embedded PowerPC processor performance. The -5 speed grade is therefore ideal for medium to high-speed applications including storage, digital broadcast, networking, and wireless networking. For example, in networking, as you move from the core of the network to the edge, the line rate and processing speed of the equipment decreases while the need for intelligent processing increases. In addition, price pressure increases, because the edge equipment is more price sensitive than the core equipment. This analogy can be applied to almost any application and market segment. Xilinx is providing -5 devices specifically to address such price-sensitive applications that benefit from system features that include embedded processors and multi-gigabit transceivers.

Virtex-II Pro FPGA Architecture Review

The Virtex-II Pro family, shipping since February of this year, is the world's first 130 nm, 9-layer copper, FPGA family and the first and only one to offer integrated IBM PowerPC microprocessor technology and 3.125 Gb/s serial transceivers. Its architecture is built upon the award-winning Virtex-II FPGA fabric, which already has thousands of satisfied users.

"The Virtex brand has been the number one choice of designers worldwide, based on its industry-leading capacity, performance, capabilities, and cost-effectiveness. In each generation of families, our mission is to deliver significantly enhanced functionality while driving down prices. We continue this strategy in the Virtex-II Pro family by including state-of-the-art multi-gigabit serial transceivers and high-performance PowerPC RISC CPUs, in the standard feature set, at no charge. Thus, we enable the creation of next-generation systems designs at previously unattainable price points."

Erich Goetting — Vice President and General Manager of the Xilinx Advanced Products Division

With 10 devices, multiple packages, and multiple speed grades to choose from, the Virtex-II Pro FPGAs give you the right features and performance to meet your specific needs. The family, as shown in Table 1, includes:

- Immersed IBM PowerPC processors (0 to 4)
- Integrated 3.125 Gb/s Rocket I/O™ transceivers (0 to 24)
- The award-winning Virtex-II FPGA fabric.

IBM PowerPC Processors

Each immersed IBM PowerPC processor runs at up to 300+ MHz and 420+ Dhrystone MIPS providing high-performance embedded processing. The PowerPC processor is supported by the IBM CoreConnect™ bus technology. A complete set of embedded software tools are available to help you quickly develop and debug your PowerPC designs – through an OEM agreement, Xilinx provides software tools from Wind River Systems, customized for Virtex-II Pro FPGAs.

"With the immersion of PowerPC cores, Xilinx has developed the optimal platform to implement our storage network designs. Virtex-II Pro devices provide the critical elements of system-level design, including high-speed serial I/O, making it an ideal combination for our next generation products. Moreover, the unique architectural synthesis design environment allows us to make hardware and software tradeoffs throughout the design cycle."

Sandy Helton – Executive VP and CTO, San Valley

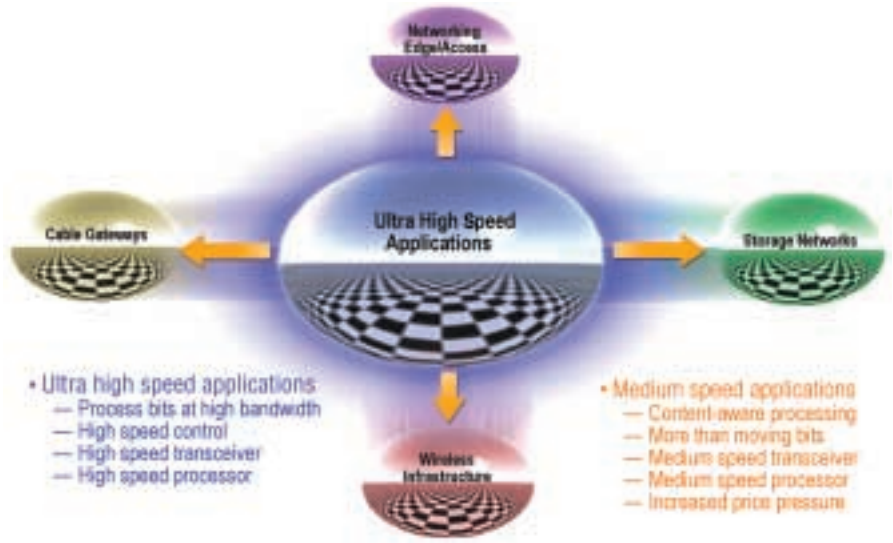

Figure 2 - Expanding the market from ultra-high speed to medium-high speed applications

Rocket I/O Multi-gigabit Transceivers

The Rocket I/O™ multi-gigabit transceivers (MGTs) are based on the Mindspeed SkyRail™ CMOS technology. Each transceiver runs at rates ranging from 622 Mb/s to 3.125 Gb/s, and includes the entire transceiver support circuitry. Each Rocket I/O transceiver consists of both a digital Physical Coding Sublayer (PCS), as well as an analog Physical Media Attachment (PMA), to provide an integrated SerDes (serializer/deserializer) function.

Award-winning Virtex-II Fabric

The Virtex-II FPGA fabric provides features for high-performance system design that has made it a platform of choice for users. These features include:

- High-performance logic with a wide choice of densities
- Embedded block RAM
- XtremeDSP embedded hardware multiply circuitry
- Advanced digital clock management circuitry
- XCITE technology for digitally controlled impedance matching on I/Os
- Bitstream encryption technology for design protection
- Flexible Select I/O™-Ultra technology for supporting over 20 single-ended and differential I/O signaling standards.

Device	XC2VP2	XC2VP4	XC2VP7	XC2VP20	XC2VP30	XC2VP40	XC2VP50	XC2VP70	XC2VP100	XC2VP125
Logic Cells	3,168	6,768	11,088	20,880	30,816	43,632	53,136	74,448	99,216	125,136
Block RAM (Kbits)	216	504	792	1,584	2,448	3,456	4,176	5,904	7,992	10,008
18x18 Multipliers	12	28	44	88	136	192	232	328	444	556
Digital Clock Management Blocks	4	4	4	8	8	8	8	8	12	12
Configuration Memory (Mbits)	1.31	3.01	4.49	8.21	11.36	15.56	19.02	25.6	33.65	42.78
IBM PowerPC Processors	0	1	1	2	2	2	2	2	2	4
Multi-Gigabit Transceivers	4	4	8	8	8	12*	16*	20	20*	24*
Max Available User I/O	204	348	396	564	692	804	852	996	1164	1200
Package										
FG256	140	140								
FG456	156	248	248							
FF672	204	348	396							
FF896			396	556	556					
FF1152				564	692	692	692			
FF1148*						804	812			
FF1517						804	852	964		
FF1704								996	1040	1040
FF1696*									1164	1200

Table 1- Virtex-II Pro Platform FPGAs Power of Choice (new -5 devices shown in red)

**Note: FF1148 and FF1696 packages support higher user I/O and zero Rocket I/O multi-gigabit transceivers*

Conclusion

The expanded Virtex-II Pro family provides a broad choice of 10 devices in scalable features and speed grades. It marks leadership in every facet, providing more capability than any other competing programmable logic device. In addition, the new pricing delivers programmable system features at programmable logic prices, making embedded PowerPC processors and multi-gigabit transceivers standard features in high-performance programmable devices. For more information on Virtex-II Pro Platform FPGAs and design resources, go to *www.xilinx.com/virtex2pro.* Σ