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A Quick JTAG ISP Checklist

Summary

In-System Programming (ISP) circuitry is beneficial for fast prototype development. However, even the most robust circuitry needs minimal consideration to deliver the best in system programming results. This application note describes a short list of considerations needed to get the best performance from your ISP designs. The list of considerations generally applies to all Xilinx ISP device families. Special considerations for Xilinx CPLDs are highlighted.

Families

XC9500/XL/XV, XC18V00, CoolRunner™, CoolRunner-II, Spartan™-II/IIE, and Spartan-XL families, as well as Virtex™ Series FPGAs and Virtex-II Series Platform FPGAs.

Overview

Charge pumps, the heart of the CPLD ISP PROM circuitry, require a modest amount of care. The voltages to which the pumps must rise are directly derived from the external voltage supplied to the VCCINT pins on the CPLD ISP PROM parts. Because these elevated voltages must be within their prescribed values to properly program the CPLD, it is vital that they be provided with very clean (noise free) voltage within the right range. This suggests the first two key rules:

1. Make sure VCC is within the range specified in the device data sheet.
2. Provide both 0.1 µF and 0.01 µF capacitors at every VCC point of the chip, attached directly to the nearest ground.

   JTAG specifications do require pull-up resistance to be supplied internally to the TDI and TMS pins by the chips, but no particular value is required. This lets vendors supply whatever they choose and still remain in full compliance. Because of this, very long JTAG chains or chains using parts from multiple vendors can present significant loading to the ISP drive cable. In these cases, it is wise to:
3. Use the latest Xilinx download cables.
4. Consider including buffers on TMS or TCK signals interleaved at various points on your JTAG circuitry to account for unknown device impedance.

   The Xilinx iMPACT downloading software is continuously being improved. With this in mind, it is appropriate to:
5. Always be certain to use the latest version of the Xilinx iMPACT software.

   In some cases, XC9500/XL/XV designs appear to experience erase time or programming time extension as the design progresses - particularly for long chains. This is probably due to the likely fact that parts being reprogrammed will have lots of switching signals delivered into them, which is different from the initial case where a blank part is being programmed. If this occurs, there is a way to lower the noise:
6. Put the rest of the JTAG chain into HIGHZ when programming a troublesome part. HIGHZ is a JTAG instruction that tristates the device I/O pins.

This will limit the number of additional signals presented both to the system and frequently to a troublesome part (because parts within a given chain tend to be connected amongst themselves). The main detail to accomplish step 6 is simply to select the HIGHZ option from the iMPACT preferences selection dialog.

7. If free running clocks are delivered into the ISP CPLD, it may be necessary to disconnect or disable their entry into the CPLD while programming.

   This is best accomplished by using the commercially available clock generation chips that permit electrical disabling of the clock output. This seldom occurs, but advanced planning makes it painless.

   Xilinx ISP devices support various JTAG I/O ranges. See the device data sheets for the JTAG I/O voltage level. Ensure JTAG I/O voltage compatibility between devices in the JTAG scan chain and the download cable.

8. Match the download cable VCC/V_{REF} power supply to the JTAG I/O levels supported in the ISP devices.

Checklist

1. Make sure VCC is within the range specified in the device data sheet.
2. Provide both 0.1 and 0.01 µF capacitors at every VCC point of the chip, and attached directly to the nearest ground.
3. Use the latest Xilinx download cables.
4. Consider including buffers on TCK and TMS interleaved at various points on your JTAG circuitry to account for unknown device impedance.
5. Always be certain to use the latest version of the Xilinx iMPACT software.
6. Put the rest of the JTAG chain into HIGHZ when programming a troublesome part.
7. If free running clocks are delivered into the ISP CPLD, it may be necessary to disconnect or disable their entry into the CPLD while programming.
8. Match the download cable VCC/V_{REF} power supply to the JTAG I/O voltage levels supported in the ISP devices.

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
04/14/00	1.0	Initial Xilinx release.
04/10/02	2.0	Revised.
06/07/02	2.1	Added "Virtex Series FPGAs" and "Virtex-II Series Platform FPGAs" to the Summary.