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Board Routability Guidelines with Xilinx Fine-Pitch BGA Packages

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Summary

Xilinx supplies full array fine-pitch BGA (Ball Grid Array) packages with 1.00 mm ball pitch. Successful and effective routing of these packages on PC boards is a significant challenge to designers. This application note provides board level routing guidelines for using Xilinx fine-pitch BGA packages. Specific examples are provided to choose appropriate routing schemes. These examples are based on package and board design rules for standard PCB technology and are not drawn to scale.

Board Level Routing Challenges

1.0 mm Ball Pitch, Fine-Pitch BGA

Xilinx fine-pitch BGA packages, (FG1156, FG900, FG676, FG456, FG256 and some newer flip-chip packages), have a full matrix of solder balls (Figure 1). These packages are made of multilayer BT substrates. Signal balls are in a perimeter format extending up to eight rows in FG676 packages and up to ten rows in FG1156 packages. Power and ground pins are grouped together appropriately.

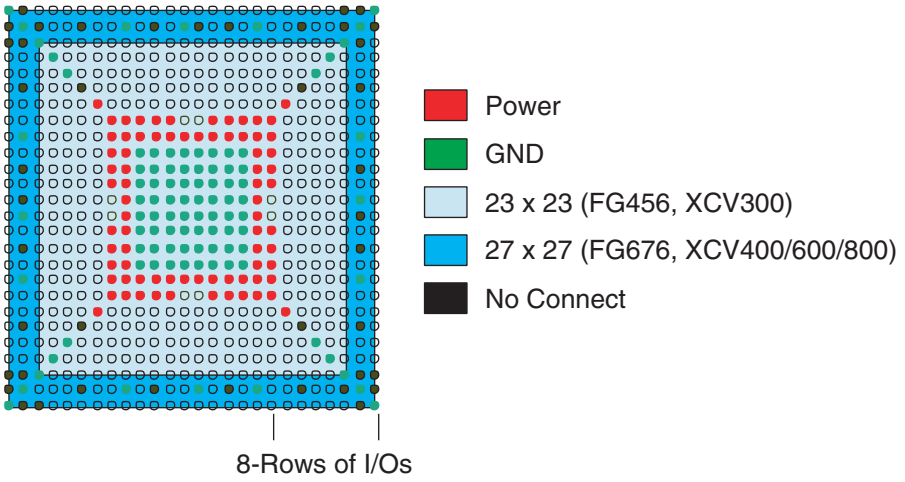


Figure 1: **Fine Pitch BGA Pin Assignments**

The number of layers required for effective routing of fine-pitch BGA packages is dictated by the layout of pins on each package. If several other technologies and components are already present on the board, the system cost is factored with every added board layer. The intent of a board designer is to optimize the number of layers required considering both cost and performance. This application note provides guidelines to minimize the required board layers for routing fine-pitch BGA products using standard PCB technologies (5/5 mils lines/space or 6/6 mils lines/space).

For high performance and other system needs, designers can use premium technologies with finer lines/spaces on the board. The pin assignment and pin grouping scheme on full array fine-pitch BGA packages enables an efficient way of routing the board with an optimum number of required board layers.

Board Routing Strategy

Minimum Requirements

The diameter of a land pad on the component side is provided by Xilinx. This information is required prior to the start of the board layout to design the board pads to match the component side land geometry. The typical values of these land pads are described in Figure 2 and summarized in Table 1.

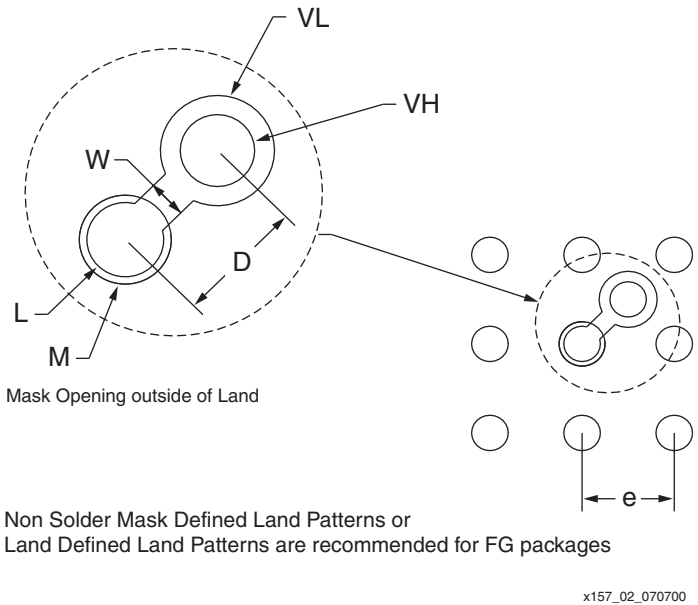


Figure 2: **Suggested Board Layout of Soldered Pads for 1.0 mm Pitch BGA**

Table 1: **Summary of Typical Values of Land Pads**

	FG256	FG456	FG676	FG680	FG860	FG900	FG1156
Component Land Pad Diameter	0.45	0.45	0.45	0.5	0.5	0.45	0.45
Solder Land (L) Diameter	0.4	0.4	0.4	0.4	0.4	0.4	0.4
Opening in Solder Mask (M) Diameter	0.5	0.5	0.5	0.5	0.5	0.5	0.5
Solder (Ball) Land Pitch (e)	1.0	1.0	1.0	1.0	1.0	1.0	1.0
Line Width Between Via and Land (w)	0.13	0.13	0.13	0.13	0.13	0.13	0.13
Distance Between Via and Land (D)	0.7	0.7	0.7	0.7	0.7	0.7	0.7
Via Land (VL) Diameter	0.61	0.61	0.61	0.61	0.61	0.61	0.61
Through Hole (VH), Diameter	0.3	0.3	0.3	0.3	0.3	0.3	0.3
Pad Array	Full	-	Full	-	-	Full	Full
Matrix or External Row	16 x 16	22 x 22	26 x 26	39 x 39	42 x 42	30 x 30	34 x 34
Periphery Rows	-	7[3]	-	5	6	-	-

Notes:
1. Dimension in millimeters.
2. 3 x 3 matrix for illustration only, one land pad shown with via connection.
3. FG456 package has solder balls in the center in addition to periphery rows of balls.

For FG series packages, NSMD (Non Solder Mask Defined) pads on the board are suggested. This allows a clearance between the land metal (diameter L) and the solder mask opening (diameter M) as shown in Figure 2. The space between the NSMD pad and the solder mask, and the actual signal trace widths depends on the capability of the PCB vendor. The cost of the PCB is higher when the line width and spaces are smaller.

Selection of the pad types and pad sizes determines the available space between adjacent balls for signal escape. Based on PCB capability, the number of lines that can share the available space is described in Figure 3. Based on geometrical considerations, if one signal escapes between adjacent balls, then two signal rows can be routed on a single metal layer. This is illustrated in Figure 3 as routing with one line/channel, either at 6 mils lines and spaces or 5 mils lines and spaces. Using this suggested routing scheme. a minimum of eight PCB layers are required to route 10 signal rows in a package.

A slightly lower trace width can be used by the inner signal rows routed in internal layers than the top and bottom external or exposed traces. Depending on the signal being handled, the practice of "necking down" a trace in the critical space between the BGA balls is allowable. Changes in width over very short distances can cause small impedance changes. Validate these issues with the board vendor and signal integrity engineers responsible for design.

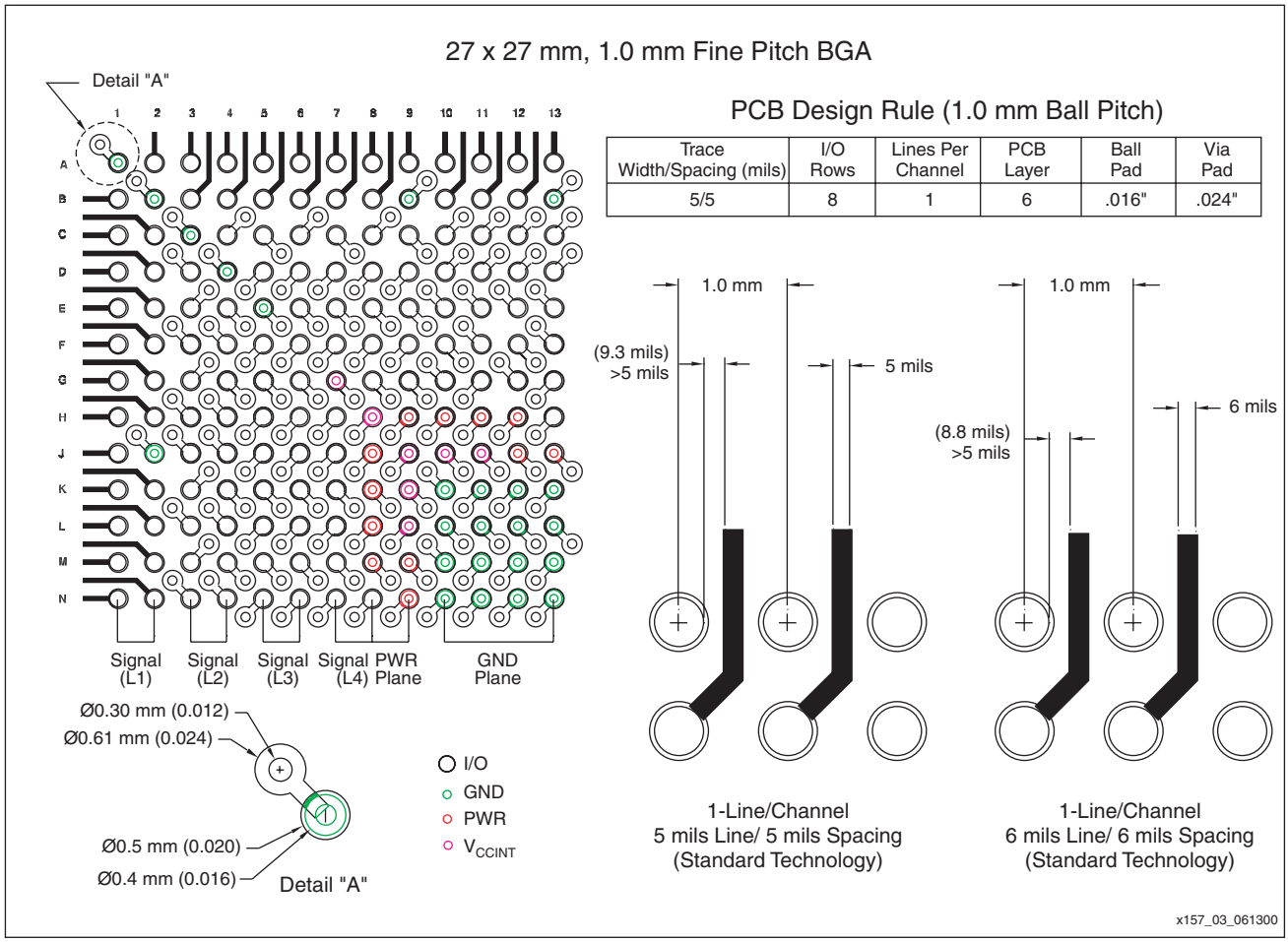


Figure 3: **FG676 PC Board Layout/Land Pattern**

Figure 3 describes a board-level layout strategy for a Xilinx 1.0 mm pitch FG676 package. Detail A in Figure 3 describes the opening geometry for the Land Pad and the Solder Mask. Routing with 5 mils lines/trace allows one signal per channel (between the balls). For successful routing, eight row deep signal traces require six PCB layers. Figure 4 shows the suggested schematic of layers for the six-layer routing scheme.

Using premium board technology such as Microvia Technology (allowing up to 4 mils lines and spaces) efficient routing is possible with a reduced number of board layers. A grouping scheme for power, ground, control and I/O pins, may also enable efficient routing.

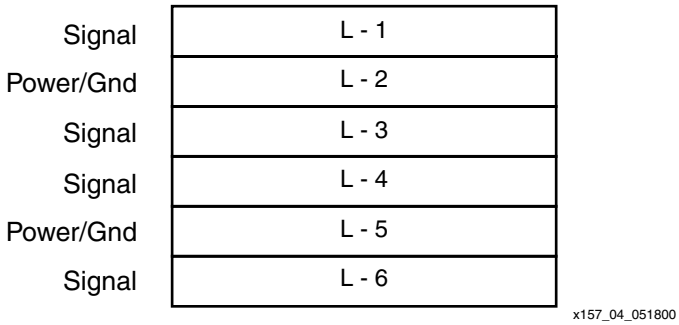


Figure 4: **Six-Layer Routing Scheme**

Figure 5 through 9 are drawings of suggested layer-by-layer board routing for the FG series 256, 456, 676, 900 and 1156 packages. These drawings assume the standard PCB technology of 5 mils lines and spaces.

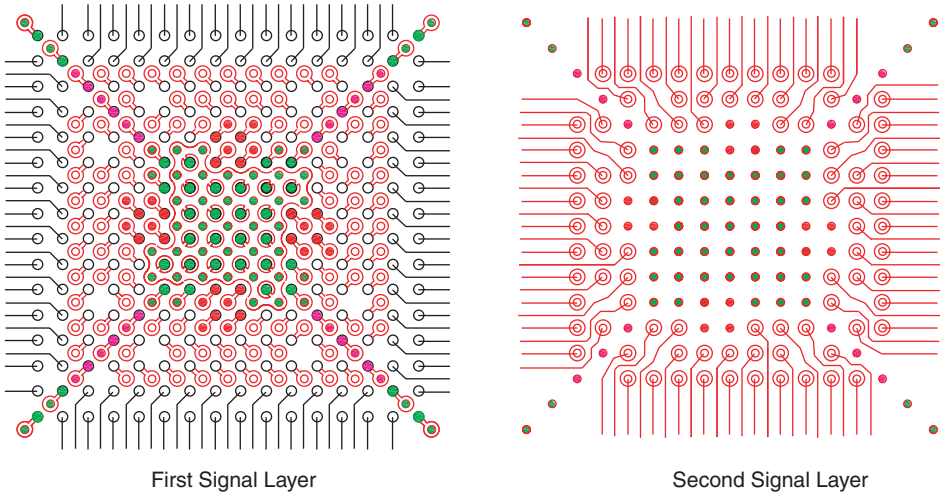
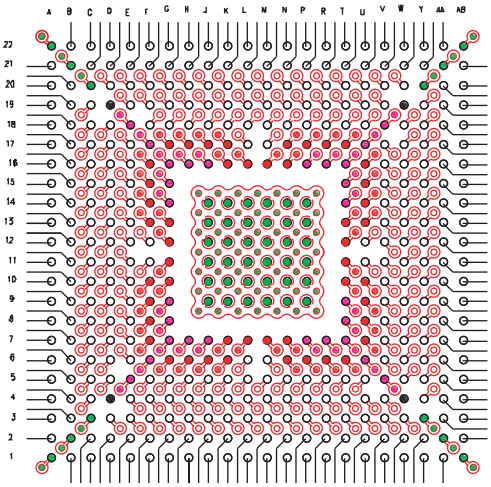
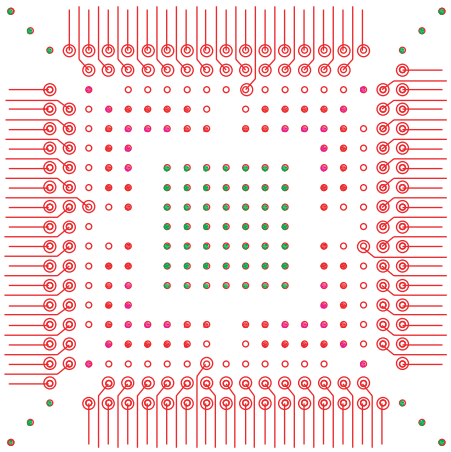


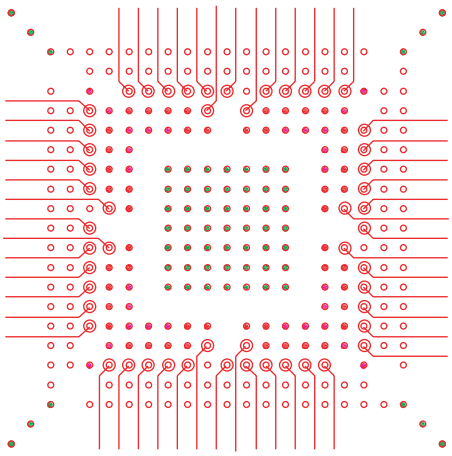
Figure 5: **XCV300E - FG256 NSMD Land Pad**



First Signal Layer



Second Signal Layer



Third Signal Layer

Notes:
1) Solder land diameter 0.4 mm Nonsolder Mask Defined.
2) Solder Mask Opening 0.5 mm diameter.
3) Via diameter 0.3 mm on 0.61 mm diameter Via Land.
4) All Layers trace width 0.127 mm.

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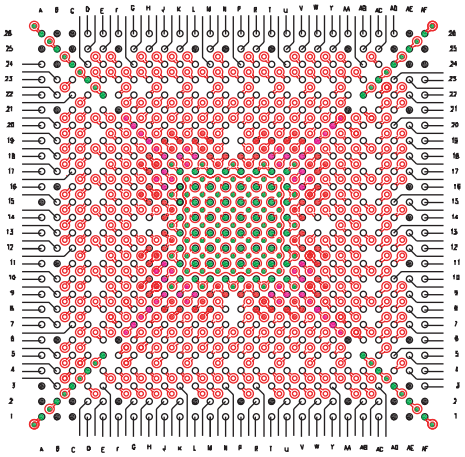
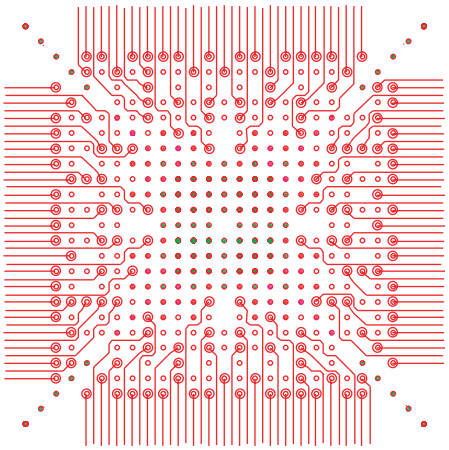
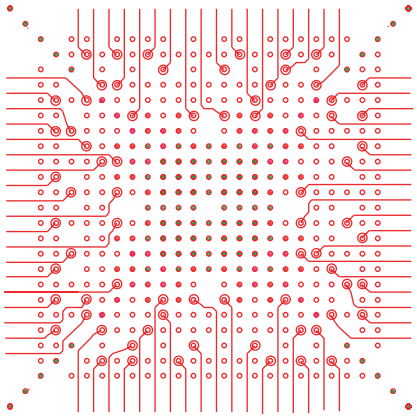
Figure 6: **XCV300E - FG456 NSMD Land Pad**



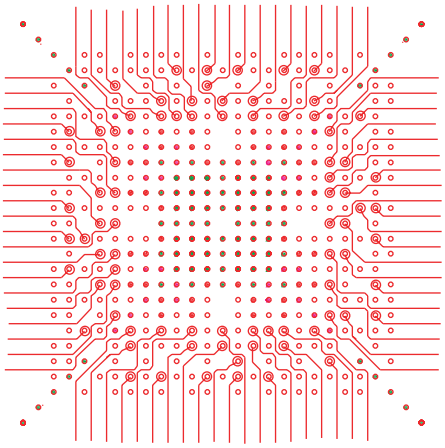
Top Signal Layer



Second Signal Layer



Third Signal Layer



Fourth Signal Layer

Notes:
1) Solder Land diameter 0.4 mm Nonsolder Mask Defined.
2) Solder Mask opening diameter 0.5 mm.
3) Via diameter 0.3 mm on 0.61 mm diameter Via Land.
4) Trace width 0.127 mm.

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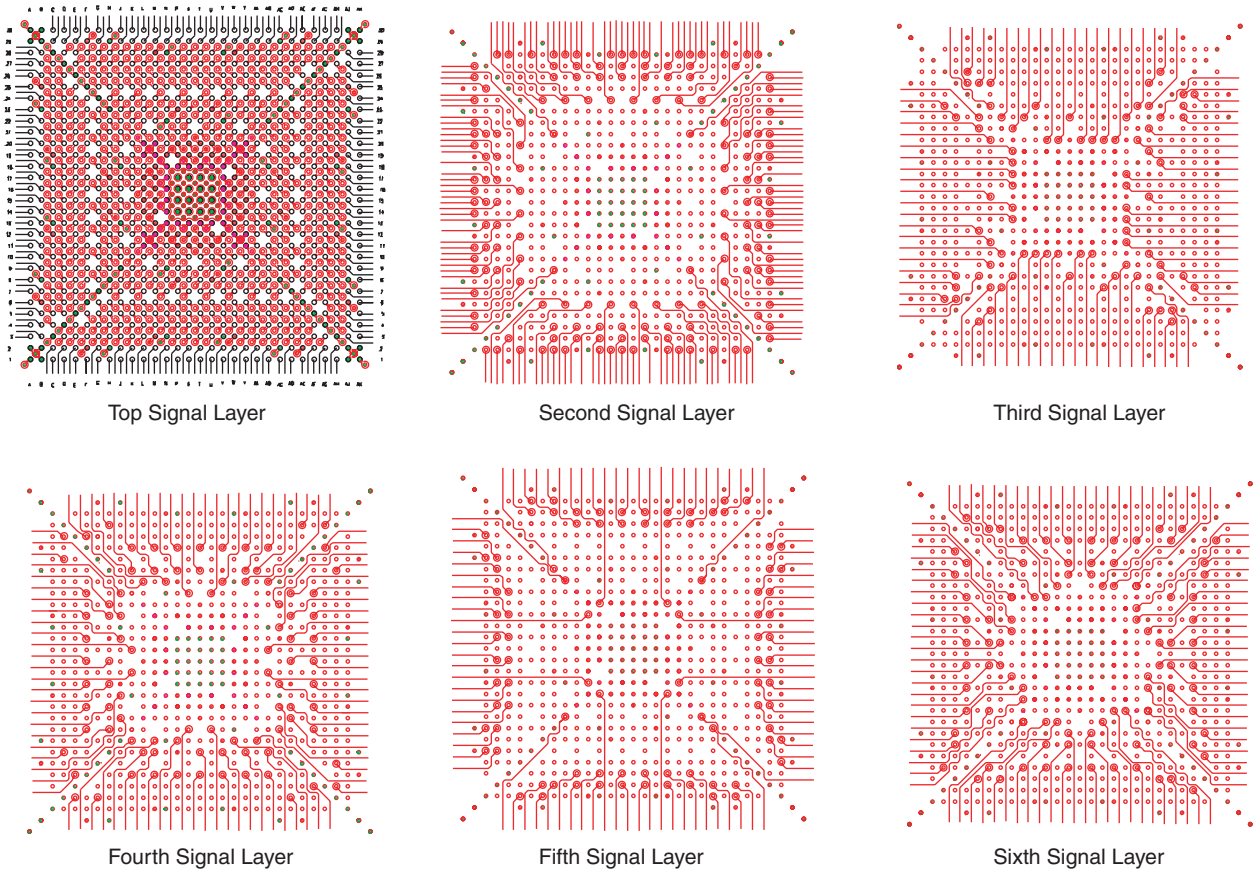
Figure 7: **XCV800 - FG676 NSMD Land Pad**



Notes:
1) Solder Land diameter 0.4 mm Nonsolder Mask Defined.
2) Solder Mask opening diameter 0.5 mm.
3) Via diameter 0.3 mm on 0.61 mm diameter Via Land.
4) Trace width 0.127 mm.

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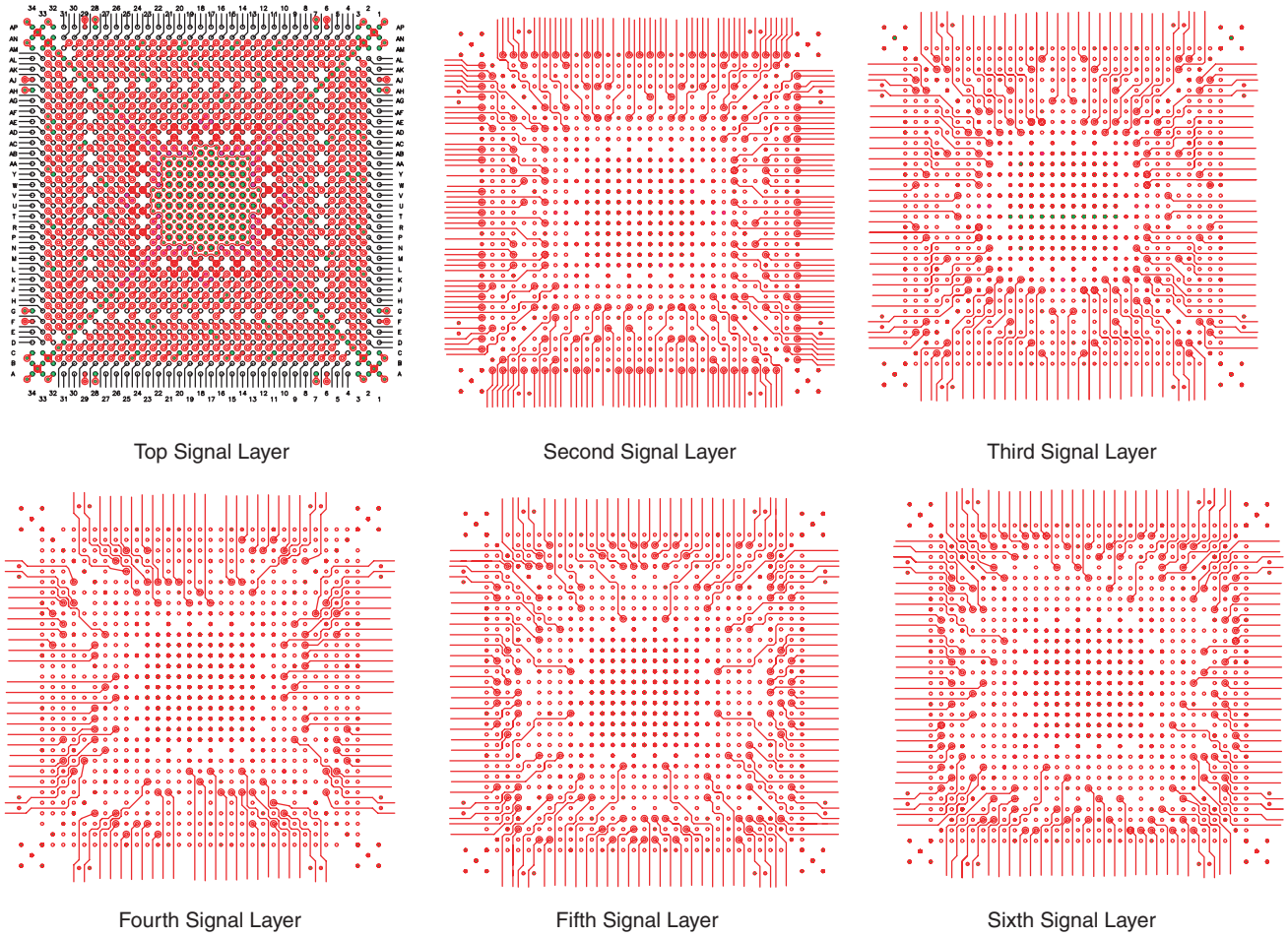
Figure 8: **XCV1600E - FG900 NSMD Solder Land Pad Layout**



Notes:
1) Solder Land diameter 0.4 mm Nonsolder Mask Defined.
2) Solder Mask Opening diameter 0.5 mm.
3) Via diameter 0.3 mm on 0.61 mm diameter Via Land.
4) All layers, trace width 0.127 mm.

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Figure 9: **XCV2000E - FG1156 NSMD Solder Land Pad Layout**

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
07/26/00	1.0	Initial Xilinx release.
04/24/02	1.1	Updated Figure 9.
11/14/02	1.2	Updated titles on a few figures.