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XC1700 and XC18V00 Design Migration Considerations (Confidential DRAFT)

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Summary

The compatibility between the XC1700™ and XC18V00™ series of PROMs allows an engineer to take advantage of the in-system reprogramming features of the XC18V00 PROM during the development phase of a project and the lower cost benefit of an XC1700 series PROM during the production phase of a project. This application note discusses the considerations for systems that support a migration path from the XC18V00 PROM to an XC1700 series PROM. The topics include package compatibility, pin compatibility, I/O voltage compatibility, power and ground connections, and Boundary Scan chain integrity.

Introduction

The XC18V00 PROM family and the XC1700 series of PROMs are simple solutions for configuring Xilinx FPGAs. They provide non-volatile storage, as well as an integrated bitstream delivery mechanism to the target FPGA(s).

The XC18V00 PROM family is an in-system programmable (ISP) PROM with many desirable features. The XC18V00 PROM supports the IEEE Boundary Scan Standard 1149.1 (JTAG). The JTAG port provides access for board testing, as well as in-system reprogramming of the PROM contents. The ISP feature is a convenient mechanism for updating FPGA designs on the desktop or through remote transports. The XC18V00 PROM supports serial and parallel modes of bitstream delivery to the target FPGA(s).

The XC1700 series of PROMs are one-time programmable (OTP) PROMs. The XC1700 series of PROMs primarily support the simple, serial bitstream delivery mode to the target FPGA(s). Some device sizes in the XC17V00 PROM family also support the parallel bitstream delivery mode to a target FPGA. The XC1700 series of PROMs provide lower-cost solutions with faster programming times, making them attractive solutions for production environments.

Many projects can take advantage of the XC18V00 ISP PROM family during the project prototyping/development phase when design updates are frequent. Compatibility between the XC18V00 ISP PROM and the XC1700 series of OTP PROMs allow migration to the lower-cost XC1700 OTP PROM for the final production stage of a project.

Feature Comparison

Several features distinguish the XC18V00 ISP PROM family from the XC1700 series of OTP PROMs. The primary difference between the XC18V00 ISP PROM and the XC1700 series of OTP PROMs is the programming support. The XC18V00 ISP PROMs are in-system reprogrammable, whereas the XC1700 series of PROMs are only one-time programmable. Table 1 lists the major features of the XC18V00 ISP PROM and the XC1700 series of OTP PROMs.

Table 1: **PROM Features**

Feature	XC18V00 ISP PROM	XC1700 series of OTP PROMs
In-system reprogrammable	Yes, via JTAG	N/A
Boundary scan test	Yes	N/A
Separate I/O power supply pin	Yes	No
Serial Output Mode	Yes	Yes
Parallel Output Mode	Yes	No (See Note 1 for exceptions)

Notes:
1. Only the XC17V08 and XC17V16 PROMs support the parallel (SelectMAP) output mode.

Recommended PROM Families for Target FPGAs

For each Xilinx FPGA, Xilinx offers an XC1700 series OTP PROM solution. Xilinx also offers an XC18V00 ISP PROM solution that is compatible to all Xilinx FPGAs. Table 2 lists the recommended PROMs for each Xilinx FPGA family.

Table 2: **Recommended PROM Families**

FPGA Family	ISP PROM Family	OTP PROM Family
Virtex-II Pro™	XC18V00	XC17V00
Virtex™-II	XC18V00	XC17V00
Virtex-E	XC18V00	XC17V00
Virtex	XC18V00	XC17V00
Spartan™-IIE	XC18V00	XC17S00A
Spartan-II	XC18V00	XC17S00A
Spartan-XL	XC18V00	XC17S00XL

See the PROM family data sheets for specific PROM recommendations for each FPGA.

Package/Pinout Compatibility

For a given package that is supported by the XC18V00 ISP PROM and the XC1700 series of OTP PROMs, the XC1700 package pinout is a subset of the XC18V00 package pinout. See Table 3.

Table 3: **XC18V00 ISP PROM to XC1700 Series OTP PROM Migration Compatibility Matrix**

PROM Family	PROM Size	XC18V00 SO20 Package	XC18V00 PC20 Package	XC18V00 PC44 Package	XC18V00 VQ44 Package
XC17V00	XC17V16	N/A	N/A	Requires 4 cascaded XC18V04s	Requires 4 cascaded XC18V04s
	XC17V08	N/A	N/A	Requires 2 cascaded XC18V04s	Requires 2 cascaded XC18V04s
	XC17V04	N/A	N/A	XC18V04	XC18V04
	XC17V02	N/A	N/A	XC18V02	XC18V02
	XC17V01	XC18V01(1)	XC18V01(1)	N/A	N/A
XC17S00A	XC17S300A	N/A	N/A	N/A	XC18V02
	XC17S200A	N/A	N/A	N/A	XC18V02
	XC17S150A	XC18V01	N/A	N/A	N/A
	XC17S100A	XC18V01	N/A	N/A	N/A
	XC17S50A	XC18V01	N/A	N/A	N/A
	XC17S30A	XC18V512	N/A	N/A	N/A
	XC17S15A	XC18V512	N/A	N/A	N/A
XC17S00XL	XC17S150XL	XC18V01	N/A	N/A	N/A
	XC17S100XL	XC18V01	N/A	N/A	N/A
	XC17S50XL	XC18V01	N/A	N/A	N/A
	XC17S40XL	XC18V512	N/A	N/A	N/A
	XC17S30XL	N/A	N/A	N/A	N/A
	XC17S20XL	N/A	N/A	N/A	N/A
	XC17S10XL	N/A	N/A	N/A	N/A
	XC17S05XL	N/A	N/A	N/A	N/A
XC1700L	XC1704L	N/A	N/A	XC18V04	XC18V04
	XC1702L	N/A	N/A	XC18V02	XC18V02
	XC1701L	XC18V01	N/A	N/A	N/A
	XC17512L	XC18V512	N/A	N/A	N/A

Notes:

1. Migration from XC18V01 to XC17V01 PROMs is supported. For some scenarios, the difference in PROM capacities may be an issue. The XC17V01 capacity is 1,679,360 bits, whereas the XC18V01 capacity is only 1,048,576 bits.
2. N/A = Not available in compatible packages or pinout is not compatible.

Timing Compatibility

When designing a system for migration between PROM families, care must be given to not exceed the maximum CLK frequency of all families under consideration for the migration path. The chosen CLK frequency is important in systems that use a fixed external CLK source. On the other hand, if the FPGA Master-Serial mode or Master-SelectMAP mode is used, the configuration CLK frequency is user selectable via the Xilinx BitGen software's ConfigRate option. Thus, the configuration rate in the Master configuration modes can be adjusted late in the design cycle to suit the PROM family.

The XC18V00 ISP PROM family supports the faster maximum configuration CLK frequencies than the XC1700 series of OTP PROMs. Table 4 shows the maximum configuration CLK frequencies for each PROM family.

Table 4: **Maximum PROM CLK Frequency**

PROM Family	Maximum CLK Frequency
XC18V00	33 MHz(1)
XC17V00	15 MHz
XC17S00A	10 MHz
XC17S00XL	10 MHz
XC1700L	15 MHz

Notes:
1. The XC18V02 and XC18V04 PROMs have a maximum CLK frequency of 20 MHz.

Power and I/O Voltage Compatibility

The XC1700 series of OTP PROMs use the same voltage supply (V_{CC}) to power the internal circuitry and I/O buffers. The families of the XC1700 series OTP PROMs span the 5V and 3.3V supply ranges. However, only the 3.3V XC1700 families of OTP PROMs can be used as drop-in replacements for the XC18V00 ISP PROMs. The 3.3V XC1700 series OTP PROMs support only 3.3V I/Os.

The XC18V00 ISP PROM is a 3.3V PROM. Although the XC18V00 ISP PROM supports a separate voltage supply (V_{CCO}) for its output buffers that can be powered at 3.3V or 2.5V, the V_{CCO} pin(s) must be tied to 3.3V for migration compatibility. The XC18V00 ISP PROM V_{CCO} pin locations are no connects in the corresponding XC1700 series OTP PROM package pins.

See Table 5 for the PROM voltage compatibility.

Table 5: **Voltage Compatibility**

PROM	Internal Voltage Supply (V_{CC})	I/O Voltage Supply (V_{CCO})	I/O Tolerance
XC18V00	3.3V	Supports 3.3V or 2.5V (Must be 3.3V for migration compatibility.)	Up to 5.5V
XC17V00	3.3V	Same as V_{CC}	Same as V_{CC} + 5%
XC17S00A	3.3V	Same as V_{CC}	Same as V_{CC} + 5%
XC17S00XL	3.3V	Same as V_{CC}	Same as V_{CC} + 5%
XC1700L	3.3V	Same as V_{CC}	Same as V_{CC} + 5%

For the Virtex Series, Virtex-II Series Platform FPGAs, and Spartan-II/IIE FPGAs, the FPGA V_{CCO} pins for banks with configuration pins are recommended to be connected to 3.3V for I/O compatibility with the Xilinx PROMs. For XC18V00 ISP PROM to XC1700 series OTP PROM

migration compatibility, the FPGA V_{CCO} pins for the banks with configuration pins must be connected to 3.3V for I/O compatibility with the XC1700 series of OTP PROMs.

A few of the XC1700 series OTP PROM families define a VPP pin. The V_{PP} pin is a voltage supply pin that has special purpose during device programming on a third-party programmer. However, on the board, the V_{PP} pin is tied to the same supply voltage as the V_{CC} pin (3.3V). The V_{PP} pin location in the XC1700 series OTP PROM packages corresponds to a V_{CC} pin on the XC18V00 ISP PROM packages. Thus, the XC1700 series OTP PROM V_{PP} pin is compatible with the XC18V00 ISP PROM V_{CC} pin connection.

Boundary Scan Integrity

Although many of the XC1700 series of OTP PROMs are drop-in compatible with the XC18V00 ISP PROMs, the XC18V00 ISP PROMs support an IEEE Boundary Scan Standard 1149.1 (JTAG) port whereas the XC1700 series of OTP PROMs do not support the JTAG port. Connections to the XC18V00 ISP PROM's JTAG port are required to access the PROM in-system for reprogramming and may optionally provide Boundary Scan test access. The pins on the XC1700 series of OTP PROMs corresponding to the XC18V00 JTAG port pins are no connects. Particular attention must be paid to the design of the JTAG connections on the board to either avoid Boundary Scan issues or maintain the Boundary Scan chain integrity after the PROM solution is migrated to an XC1700 series PROM.

The simplest solution is to put the PROMs on a separate Boundary Scan chain from the rest of the JTAG devices on the board. See Figure 1. With this architecture, the separate Boundary Scan chain can be used to access the PROMs when the PROM locations are populated with XC18V00 ISP PROMs, and conversely, the separate Boundary Scan chain can be ignored when the PROM locations are populated with XC1700 series OTP PROMs. The scan chain associated with the XC18V00 ISP PROMs can optionally be connected to the scan chain with the other JTAG devices through jumpers on the board to create a single scan chain.

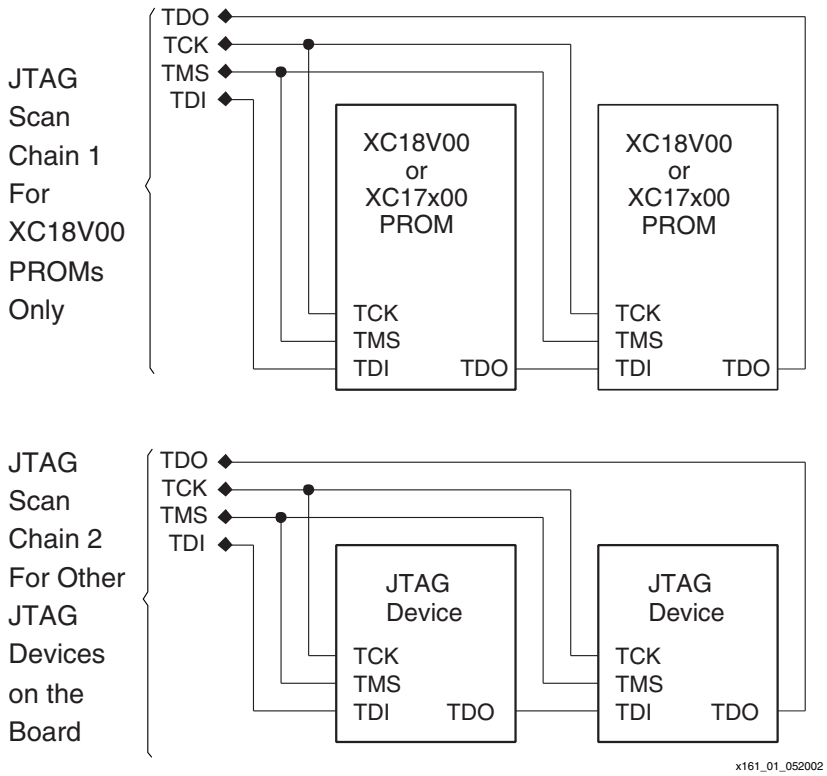

Figure 1: **Separate JTAG Scan Chain for the PROMs**

Another solution is to place jumpers on the board connecting the PROM's TDI pin to the PROM's TDO pin. See Figure 2. The jumpers should be removed when the PROM locations are populated with XC18V00 PROMs, and conversely, the jumpers should be inserted when the PROM locations are populated with XC1700 series of PROMs. This solution essentially makes the XC1700 series of PROMs transparent to the JTAG scan chain. The JTAG scan chain changes depending on the population of PROMs on the board. The change in the scan chain affects other systems that access the scan chain, e.g., Boundary Scan test systems.

Figure 2 shows that the jumpers are used to maintain Boundary Scan integrity after XC18V00 PROMs are migrated to XC1700 series PROMs.

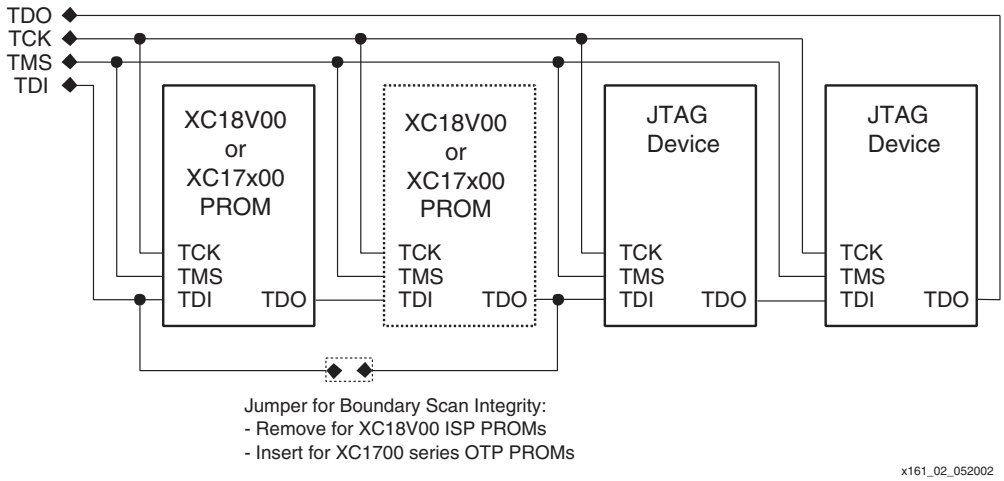

Figure 2: **JTAG Scan Chain for PROMs With Jumpers to Maintain Boundary Scan Integrity**

Special Signals

The XC18V00 CF signal is not available on the XC1700 series of PROMs. A board that will migrate from the XC18V00 to an XC1700 series PROM cannot depend on the CF signal.

The set of configuration signals for the Virtex Series SelectMAP configuration mode includes the BUSY signal. When asserted High, the BUSY signal indicates that the PROM data source should hold the current data byte until BUSY is deasserted. The XC18V00 PROMs do not support the BUSY signal, but the XC17V08 and XC17V16 PROMs do support the BUSY signal. When designing for migration, the lack of BUSY signal support in the XC18V00 PROM will limit the configuration CLK frequency to less than the frequency at which the Virtex Platform FPGAs will begin to assert the BUSY signal. See the Virtex Platform FPGA data sheet for the configuration CLK frequency at which the FPGA will begin to assert the BUSY signal.

Notes:

1. For encrypted bitstreams, the Virtex-II FPGAs may assert BUSY when the configuration CLK is as fast as 6 MHz.

Appendix - Example Board Layouts for PROM Migration

Figure 3 shows the pad locations for the pins of a PROM in an SO20 package. The board-level pad connections are shown. The layout in Figure 3 is compatible with both the XC18V01-SO20 ISP PROM and the XC17V01-SO20 OTP PROM. A few of the XC17V01-SO20 no connect NC) pins will land on pads that have connections to board-level signals. It is safe to connect the XC17V01-SO20 NC pins to these board-level signals.

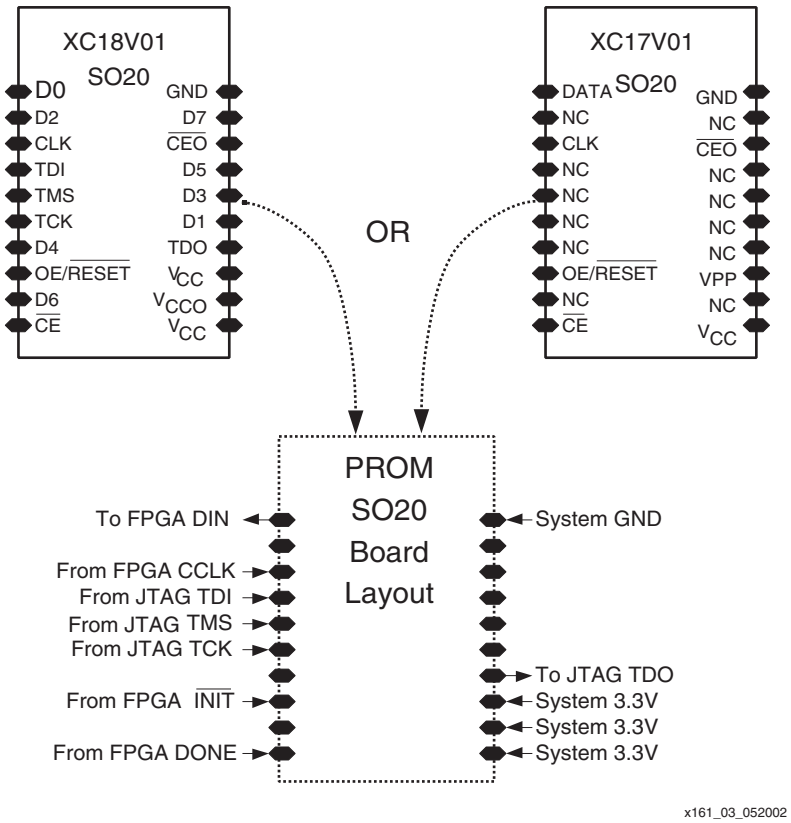

Figure 3: **Example Board Layout for XC18V01 ISP PROM or XC17V01 OTP PROM**

Figure 4 shows the pad locations for the pins of a PROM in a VQ44 package. The signal connections to a Xilinx FPGA are also shown. The pad layout in Figure 4 is compatible with both the XC18V04-VQ44 ISP PROM and the XC17V04-VQ44 OTP PROM. A few of the XC17V04-VQ44 no-connect (NC) pins will land on pads that have connections to board-level signals. It is safe to connect the XC17V04-VQ44 NC pins to these board-level signals.

Figure 4 shows separate JTAG scan chains for the PROM and FPGA. See the Boundary Scan Integrity section of this application note for alternate suggestions regarding the JTAG scan chain architecture.

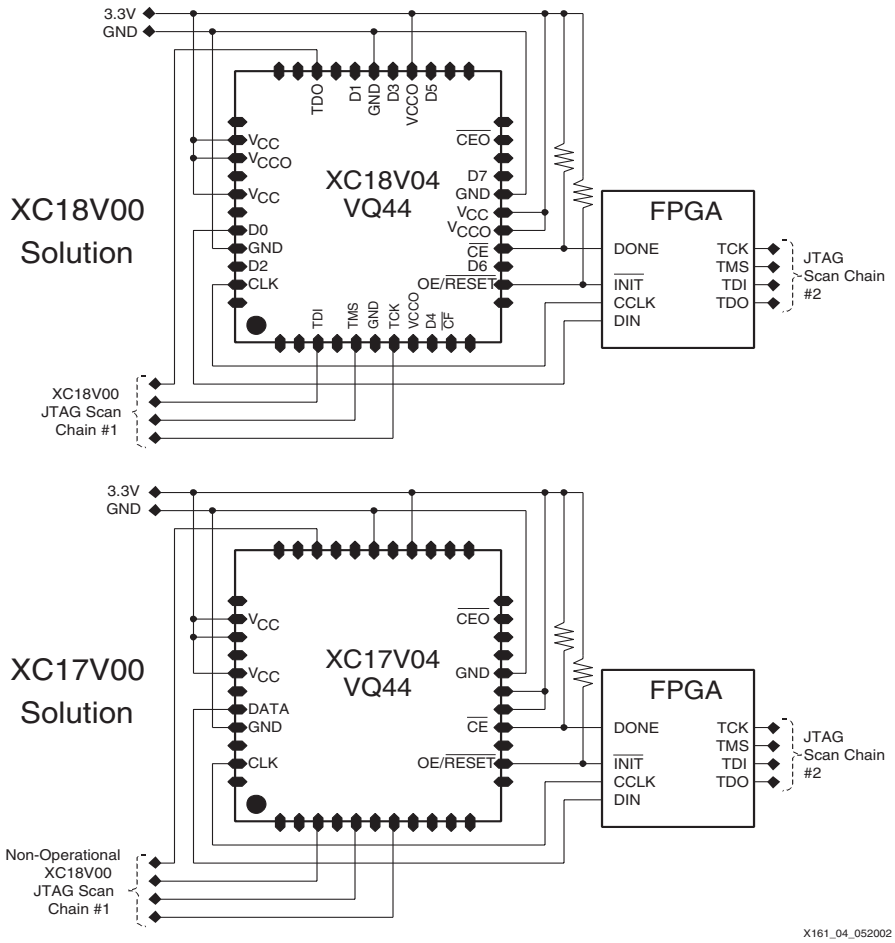

Figure 4: **Example Board Layout for XC18V04 to XC17V04 PROM Migration**

Figure 5 shows the pad locations for the pins of two cascaded PROMs in VQ44 packages. The signal connections to a Xilinx FPGA are also shown. Although two XC18V04-VQ44 ISP PROMs or two XC17V04-VQ44 OTP PROMs can be placed in the pad layout in Figure 5, the figure demonstrates that a cascaded set of XC18V04 ISP PROMs can be replaced with a single, higher-density XC17V00 OTP PROM using the same board layout. A few of the XC17V08-VQ44 no-connect (NC) pins will land on pads that have connections to board-level signals. It is safe to connect the XC17V08-VQ44 NC pins to these board-level signals.

Figure 5 shows separate JTAG scan chains for the PROMs and FPGA. See the **Boundary Scan Integrity** section of this application note for alternate suggestions regarding the JTAG scan chain architecture.

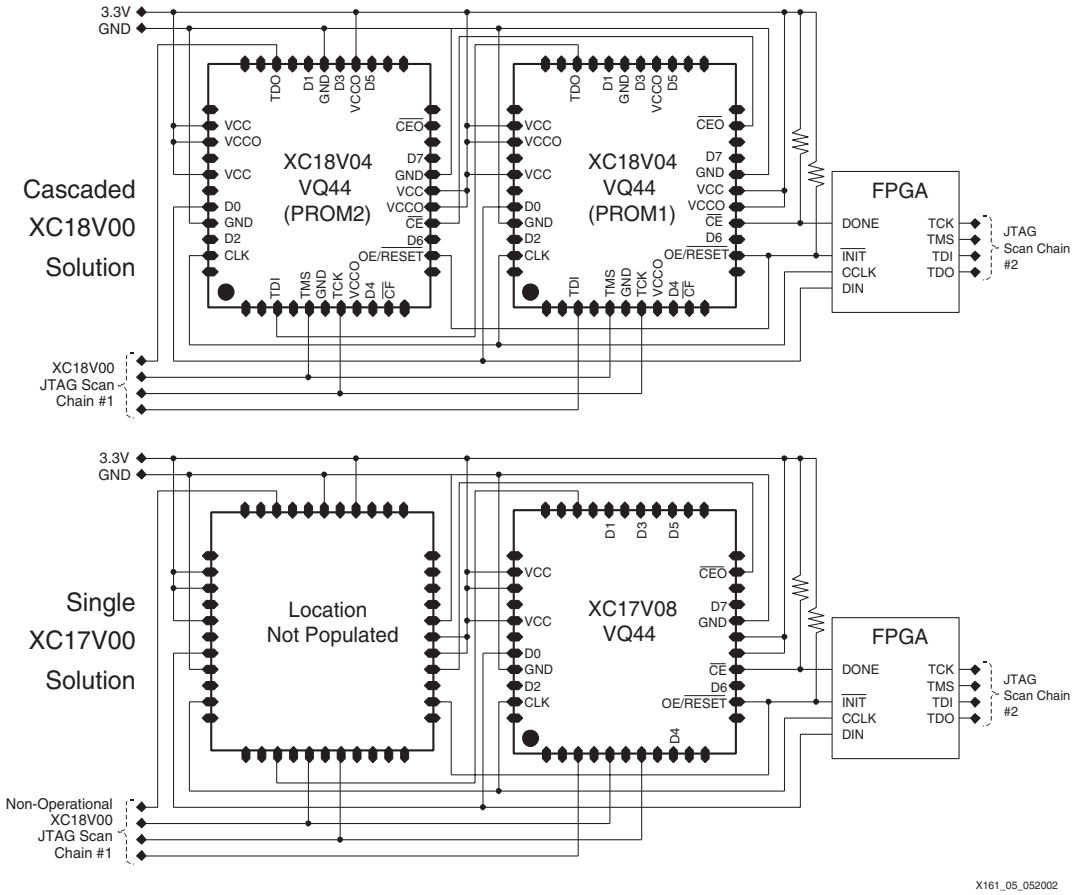

Figure 5: **Example Board Layout for Cascaded XC18V04 to XC17V08 PROM Migration**

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
9/28/99	1.0	Xilinx initial release.
2/17/00	2.0	Changed XC1800 to XC18V00 and updated format.
5/20/02	3.0	Major revision of technical content.
6/10/02	3.1	Product name amended for Virtex Series and Virtex-II Series Platform FPGA on pages 4 and 6.
01/25/03	3.2	Edits to Table 3.