XAPP310 (v1.2) December 20, 2000

Power-Up Reset Characteristics of CoolRunner XPLA3 CPLDs

Introduction

Depending upon where and how CoolRunner™ CPLDs are used, the power up characteristics may be of interest. Figure 1 describes an "ideal" system power voltage ramp for Xilinx CoolRunner CPLDs. As one can see, the voltage must be monotonic during V_{CC} ramp. Also notice that the voltage must not reach valid V_{CC} in less than 100 nanoseconds. This will not present a problem because a system power bus would have to have an impedance of less than 0.5 Ohms and a total capacitance of less than 0.1 microfarads in order to produce a voltage ramp below this minimum. Even if one were to power a CoolRunner CPLD from the output of another device, (something that can be accomplished since they are such LOW power consumers) it would still be difficult to ramp up before the minimum ramp specification.

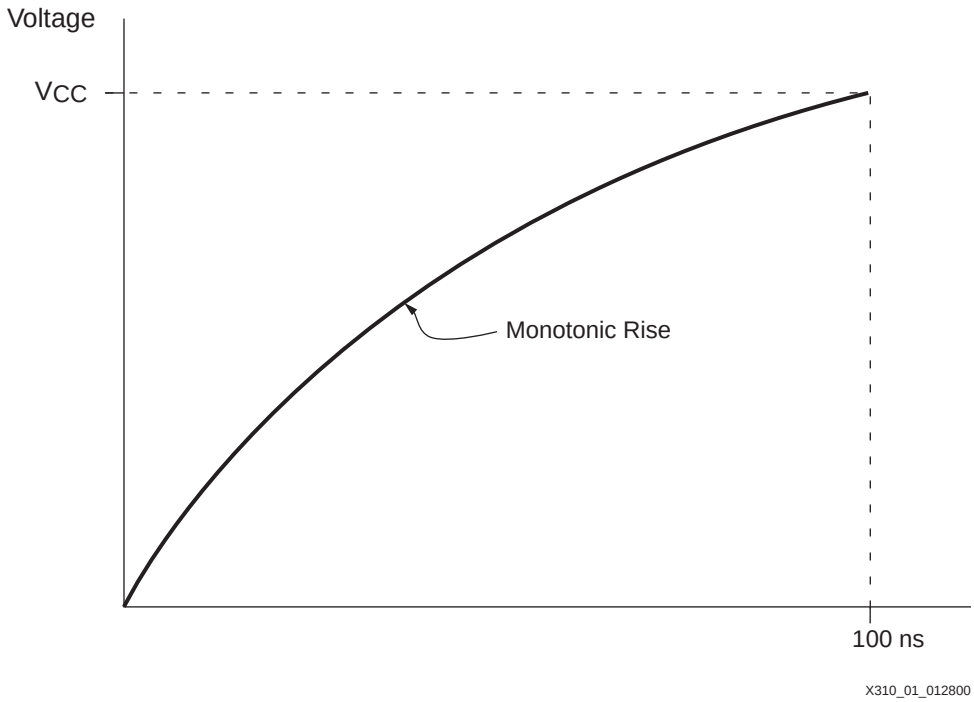

Figure 1: **"Ideal" Voltage Ramp**

Figure 1 is the "Ideal" voltage ramp, and does not exist in most applications. A more realistic example of a power voltage ramp appears in Figure 2.

Many times a "glitch" will appear in the system power voltage ramp due to the instantaneous current demand produced by many active devices "turning on" at the same time. This flattening

out of the voltage curve is acceptable as far as CoolRunner CPLDs are concerned, as long as it does not go in a negative direction.

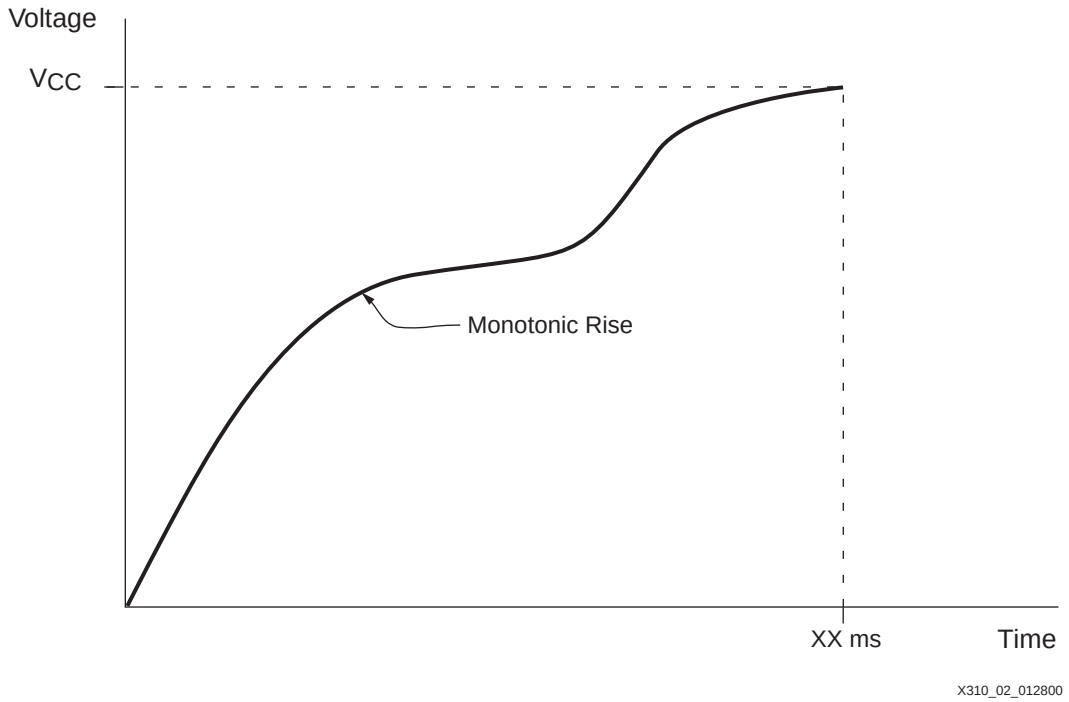

Figure 2: **Realistic Voltage Ramp**

During the time that the power voltage ramp is below a nominal V_{CC} operating level, the I/O pins on the CoolRunner devices will be in a high-impedance state. Once a valid operating V_{CC} is reached the following will occur:

1. Output pins controlled by combinatorial logic will immediately go to the proper level determined by the result of the logic equations.
2. Registered output pins will go to either a set or reset until the first valid clock edge is generated. This clock edge will then clock the value of the register's input to its output. Figure 3 illustrates how the set or reset state upon power up is software selectable in Project Navigator. This property can be selected in the **Implement Design Process Properties** window for all registers. To specify the initial state for an individual register, please refer to XAPP352: "Utilizing a User Constraint File for CoolRunner CPLDs".

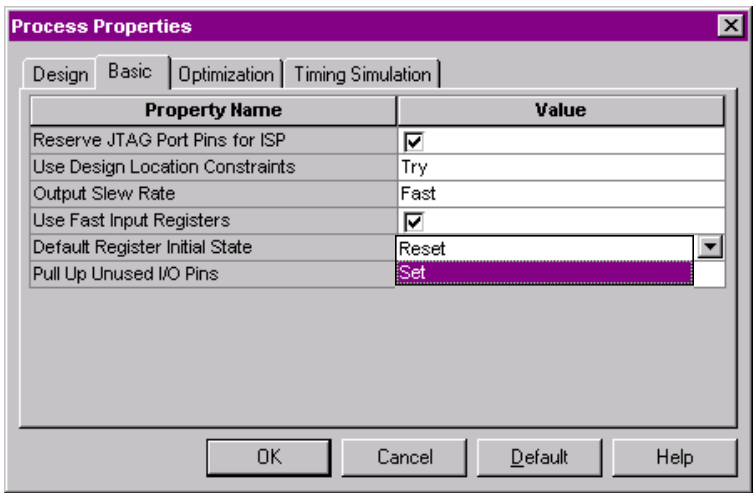

Figure 3: **Selecting Register Power-Up State**

Figure 4 graphically describes this situation.

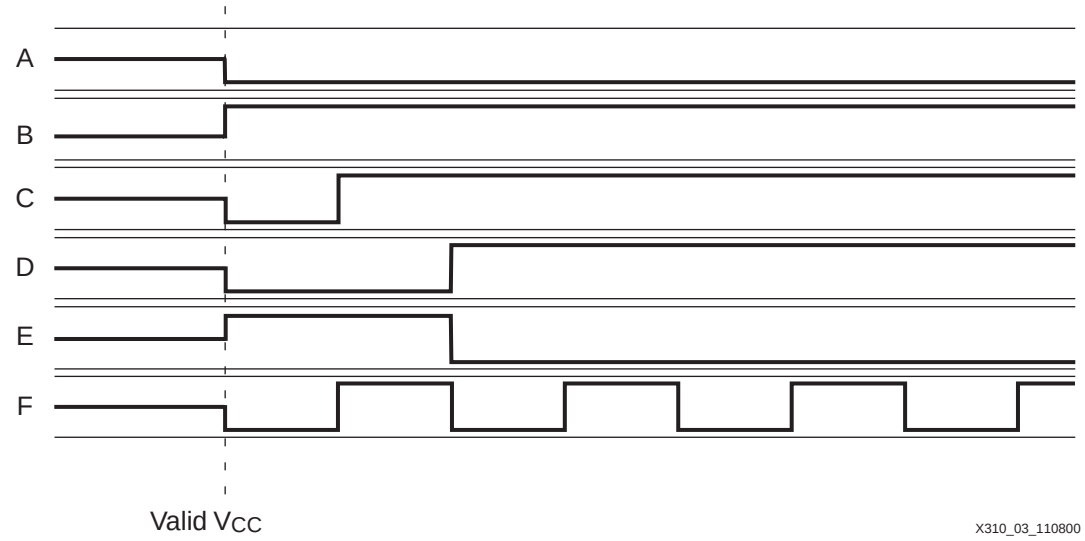

Figure 4: **Power-up Graphic**

The signals represented by the letters A through F are:

A - Output combinatorial signal driving Low

B - Output combinatorial signal driving High

C - Output registered signal reset on power-up driving the output High on valid rising edge clock

D - Registered signal reset on power-up driving the output High on valid falling edge clock

E - Registered signal set high on power-up driving the output Low on valid falling edge clock

F - Clock input

As can be seen if Figure 4, all I/Os are at high impedance until valid V_{CC} is reached. After the power voltage ramp reaches a valid level, a few milliamps of current will be drawn while the device configures. The time during which this current is drawn is approximately 50 microseconds. After configuration is complete the device will draw less than 100 microamps with no toggling inputs. This is true of all the parts in the CoolRunner family.

XPLA3 POR Thresholds

The minimum value of V_{CC} for operation of a device starting from a non-powered state is referred to as the upper threshold voltage. Note that this upper threshold is well below the minumum operating voltage that the device is characterized at, therefore, operation at this voltage is not guaranteed. The device continuously monitors V_{CC} for adequate operating voltage. During power down, V_{CC} will pass through the upper threshold and will then pass through a lower voltage threshold. The lower voltage threshold has been identified as the lowest voltage that the part will operate at (please note that devices are not characterized or guaranteed at this voltage). As the voltage goes below the lower threshold, all I/Os are forced into a 3-state condition.

XPLA3 devices have dual hysteresis circuits where the lower threshold is adjusted downward after initialization. If a device voltage passes upward through both the lower threshold and the upper threshold, all registers in the CPLD are reset or preset to their initial operating state.

If a device is operating at nominal V_{CC}, and the V_{CC} value drops below the upper threshold and returns to nominal, no reset will occur. If V_{CC} drops below the lower threshold (for any period of

time) and returns to nominal V_{CC}, a reset will occur. Refer to Table 1 for actual voltage levels of XPLA3.

Table 1: **XPLA3 Power On Reset Thresholds**

Temperature	Upper Threshold	Lower Threshold Before Init	Lower Threshold After Init
Typical at 25°C	2.03V	1.95V	1.65V
Over Process Corners at 25°C	2.00V-2.05V	1.92V-1.97V	1.62 -1.68V
Over Process Corners –40° to 80°C	1.96V-2.08V	1.88V-2.00V	1.58V-1.71V

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
02/14/00	1.1	Converted to Xilinx format.
12/20/00	1.2	Changed for XPLA3 and added POR threshold section