CoolRunner-II I/O Characteristics

XAPP382 (v1.0) November 11, 2002

Summary

This document is designed to be a comprehensive description of the I/O structure of the CoolRunner™-II CPLD family. The I/O pins have the most dramatic externally observed behavior of any IC feature. This application note should help illustrate what the I/Os can and cannot do, as well as detail the limits of their drive and performance.

Introduction

The CoolRunner-II CPLD family is the industry's lowest power programmable logic device, operating at a core voltage of 1.8V. It provides even lower power consumption than its predecessor, the CoolRunner XPLA3 family. More importantly, CoolRunner-II devices are the industry's first CPLDs to promote system integration by including features such as clock division, DualEDGE, DataGATE, Schmitt trigger inputs, I/O banking, and multiple I/O standards.

CoolRunner-II CPLD I/O Architecture Overview

Basic Structure

Figure 1 shows the basic structure of the CoolRunner-II CPLD I/O cell. As shown, there are a variety of input and/or output options available at each pin. This section provides an overview of each component in the figure below. A more detailed analysis of each block is provided in later sections.

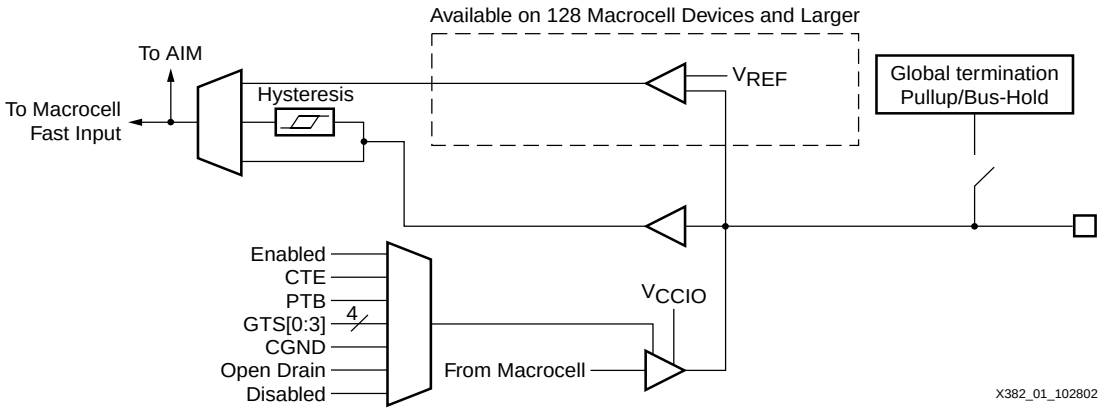

Figure 1: **CoolRunner-II I/O Cell Diagram**

Input/Output Buffers

CoolRunner-II devices feature highly configurable input and output buffers which provide support for a wide variety of I/O standards. An input buffer can be configured either as a simple single-ended buffer or as a comparator.[1] Single-ended voltage inputs have the option of using

1. Voltage referenced logic inputs are only available on 128-macrocell and denser parts.

hysteresis (Schmitt trigger). This adds a time delay, but significantly improves input buffer stability for noisy and slow rising signals.

An output buffer can be configured as either a Push-Pull output or as an Open Drain output. CoolRunner-II CPLD I/O buffers are capable of supporting a variety of current and voltage requirements. The **Overview of Supported I/O Standards** section on page 3 provides a complete list of these I/O capabilities. CoolRunner-II devices also support slew rate control on all output buffers.

I/O Termination Schemes

Pull-up resistors and bus-hold (weak keeper) circuits are available to each I/O pad. These termination types are typically used to prevent I/O pins configured as inputs from floating. They can also be used to terminate unused I/O pins. If no pull-up or bus-hold is desired, the pads can be allowed to float. However, floating I/O pins can cause excessive current draw, and should be done only when absolutely necessary. This is detailed below.

Input Termination

Table 1 shows the possible termination schemes for an I/O pin configured as an input. Note that selection of pull-up or bus-hold terminations are done on a global basis and are mutually exclusive. In other words, CoolRunner-II devices support either pull-up or bus-hold termination, but never a combination of the two on the same device. Once a global termination type has been set, any individual I/O pin can choose to ignore the selected global termination type and can instead be set to float.

However, use caution when floating an input pin. It is the user's responsibility to ensure that the signals driving the floating I/O pin are as close to the voltage rails as possible and that these signals transition as quickly as possible. For absolute low power operation, it is imperative that CoolRunner-II CPLD input pins are never allowed to float and that they be driven by full rail-to-rail outputs.

Table 1: **All Possible Termination Schemes for I/Os Configured as Inputs**

Possible Input Termination Schemes
All Pull-up
All Bus-Hold
Combination of Pull-Up and Float
Combination of Bus-Hold and Float
All Float

Unused I/O Termination

Table 2 shows the possible termination schemes available for unused I/O pins. Notice that unused I/O pins have an additional option: Configurable Ground or CGND. Again, selection of Pull-up or bus-hold termination is done on a global basis and are mutually exclusive. It is not possible to have some I/Os pulled-up while others are utilizing bus-hold. For example, if Pull-up is selected as the termination type for I/Os configured as inputs, unused I/O pins can no longer use bus-hold. However, each individual I/O pin can be set to ignore the chosen global termination type and can instead be set to float or to CGND.

In cases where it may be necessary to float unused I/O pins, it is recommended that external resistors be used to pull the unused input as close to the voltage rails as possible. Leaving the pins floating will cause excessive current draw.

Table 2: **All Possible Termination Schemes For Unused I/Os**

Unused I/O Termination Schemes
All Pulled-Up (not possible if Bus Hold is selected for input termination)
All Bus-Hold (not possible if Pull-up is selected for input termination)
All CGND
All Float

Overview of Supported I/O Standards

This section provides an overview of the I/O standards supported by CoolRunner-II devices. More detailed information on each specification can be obtained from the Electronic Industry Alliance JEDEC website at: **http://www.jedec.org**. Table 3 summarizes these supported I/O standards.

LVTTL—Low Voltage TTL

The Low-Voltage TTL (or LVTTL) standard is a general purpose EIA/JESDSA standard for 3.3V applications that use an LVTTL input buffer and a Push-Pull output buffer. The LVTTL interface is defined by JEDEC Standard JESD 8-A, *Interface Standard for Nominal 3.0 V/3.3 V Supply Digital Integrated Circuits*. The LVTTL specification requires the output buffer to drive to at least 2.4V. The maximum recommended input voltage for CoolRunner-II devices is 3.9V, which meets the 3.9V requirement of the LVTTL Specification. This standard requires a 3.3V output source voltage (V_{CCIO}), but does not require the use of a reference voltage (V_{REF}) or a termination voltage (V_{TT}). CoolRunner-II CPLDs are fully compliant with this standard.

LVCMOS33—Low Voltage CMOS for 3.3 Volts

The Low-Voltage CMOS for 3.3V or LVCMOS33 standard is used for general purpose 3.3V operations. This standard is defined in JEDEC Standard JESD 8-A, *Interface Standard for Nominal 3.0 V/3.3 V Supply Digital Inegrated Circuits*. LVCMOS33 is more stringent than the LVTTL specification in that the outputs are required to swing rail to rail under light dc load conditions (minimum $V_{OH} = V_{CCIO} –0.2V$). The input buffer requirements are the same as the LVTTL requirements. This standard requires a 3.3V output source voltage (V_{CCIO}), but does not require the use of a reference voltage (V_{REF}) or a termination voltage (V_{TT}). CoolRunner-II devices are fully compliant with this standard.

LVCMOS25—Low-Voltage CMOS for 2.5 Volts

The Low-Voltage CMOS for 2.5V or LVCMOS25 standard is an extension of the LVCMOS standard used for general purpose 2.5V applications. LVCMOS25 is defined in JEDEC Standard JESD 8-5, *2.5 V ± 0.2 V (Normal Range) and 1.7 V to 2.7 V (Wide Range) Power Supply Voltage and Interface Standard for Nonterminated Digital Integrated Circui*t. This standard requires that the output buffer drive to at least 2.1V when sourcing 100 µA of current. In addition, the maximum input voltage for CoolRunner-II CPLDs is 3.9V, which is consistent with the LVCMOS25 specification. LVCMOS25 requires a 2.5V output source voltage (V_{CCIO}), but does not require the use of a reference voltage (V_{REF}) or a board termination voltage (V_{TT}). CoolRunner-II devices are fully compliant with the LVCMOS25 standard.

LVCMOS18—Low-Voltage CMOS for 1.8 Volts

The Low-Voltage CMOS for 1.8V or LVCMOS18 standard, as defined by JEDEC Standard JESD 8-7, is used for general purpose 1.8V applications. This standard is similar to LVCMOS33 and LVCMOS25 but is used for 1.8V power supply levels and has been modified to reduce input and output thresholds. This standard requires a 1.8V output source voltage

(V_{CCIO}), but does not require the use of a reference voltage (V_{REF}) or a board termination voltage (V_{TT}). CoolRunner-II devices are fully compliant with LVCMOS18.

1.5V I/O

CoolRunner-II CPLDs are capable of supporting 1.5V single-ended I/O operation. This standard requires a 1.5V output source voltage (V_{CCIO}), but does not require the use of a reference voltage (V_{REF}) or board termination voltage (V_{TT}).

HSTL—High-Speed Tranceiver Logic

The High-Speed Transceiver Logic, or HSTL standard is a general purpose high-speed, 1.5V bus standard sponsored by IBM (EIA/JESD 8-6). HSTL is a voltage-referenced standard requiring a Voltage Referenced Amplifier input buffer and a Push-Pull output buffer. HSTL also requires a 0.75V reference voltage (V_{REF}), a 1.5V I/O voltage (V_{CCIO}), and a 0.75V threshold voltage (V_{TT}). This standard has four variations or HSTL classes. CoolRunner-II devices are fully compliant HSTL Class I.

SSTL3—Stub Series Terminated Logic for 3.3V

The Stub Series Terminated Logic for 3.3V, or SSTL3 standard is a general purpose 3.3V memory bus standard also sponsored by Hitachi and IBM (JESD8-8). SSTL3 is typically used for high speed memory interfaces, such as SDRAM. It is a voltage-referenced standard which requires a Voltage Referenced Amplifier input buffer and an Push-Pull output buffer. SSTL3 also requires a 1.5V reference voltage (V_{REF}), a 3.3V I/O Voltage (V_{CCIO}) and a 1.5V threshold voltage (V_{TT}). This standard has two classes, I and II. CoolRunner-II devices are fully compliant with the SSTL3 Class I standard.

SSTL2 -- Stub Series Terminated Logic for 2.5V

The Stub Series Terminated Logic for 2.5V, or SSTL2 standard is a general purpose 2.5V memory bus standard sponsored by Hitachi and IBM (JESD8-9). SSTL2 is typically used for high speed memory interfaces, such as SDRAM. It is a voltage referenced standard which requires a Voltage Referenced Amplifier input buffer and an Push-Pull output buffer. SSTL2 also requires a 1.25V reference voltage (V_{REF}), a 2.5V I/O voltage (V_{CCIO}) and a 1.25V threshold voltage (V_{TT}). This standard has two classes, I and II. CoolRunner-II devices are fully compliant with the SSTL2 Class I standard.

Table 3: **Supported I/O Standards (Typical values)**

I/O Standard	Output Source Voltage (V_{CCIO})	Input Reference Voltage (V_{REF})	Board Termination Voltage (VTT)
LVTTL	3.3	N/A	N/A
LVCMOS33	3.3	N/A	N/A
LVCMOS25	2.5	N/A	N/A
LVCMOS18	1.8	N/A	N/A
1.5V I/O	1.5	N/A	N/A
HSTL Class I	1.5	0.75	0.75
SSTL2 Class I	2.5	1.25	1.25
SSTL3 Class I	3.3	1.5	1.5

CoolRunner-II Output Buffers: A Detailed Look

Overall Structure of CoolRunner-II CPLD Output Buffers

All output buffers in CoolRunner-II CPLDs can be modeled by a basic CMOS inverter as shown in Figure 2. In order to drive the pin to a logic high level, the P-channel transistor is turned on while the N-channel transistor is off, thereby sourcing current from V_{CCIO} to the I/O pin. To drive a logic low value, the P-channel transistor is turned off while the N-channel transistor is turned

on. This discharges the load capacitance and causes current to flow through the N-channel transistor to ground. Note that the voltage on V_{CCIO} determines the voltage swing on the I/O pin.

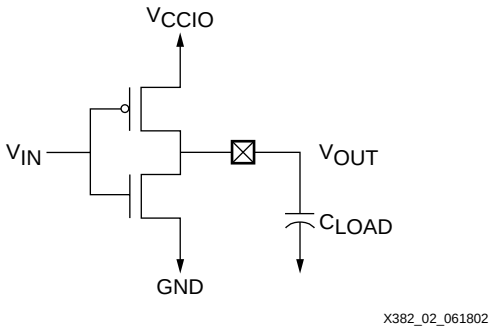

Figure 2: **Basic CMOS Inverter**

Note: It is therefore important to select the correct I/O Standard through the Xilinx implementation software. Doing so will ensure the correct transistor configuration, and will result in appropriate rise and fall times as well as appropriate current drive.

Programmable Output Capabilities

Open-Drain

CoolRunner-II output buffers can be optionally configured for open drain operation. When configured as open-drain, the logic value at the output pin will either be high-Z or constant 0 (GND). In other words, a one state in the design will produce a high-Z on the device, while a zero state in the design will produce a constant 0 on the device. Typically, an external pullup resistor is used to create a logic High value when the output is undriven.

Figure 3 shows the circuit when a CoolRunner-II I/O pin is configured as open-drain. Notice that the PMOS transistor network of Figure 2 is completely turned off and can therefore be ignored. When the N-channel transistor is turned on (by internal user logic) the pin is pulled Low. Alternately, when the N-channel transistor is shut off, the external resistor creates a valid logic High level at the pin.

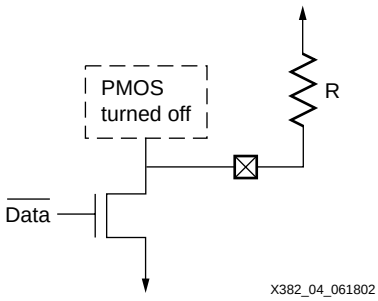

Figure 3: **CoolRunner-II Open-Drain Operation with External Pullup Resistor**

Open-Drain operation is a user-controlled software attribute—there is no need to code the design any differently. Instead, a user simply needs to use software attributes to declare which outputs should be configured as open-drain.

Slew Rate Control

All CoolRunner-II CPLD outputs have an option for fast or slow slew rates. Table 4, Table 5, and Table 6 show typical rise and fall times for 1.8V, 2.5V, and 3.3V I/O operation using both fast and slow slew rate settings. The rise/fall times, denoted in nanoseconds (ns), are equal to

the time difference between 10% and 90% of V_{CCIO}. Note that data is provided for different load capacitances.

Note: The numbers indicated below are based upon a single data point and are given solely as a service for customers to estimate the effects of additional capacitive loading. Xilinx does not guarantee these numbers.

Table 4: **Rise/Fall Times @ V_{CCIO} = 1.8V @ 25°C**

Load Capacitance	Rise Time (ns)		Fall Time (ns)	
	Fast Slew Rate	Slow Slew Rate	Fast Slew Rate	Slow Slew Rate
0 pF	0.2	1.2	0.6	1.0
10 pF	0.9	2.2	1.2	2.0
35 pF	2.5	3.8	2.6	3.5
45 pF	3.2	4.4	3.2	4.0
100 pF	6.8	7.7	6.3	7.2

Table 5: **Rise/Fall Times @ V_{CCIO} = 2.5V @ 25°C**

Load Capacitance	Rise Time (ns)		Fall Time (ns)	
	Fast Slew Rate	Slow Slew Rate	Fast Slew Rate	Slow Slew Rate
0 pF	0.3	1.1	0.7	1.1
10 pF	1.2	2.6	1.4	2.3
35 pF	3.7	4.9	3.1	4.0
45 pF	4.6	5.8	3.8	4.7
100 pF	9.9	11.2	7.8	8.7

Table 6: **Rise/Fall Times @ V_{CCIO} = 3.3V @ 25°C**

Load Capacitance	Rise Time (ns)		Fall Time (ns)	
	Fast Slew Rate	Slow Slew Rate	Fast Slew Rate	Slow Slew Rate
0 pF	0.3	0.8	0.8	1.4
10 pF	1.0	2.2	1.6	2.6
35 pF	2.9	4.3	3.7	4.8
45 pF	3.6	5.0	4.6	5.6
100 pF	7.8	9.0	9.6	10.5

Input Buffers

Overview

Figure 4 shows the input structure of CoolRunner-II CPLD I/O pins. All I/O pins can be configured for single-ended or voltage referenced operation. Single-ended inputs can pass through either a general purpose input buffer or a Schmitt trigger input buffer. Using the Schmitt trigger input buffer provides 500 mV of hysteresis (noise immunity), but will add a time delay.

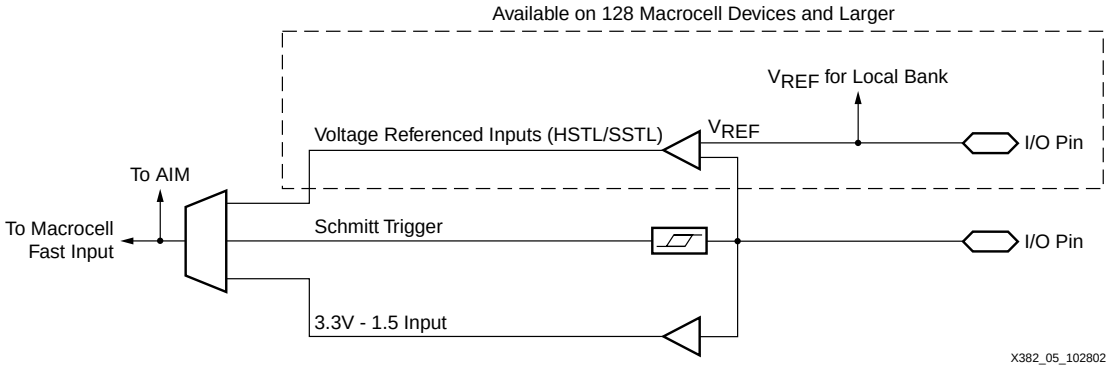

Figure 4: **CoolRunner-II Input Structure**

Schmitt Trigger (3.3V-1.5V)

All CoolRunner-II input pins can be configured as Schmitt trigger inputs. The use of Schmitt triggers greatly improves noise immunity but at a cost of a longer propagation delay. Schmitt triggers are particularly useful for noisy and/or slow rising input signals. Without Schmitt triggers, slow rising or noisy inputs may cause oscillations to occur while the slow rising input signal crosses through the input threshold. Such oscillations can cause false triggering which can lead to system reliability problems and intermittent failures.

Schmitt triggers solve these problems by adding hysteresis. As a result, the input buffers will not trip high until the input signal crosses an upper voltage threshold (V_{T+}) and will not trip low until the input signal crosses lower voltage threshold (V_{T-}). The result is a clean signal coming out of the Schmitt trigger input buffer. Figure 5 represents this. The waveform represents a slow rising, noisy input signal.

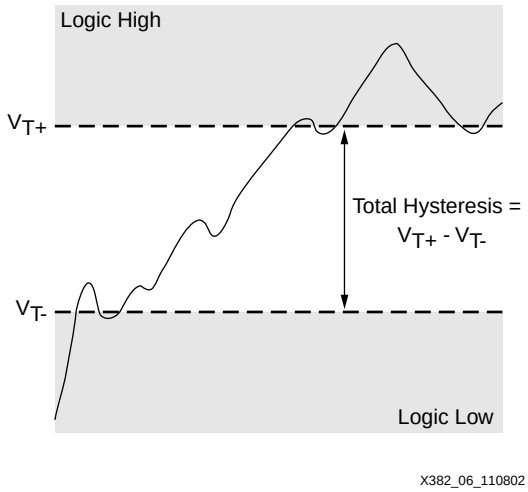

Figure 5: **Representation of a Schmitt Trigger Input Buffer**

Figure 6 illustrates how slow rising input signals can cause the input buffer to oscillate and Figure 7 shows how Schmitt trigger inputs can help resolve this problem. In Figure 6, a slow rising, 1 Hz sawtooth waveform is input to a CoolRunner-II CPLD I/O pin with Schmitt trigger disabled. This input is internally buffered and routed to an output pin. The resulting output waveform, shown on the bottom of the figure, exhibits high frequency oscillations whenever the input waveform crosses the input threshold. In Figure 7, the CoolRunner-II device is configured

to use Schmitt trigger inputs, and as shown, the same slow rising, 1 Hz input sawtooth waveform results in a very clean 1 Hz output.

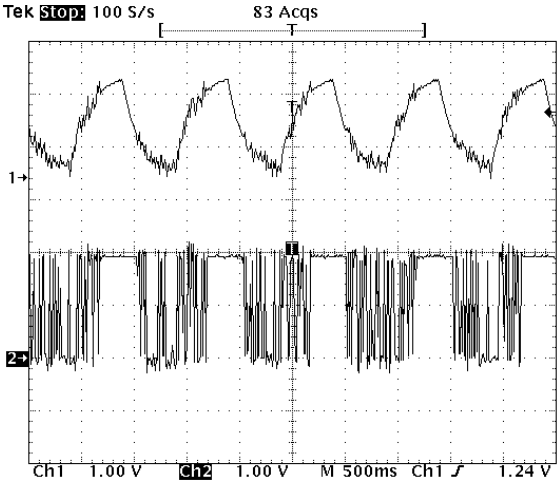

Figure 6: **Effect of Not Using Schmitt Trigger Inputs on a Slow Rising Input Signal**

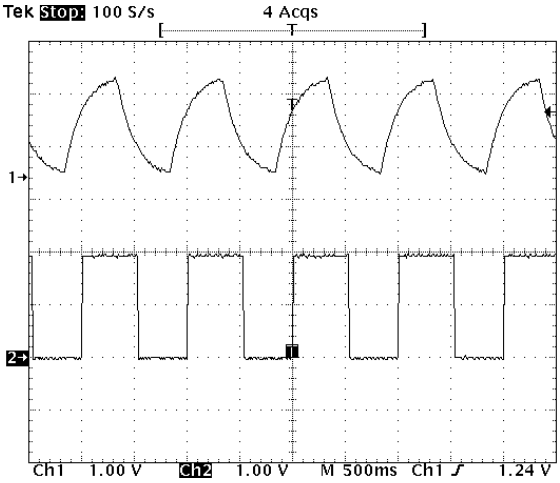

Figure 7: **Benefit of Using Schmitt Trigger Inputs on a Slow Rising Input Signal**

Schmitt trigger inputs are ideal for slow edge rate, noisy signals such as those comming from Analog comparators/sensors, Hall effect switches, IR inputs, and R/C oscillators. They eliminate the need for external Schmitt trigger buffers.

The Schmitt trigger input voltage threshold is dependent upon the output bank voltage. When selected, the Scmitt trigger is designed to provide 400 mV of hysteresis when V_{CCIO} is 1.5V, 500 mV of hysteresis when V_{CCIO} is 1.8V or 2.5V, and 1.0V of hysteresis when V_{CCIO} is 3.3V. This operating window will fall within voltage ranges specified in Table 7.

Table 7: **Input Schmitt Trigger Operating Window**

Edge	Min	Max
V_{T+}	0.5 * V_{CCIO}	0.8 * V_{CCIO}
V_{T-}	0.2 * V_{CCIO}	0.5 * V_{CCIO}

Figure 8 shows typical Schmitt trigger operation at 1.5V, 1.8V, 2.5V, and 3.3V. In all cases a sawtooth waveform is input to a CoolRunner-II CPLD I/O pin configured as a Schmitt trigger.

The signal is in turn buffered and directly routed to an output pin. The traces show both the input and output waveforms. The V_{T+} and V_{T-} levels for each voltage range are also shown and are represented by the horizontal cursors in the figure. The top two images in Figure 9 (from left to right) represent 1.5V and 1.8V V_{CCIO}, and the bottom two images (from left to right) represent 2.5V and 3.3V V_{CCIO} operation.

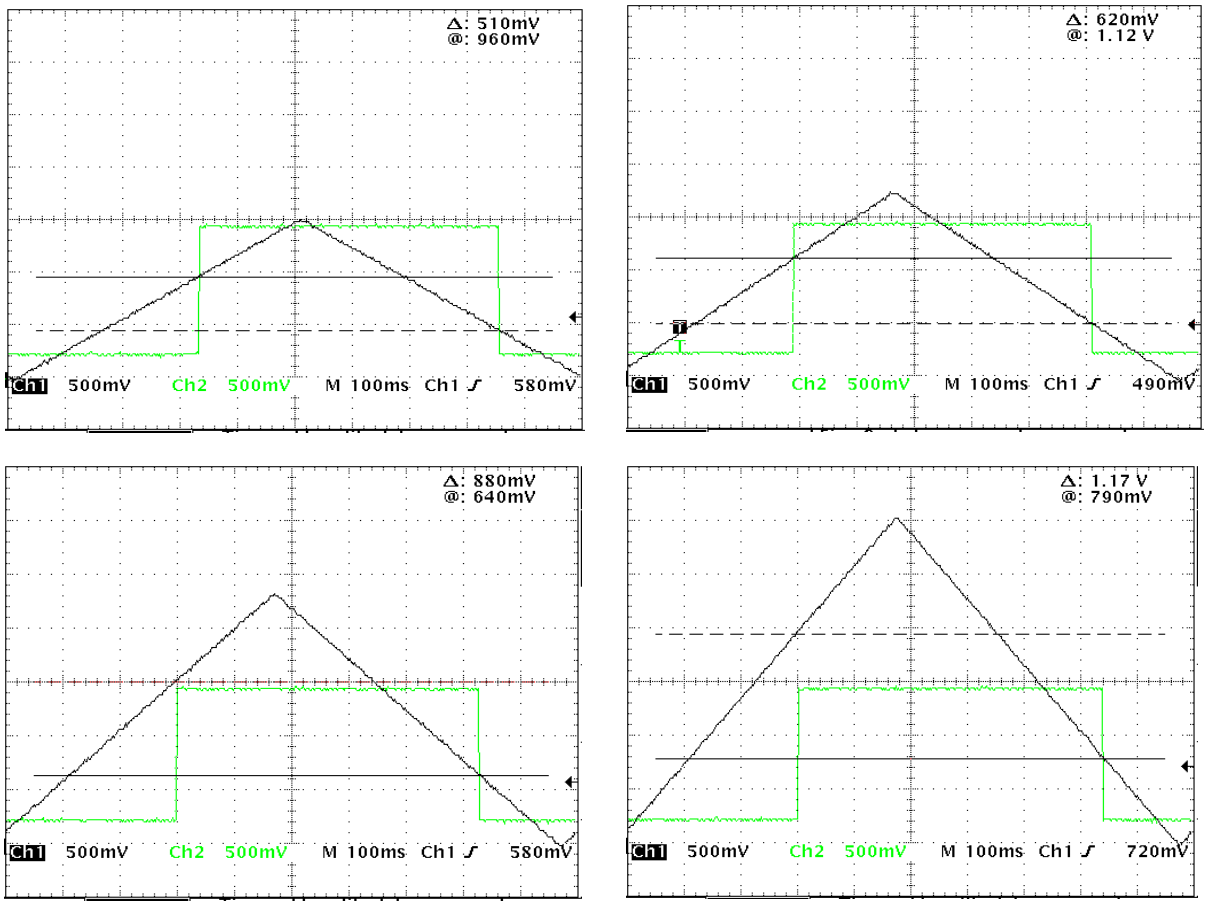

Figure 8: **Schmitt Trigger Operation at 1.5V, 1.8V, 2.5V, and 3.3V**

Table 8 summarizes these results.

Table 8: **Schmitt Trigger Characteristics**

	V_{CCIO} = 1.5V	V_{CCIO} = 1.8V	V_{CCIO} = 2.5V	V_{CCIO} = 3.3V
V_{T+}	0.96V	1.12V	1.52V	1.96V
V_{T-}	0.45V	0.5V	0.88V	0.79V
Hysteresis	0.51V	0.62V	0.64V	1.17V

Voltage Referenced Inputs

Voltage Referenced inputs exist as an option for devices with two or more I/O banks (128MC devices and larger). These voltage referenced inputs require a voltage reference source (V_{REF}). CoolRunner-II devices are designed such that any I/O pin may be selected to provide a voltage reference for these voltage referenced inputs. Software attributes allow designers to specify which pins should be designated as V_{REF}. When determining placement of V_{REF}, the following two rules must be obeyed:

1. A single V_{REF} pin can only support up to a maximum of six voltage referenced inputs.

2. No voltage referenced input signal can be more than a distance of six pads away from a V_{REF} pin.

Failure to follow these rules will result in a software error, and the design will not route.

Note: It is strongly recommended that designers allow the software to assign V_{REF} pins prior to laying out a printed circuit board.

I/O Termination Options

Bus-Hold (Weak Keeper)

An optional bus-hold circuit (also known as a weak-keeper) is connected to each output as shown in Figure 9. When selected, the circuit monitors the voltage on the pad and weakly drives the pin high or low to match the input signal. Bus-hold circuitry is equivalent to a full latch on the I/O pin—it will drive the I/O pin either high or low, depending on its previous state. Bus-hold prevents the CoolRunner-II I/O pins from going into the high-impedance state. Maintaining a valid logic level in this way eliminates bus chatter.

The bus-hold circuit drives back the same state via a nominal resistance (R_{BH}) of approximately 100k ohms at 1.8V. The bus-hold circuit will drive no higher than V_{CCIO}.

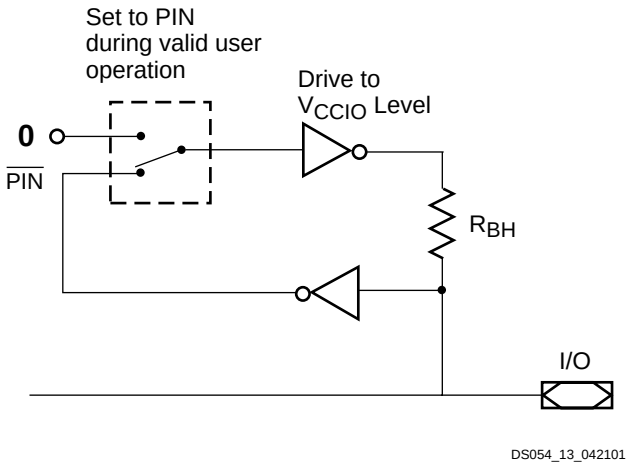

Figure 9: **CoolRunner-II Bus-Hold Circuit**

Pull-Up

As an alternative to bus-hold, inputs can be internally pulled up. This connects a high-impedance resistive load onto the I/O pad to prevent a floating situation on the pin. Note that there are some cases where a pull-up is undesirable. For example, if a CoolRunner-II CPLD I/O pin configured with pull-up is connected to a bus that is pulled down for the majority of the time, current will unnecessarily flow from V_{CCIO} to ground. This will cause excess power consumption in the CoolRunner-II device. For such cases, bus-hold termination is a better choice. The pull-up resistance is approximately 100k ohms at 1.8V.

CGND (Configurable Ground)

Unused inputs can be independently configured to be configurable ground, or CGND. This allows the device I/O pins to be configured as additional ground pins in order to force otherwise unused pins to a low voltage state. This also provides for additional device grounding capability. This grounding of the pin is achieved by internal logic that forces a logic low output regardless of the internal macrocell signal, so the internal macrocell logic is unaffected by the configurable ground capability. Additional benefit can be gained by attaching CGND configured pins to the PCB ground.

Power-Up Characteristics

During power-up, CoolRunner-II devices employ internal circuitry which keeps the devices in the quiescent state until the V_{CCINT} supply voltage is at a sufficient level for power-up (approximately 1.3V). In the quiescent state, JTAG pins are disabled, and all device outputs are disabled with the pins weakly pulled high, as shown in Table 9. When the supply voltage reaches a safe level, all user registers become initialized (typically within 200 µs), and the device is immediately available for operation, as shown in Figure 10.

After power-up, if the device is in the erased state (before any user pattern is programmed), the device outputs remain disabled with a weak pull-up. The JTAG pins are enabled to allow the device to be programmed at any time. All devices are shipped in the erased state from the factory.

If the device is programmed after power-up, the device inputs and outputs take on their configured states for normal operation. The JTAG pins are enabled to allow device erasure or boundary-scan tests at any time.

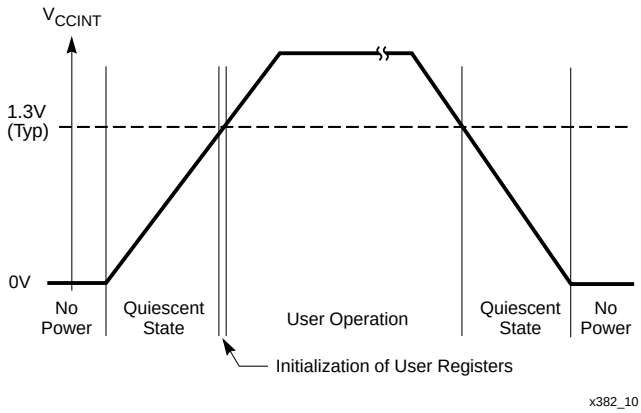

Figure 10: **Device Behavior During Power Up**

Table 9: **I/O Power-Up Characteristics**

Device Circuitry	Quiescent State	Erased Device Operation	Valid User Operation
IOB Termination	Pull-up	Pull-up	As Configured(1)
Device Outputs	Disabled	Disabled	As Configured
Device Inputs and Clocks	Disabled	Disabled	As Configured
JTAG Controller	Disabled	Enabled	Enabled

Notes:
1. Refer to **I/O Termination Schemes**, page 2

Conclusion

CoolRunner-II CPLDs feature a uniform I/O structure that provides system designers with a variety of I/O options. Understanding these I/O capabilities and characteristics can greatly simplify the implementation of CoolRunner-II CPLD-based designs.

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
11/11/02	1.0	Initial Xilinx release.