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Packaging Thermal Management

Thermal Management

Modern high-speed logic devices consume appreciable amount of electrical energy. This energy invariably turns into heat. Higher device integration drives technologies to produce smaller device geometry and interconnections. With the chip sizes getting smaller and circuit densities at their highest levels, the amount of heat generated on these fast switching CMOS circuits can be very significant. As an example, the latest high-end Xilinx FPGA devices incorporate multiple processors, multiple gigabit transceivers, digital controlled impedance I/Os and I/Os capable of supporting various high current standards. Special attention must be paid to address the heat removal needs for these devices.

The need to manage the heat generated in a modern CMOS logic device is not unique to Xilinx. This is a general industry pursuit. However, unlike the power needs of a typical industry Application Specific Integrated Circuit (ASIC) gate array, the Field Programmable device's power requirement is not determined as the device leaves the factory. Customers' designs can vary in power as well as physical needs. Therein lies the challenge in predicting the FPGA thermal management needs.

There is no sure way of anticipating accurate power dissipation of an FPGA device short of actual measurement. Several software based power estimator tools have been developed by Xilinx to help the end user predict power consumption. The tools can be useful as a first step. Like most tools, however, the predicted output depends on the work put into the predicting effort. In assigning packages to devices, efforts have been made to tailor the packages to the typical user power needs. For each device, suitable packages are typically chosen to handle "typical" designs and gate utilization for the device. For the most part, the choice of a package as the primary or internal heat removal casing works well without any external heat management. Increasingly with the highly integrated devices the need arises for customers to exercise an FPGA device beyond "typical" designs. For these situations, the use of the primary package without external enhancement may not be adequate to address the heat removal needs of the device. It is for these cases that the need to manage the heat removal through external means becomes essential.

Heat needs to be removed from a device to ensure that the device is maintained within its functional and maximum design temperature limits. If heat buildup becomes excessive, the device's temperature may exceed the temperature limits. A consequence of this is that the device may fail to meet speed-files performance specifications. In addition to performance considerations, there is also the need to satisfy system reliability objectives by operating at a lower temperature. Failure mechanisms and failure rate of devices have an exponential dependence on device operating temperature. Thus, the control of the package, and by extension device temperature, is essential to ensure product reliability.

Package Thermal Characterization Methods and Conditions

Characterization Methods

There are several ways that Xilinx obtains thermal performance characteristics of Integrated Circuit packages. The methods include thermal simulation using finite element software tools, and indirect electrical method, using an isolated diode on a special thermal test die or even on a Xilinx FPGA that is housed in the package of interest. The majority of the data reported by Xilinx is based on the indirect diode method with a few using simulation tools.

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Calibration of Isolated diode

In the indirect electrical method, the forward-voltage drop of an isolated diode residing on a special test die or a Xilinx FGPA is calibrated at constant forcing current in the range of 0.150 mA to 0.500 mA with respect to temperature over a correlation temperature range of up to 125°C (degree Celsius). The calibrated packaged device is then mounted in an appropriate board and placed in the testing environment — e.g., still air or forced convection. Power (P_D) is applied to the device through diffused resistors on the same thermal die. In the FPGA, a known self-heating program is loaded and clocked to generate the monitored power. Usually between 0.5 Watts to 4 Watts may be applied. Higher power is possible depending on the package. The resulting rise in junction temperature is monitored with the forward-voltage drop of the pre-calibrated diode.

Measurement Standards

Previously Xilinx Thermal lab used the SEMI thermal test methods (#G38-87) and associated SEMI based boards (#G42-87) to do thermal characterization. Most of our recent measurements and simulations are based on provision of the JEDEC and EIA Standard — JESD51-n series specifications. It is our assessment that the latter standard offers some options that are not available in the SEMI method. We will continue to quote the SEMI based data (designated with SEMI in comment column) for older packages measured in the earlier era, and when we quote new data, they will be designated as JESD in the comment section.

It is also essential to note that these standard-based measurements give characterization results that allow packages and conditions to be compared. Like miles per gallon (MPG) figures quoted on new cars, the numbers should be used with caution. Since specific user environment will not be the same as the conditions used in the characterization, the numbers quoted may not precisely predict the performance of the package in an application-specific environment.

Definition of Terms

T_J Junction Temperature; defined as the maximum temperature on the die, expressed in °C (degree Celsius).

T_A Ambient Temperature; defined as the temperature of the surrounding environment, expressed in °C (degree Celsius).

T_C Temperature of the package taken at a defined location on the body. In most situations it is taken at the primary heat flow path on the package, and will represent the hottest part on the package, expressed in °C. See below when T_C is taken at the top.

T_t Temperature of the package body taken at the top location on the package. This is a special case of T_C.

T_B This is the board Temperature taken at a predefined location on the board near the component under test, expressed in °C.

T_I This is the isothermal fluid temperature when junction to case temperature is taken, expressed in °C.

P_D The total device power dissipation, expressed in Watts.

Junction-to-Reference General Setup

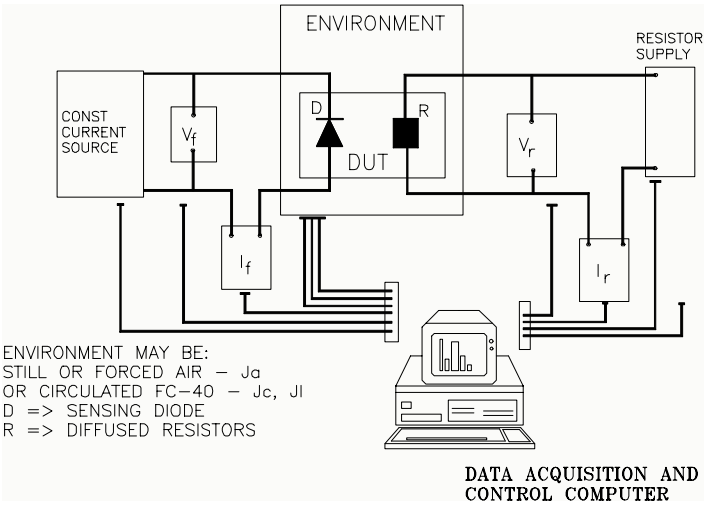

Figure 1: **Thermal Measurement Setup (Schematic for Junction to Reference)**

Junction-to-Case Measurement — θ_{JC}

Theta-jc (θ_{JC}) measures the heat flow resistance between the chip surface and the surface of the package (case). This data is relevant for packages used with external heatsinks. It assumes that heat is flowing through the top to the exclusion of the others. In the ideal case all the heat is forced to escape the package at the path where T_C is taken. The lateral heat flow is not allowed or minimized so that the source of temperature differential will be attributable to the total known heat input.

Copper heatsink plate at the top of the package is used in θ_{JC} methods to achieve the forced preferred directional flow.

Prior to 1999, the junction-to-case characterization on some heatsink packages were accomplished in a 3M Flourinert (FC-40) isothermal circulating fluid stabilized at 25°C. Current Xilinx data on θ_{JC} is simulated using the cold plate approach.

With applied power (P_D) and under stabilized conditions, case temperature (T_C) is measured with a low gauge thermocouple (36-40 AWG) at the primary heat-flow path of the particular package. Junction temperature (T_J) is calculated from the diode forward-voltage drop from the initial stable condition before power was applied, i.e.,

$$\theta_{JC} = (T_J - T_C)/P_D$$

where the terms are as defined above. A poorly defined θ_{JC} condition can usually lead to lower numbers being reported. Most of the temperature difference will be due to a fraction of the power applied but most likely the full power may be used.

Junction-to-Top Measurement — Ψ_{JT}

Psi-jt (Ψ_{JT}) is a junction to top thermal parameter (*not thermal resistance*) defined in JEDEC specification that shadows θ_{JC} in a real world situation. This parameter provides correlation between chip junction temperature and the temperature of the package at the top. It is measured on a defined FR4 based PC board as described under θ_{JA}. The reference temperature is the temperature monitored at the top of the component, T_t. Though the cause of the temperature rise may not be due to all the power applied, the full power is used in the calculation, i.e.,

$$\Psi_{JT} = (T_J - T_t)/P_D$$

where P_D is the full applied power.

The parameter value depends on airflow conditions. In heatsink type packages (some BGs and most FF packages) where the primary heat flow is almost one dimensional and the heat flux is confined to the top, T_C and T_t are taken at the same point and Ψ_{JT} approaches θ_{JC}.

In molded packages like Xilinx FG676, FG900 and FG1156, the one-dimensional condition is difficult to meet. At best, a fraction of the heat flux (~40 – 60%) goes to the top in the standardized setup. In an end-user application, the heat flux division may follow a similar pattern. Under such cases, psi-jt (Ψ_{JT}) and theta-jc (θ_{JC}) tend to diverge from each other. If the total power is known, and the top temperature can be carefully measured, Ψ_{JT} is used to predict the T_J in application environment.

In some plastic molded packages, we may be able to apply Ψ_{JT} numbers relevant to our setup.

Junction-to-Ambient Measurement — θ_{JA}

SEMI method: Some of the data reported are based on the SEMI standard methods and associated board standards. θ_{JA} data reported as based on SEMI were measured on FR4 based PC boards measuring 4.5” x 6.0 x .0625” (114.3mm x 152.4mm x 1.6mm) with edge connectors. Several versions are available to handle various surface mount (SMT) devices. They are however grouped into two main types. Type I board (the equivalent of the JEDEC low conductivity board) is single layer with two signal planes (one on each surface) and no internal Power/Gnd planes. This is the 2L/0P or 2S/0P board and the trace density on this board is less than 10% per side. The type II board (the equivalent of the JEDEC 2S/2P board) has two internal copper planes — one power and one ground. These planes are in addition to the two signal trace layers on both surfaces. This is the 4L/2P (4 layer also referred to as 2S/2P) board.

JEDEC measurements: Packages are measured in a one foot-cube enclosure based on JEDS51-2. Test boards are fashioned per test board specification JESD51-3 and JESD51-7. The board size depends on the package and are typically 76.2mm x 114.3mm x 1.6mm or 101.6mm x 114.3mm x 1.6mm. These come in low conductivity as well as high conductivity versions.

Thermal resistance data may be taken with the package mounted in a socket or, with the package mounted directly on traces on the board. Socket measurements typically use the 2S/0P or low conductivity boards. SMT devices, on the other hand, may use either board. Published data always reflect the board and mount conditions used (ref 2S/0P or 4L/2P).

The board with the device under test (DUT) is mounted in the test enclosure and data is taken at the prevailing temperature and pressure conditions — between 20°C and 30°C ambient (T_A). Appropriate power is used, depending on the anticipated thermal resistance of the package. Applied power, signal-monitoring — including the enclosure (ambient) temperatures are noted. The junction to ambient thermal resistance is calculated as follows:

$$\theta_{JA} = (T_J - T_A)/P_D$$

In the case of Airflow measurement, this is done in a special airflow enclosure section of a suction-type low velocity wind tunnel. Airflow velocities from 0-1000 Linear Feet per Minute (LFM), i.e., 0-5.08 m/s are used with very low turbulence. The controlling specification is JESD51-6. Airflow measurement use similar boards as θ**ja** with air conditions noted with hot wire anemometer.

Thermal Resistance: Junction-to-Board — θ_{JB}

This is defined as:

$$\theta_{JB} = (T_J - T_B)/P_D$$

where T_B is the board temperature at steady state measured at specified location on the board. P_D is the actual power in Watts that produces the change in temperature.

T_B is monitored on a board with a 40-gauge thermocouple at specific location in the proximity of the package leads or balls. As an example, for BGA package, the thermocouple is attached to a trace midway along the side of the package with the attachment point within 1mm of the package body.

Like **Theta-jc, Theta-jb** depends on constrained flow in a preferred direction. In actual measurement or simulations the heat flow is forced to go preferably through the board by excluding other paths with insulation. The measurement conditions are not likely to be reproduced in a real application.

Junction-to-Board Measurement — Ψ_{JB}

Junction-to-board thermal parameter — Ψ_{JB} is a thermal parameter (*not thermal resistance*) defined by JEDEC specification that approximates θ_{JB} in a real world situation. This parameter provides correlation between chip junction temperature and the temperature of the board. It is measured on a high effective thermal conductivity board as described under θ_{JA}**.** The reference temperature is the temperature monitored on the board, T_B. Though the cause of the temperature rise may not be due to all the power applied, the full power is used in the calculation, i.e.,

$$\Psi_{JB} = (T_J - T_B)/P_D$$

where P_D is the full applied power. This parameter is used to obtain chip temperature (T_J) in applications where the board temperature can be monitored as described.

Though currently Xilinx does not publish θ_{JB} and Ψ_{JB} some limited data on Ψ_{JB} exist for some of the high performance Xilinx packages. These may be requested for the specific device package combination.

Since the board selection (copper trace density, absence or presence of ground planes, etc.) affects the results of the thermal resistance, the data from these tests shall always be qualified with the board mounting information as were as the test standard.

Data Acquisition and Package Thermal Database

Data for a package type is gathered for various die sizes, power levels, cooling modes (air flow and sometimes heatsink effects) with a Data Acquisition and Control System (DAS). The system controls and conditions the power supplies and other ancillary equipment for a hands-free data taking. A package is completely characterized with respect to the major variables that influence the thermal resistance. A database is generated for the package. From the database, thermal resistance data is interpolated as typical values for the individual Xilinx devices that are assembled in the characterized package. Table 1 shows the typical values for various packages. It must be noted that specific device data may not be the same as the typical data listed for the package, however, the data will fall within the min. and max. ranges given. The more widely a package is used across FPGA and EPLD families, the wider the range quoted here. If specific device data is required, customers may contact the Xilinx application group for a detailed listing applicable to the device.

More detailed data is also available for the newer packages.

Table 1: **Summary of Thermal Resistance for Packages**

Pkg-Code	θ_{JA} still air (Max) °C/Watt	θ_{JA} still air (Typ) °C/Watt	θ_{JA} still air (Min) °C/Watt	θ_{JA} 250 LFM (Typ) °C/Watt	θ_{JA} 500 LFM (Typ) °C/Watt	θ_{JA} 750 LFM (Typ) °C/Watt	θ_{JC} (Typ) °C/Watt	Comments
BF957	11.2	10.9	10.6	6.8	5.4	4.6	1.1	JESD: 4L/2P-SMT Simulation
BG225	37.2	30.3	23.9	21.9	19.3	18.5	3.6	SEMI: 4L/2P-SMT
BG256	38.8	27.0	21.2	19.5	17.2	16.5	3.9	SEMI: 4L/2P-SMT
BG352	13.3	12.6	11.8	8.8	7.2	6.5	1.0	SEMI: 4L/2P-SMT
BG432	11.8	11.2	10.7	7.9	6.5	5.9	0.9	SEMI: 4L/2P-SMT
BG492	17.2	17.2	17.2	12.2	11.9	11.9	0.8	SEMI: 4L/2P-SMT
BG560	11.2	10.6	10.2	7.4	6.1	5.6	0.8	SEMI: 4L/2P-SMT

Table 1: **Summary of Thermal Resistance for Packages *(Continued)***

Pkg-Code	θ_{JA} still air (Max) °C/Watt	θ_{JA} still air (Typ) °C/Watt	θ_{JA} still air (Min) °C/Watt	θ_{JA} 250 LFM (Typ) °C/Watt	θ_{JA} 500 LFM (Typ) °C/Watt	θ_{JA} 750 LFM (Typ) °C/Watt	θ_{JC} (Typ) °C/Watt	Comments
BG575	16.9	15.8	14.7	12.1	11.4	11.0	2.8	JESD: 4L/2P-SMT Simulation
BG728	13.7	13.6	13.2	10.2	9.3	8.7	1.9	JESD: 4L/2P-SMT Simulation
CB100	48.8	41.9	38.5	25.4	19.7	17.8	5.8	SEMI:Socketed
CB164	29.8	26.7	25.0	16.6	12.4	10.6	3.7	SEMI:Socketed
CB196	26.2	25.0	23.8	15.6	11.6	10.0	2.5	SEMI:Socketed
CB228	21.3	18.5	16.3	11.5	8.6	7.4	1.9	SEMI:Socketed
CC20	105.0	105.0	105.0	72.8	57.7	35.0	7.0	SEMI:Socketed
CC44	48.6	45.8	44.5	37.6	30.8	25.2	8.3	SEMI:Socketed
CD8	121.0	112.9	103.9	80.0	65.7	58.0	7.1	SEMI:Socketed
CD48	40.0	40.0	40.0	-	-	-	5.0	SEMI:Socketed
CG560	14.3	14.3	14.3	9.2	7.2	6.3	1.6	SEMI:Socketed
CG1156	10.7	10.7	10.7	8.0	7.6	6.8	1.0	JESD: 4L/2P-SMT Simulation
CP56	65.0	65.0	65.0	-	-	-	15.0	Estimated
CS48	45.0	45.0	45.0	-	-	-	5.0	Estimated
CS144	65.0	35.7	34.0	25.9	23.9	23.2	2.5	Estimated
CS280	30.5	30.5	30.5	25.0	23.1	22.2	0.8	Estimated
DD8	115.9	109.3	94.0	89.8	73.5	60.2	8.3	Socketed
FF896	11.8	11.8	11.8	8.2	6.7	5.9	1.1	JESD: 4L/2P-SMT Simulation
FF1152	11.9	11.7	11.4	7.6	6.1	5.2	1.1	JESD: 4L/2P-SMT Simulation
FF1517	10.5	10.5	10.5	6.5	5.1	4.4	1.1	JESD: 4L/2P-SMT Simulation
FG256	33.6	25.1	18.4	21.2	19.7	19.1	3.9	SEMI: 4L/2P-SMT
FG324	29.4	26.0	21.1	19.3	17.2	16.5	3.4	SEMI: 4L/2P-SMT
FG456	23.5	19.6	16.5	15.5	14.1	13.6	2.2	SEMI: 4L/2P-SMT
FG556	13.7	13.6	13.5	9.7	9.4	9.4	2.1	SEMI: 4L/2P-SMT
FG676	16.7	16.6	16.6	13.2	12.0	11.5	2.0	SEMI: 4L/2P-SMT
FG680	11.1	10.8	10.4	7.5	6.2	5.6	0.9	SEMI: 4L/2P-SMT
FG860	10.5	10.2	10.0	7.2	5.9	5.4	0.8	SEMI: 4L/2P-SMT
FG900	14.1	13.7	13.5	9.8	9.5	9.5	2.0	Estimated
FG1156	13.7	13.4	13.2	9.7	9.2	9.0	2.0	JESD: 4L/2P-SMT Simulation
FT256	34.6	30.9	27.5	26.2	24.4	23.7	4.3	SEMI: 4L/2P-SMT
HQ160	16.5	15.6	14.7	10.8	8.6	7.7	2.0	SEMI: 4L/2P-SMT
HQ208	16.7	15.8	14.4	10.9	8.7	7.8	2.1	SEMI: 4L/2P-SMT
HQ240	14.5	13.2	11.8	9.1	7.3	6.5	1.5	SEMI: 4L/2P-SMT
HQ304	11.3	10.6	10.0	7.1	5.6	4.9	1.1	SEMI: 4L/2P-SMT

Table 1: **Summary of Thermal Resistance for Packages *(Continued)***

Pkg-Code	θ_{JA} still air (Max) °C/Watt	θ_{JA} still air (Typ) °C/Watt	θ_{JA} still air (Min) °C/Watt	θ_{JA} 250 LFM (Typ) °C/Watt	θ_{JA} 500 LFM (Typ) °C/Watt	θ_{JA} 750 LFM (Typ) °C/Watt	θ_{JC} (Typ) °C/Watt	Comments
HT144	19.1	18.5	18.2	12.6	10.7	10.1	2.1	SEMI: 4L/2P-SMT
HT176	15.6	15.3	15.2	10.4	8.9	8.4	2.0	SEMI: 4L/2P-SMT
HT208	13.6	13.4	13.3	9.0	7.6	7.2	1.9	SEMI: 4L/2P-SMT
MQ208	18.4	17.9	17.4	14.0	12.6	11.9	1.3	SEMI: 2L/0P-SMT
MQ240	16.8	16.7	16.4	12.0	10.8	10.5	1.2	SEMI: 2L/0P-SMT
PC20	87.3	82.3	72.0	62.1	55.5	51.8	24.2	SEMI: 2L/0P-SMT
PC28	67.6	66.1	63.0	49.8	44.6	41.6	17.8	SEMI:Socketed
PC44	53.7	46.5	42.3	35.1	31.4	29.3	14.9	SEMI:Socketed
PC68	46.2	41.9	38.4	31.6	28.2	26.4	9.5	SEMI:Socketed
PC84	41.7	33.3	27.9	25.8	20.8	16.8	5.6	SEMI:Socketed
PD8	83.0	78.9	71.3	59.4	53.2	49.6	21.5	SEMI:Socketed
PD48	43.2	43.2	43.2	32.6	29.1	27.2	11.6	SEMI:Socketed
PG68	38.8	37.0	34.1	25.6	19.9	17.3	7.8	SEMI:Socketed
PG84	38.5	34.4	31.3	23.8	18.5	16.1	6.0	SEMI:Socketed
PG120	37.8	27.8	24.6	19.3	15.2	13.3	4.0	SEMI:Socketed
PG132	32.0	28.7	23.9	20.3	16.7	14.8	2.9	SEMI:Socketed
PG144	25.8	24.5	23.3	17.4	14.3	12.6	3.7	SEMI:Socketed
PG156	25.6	23.9	20.7	14.9	11.6	10.3	2.7	SEMI:Socketed
PG175	25.2	23.3	19.9	14.5	11.3	10.0	2.6	SEMI:Socketed
PG191	25.7	21.8	18.5	15.5	12.7	11.2	1.5	SEMI:Socketed
PG223	25.3	21.1	17.7	15.0	12.3	10.8	1.5	SEMI:Socketed
PG299	21.0	17.3	15.1	10.4	8.7	8.3	2.0	SEMI:Socketed
PG411	16.1	14.7	14.3	9.5	7.4	6.5	1.4	SEMI:Socketed
PG475	15.1	14.6	14.3	9.4	7.3	6.4	1.4	SEMI:Socketed
PG559	13.7	13.4	13.2	8.6	6.7	5.9	1.3	Estimated
PP132	35.4	34.4	32.8	23.5	17.9	17.1	6.1	SEMI:Socketed
PP175	29.5	28.9	28.0	19.0	15.0	13.0	2.5	SEMI:Socketed
PQ44	52.2	51.3	50.1	39.8	36.4	35.4	12.4	SEMI: 4L/2P-SMT
PQ100	35.0	33.5	32.0	29.5	27.6	26.6	5.6	SEMI: 4L/2P-SMT
PQ160	38.1	31.8	20.6	23.5	20.8	19.2	5.0	SEMI: 4L/2P-SMT
PQ208	36.9	30.4	18.9	22.4	19.8	18.4	4.8	SEMI: 4L/2P-SMT
PQ240	28.5	19.9	14.0	14.7	13.0	12.0	3.8	SEMI: 4L/2P-SMT
SO8	147.1	147.1	147.1	112.2	104.6	98.6	48.3	IEEE-(Ref)
SO16	106.0	106.0	106.0	-	-	-	47.0	Vendor data
SO20	86.0	86.0	86.0	65.4	61.1	57.6	36.0	Vendor data
SO24	80.0	80.0	80.0	60.8	56.8	53.6	28.0	Vendor data
TQ44	76.5	76.2	75.8	59.2	50.0	45.1	8.2	SEMI: 4L/2P-SMT
TQ100	39.5	31.8	30.6	25.9	24.0	23.5	7.5	SEMI: 4L/2P-SMT
TQ128	31.5	30.6	30.0	26.9	25.2	24.3	5.3	SEMI: 4L/2P-SMT

Table 1: **Summary of Thermal Resistance for Packages *(Continued)***

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TQ144	57.6	33.5	29.8	26.1	22.3	20.9	5.5	SEMI: 4L/2P-SMT
TQ160	28.9	28.9	28.9	21.8	18.5	17.0	5.6	SEMI: 4L/2P-SMT
TQ176	29.7	28.1	26.7	21.3	18.0	16.5	5.3	SEMI: 4L/2P-SMT
VO8	160.0	160.0	160.0	137.6	129.6	123.2	60.0	Estimated
VO24	76.0	76.0	76.0	57.8	54.0	50.9	28.0	Estimated
VQ44	46.9	42.2	38.9	35.2	32.8	32.1	8.2	SEMI: 4L/2P-SMT
VQ64	46.9	42.3	39.3	35.2	32.9	32.1	8.2	SEMI: 4L/2P-SMT
VQ100	53.2	38.8	32.4	32.3	30.1	29.3	9.3	SEMI: 4L/2P-SMT

Notes:

1. The maximum, typical and minimum numbers reported here are based on numbers for all the devices for the specific package at the time of compilation. The numbers do not necessarily reflect the absolute limits of that packages. Specific device data should lie within the limits. Packages used for a broader spectrum of devices have a wider range in the table. Specific device data in a package may be obtained from the factory.
2. Data is listed alphabetically by the Xilinx package code. Package configurations and drawings corresponding to these codes may be found in the section of the databook with package outline drawings.
3. In the comment section, 2L/0P-SMT implies that the data was taken from a surface mount type I board or low conductivity type board — no internal planes on the board.
4. 4L/2P-SMT (2S/2P) implies that the data was taken from a 4-layer SMT board incorporating two internal planes. We have included SEMI and JESD to designate what method the data came from.
5. Socketed data is also specified where applicable.
6. Thermal data is in degree Celsius/Watt. **JA** refers to θ_{JA}. Airflow is in Linear Feet per minute (LFM). 500 LFM = 2.5 Meters per Second.

Application of Thermal Resistance Data

Thermal resistance data is used to gauge the IC package thermal performance. There are several ways to express the thermal resistance between two points. The following are a few of them:

- θ_{JA} = Junction to ambient thermal resistance (°C/W).
- θ_{JC} = Junction to case thermal resistance (°C/W)
- θ_{JB} = Junction to board thermal resistance (°C/W)
- θ_{CA} = Case to ambient thermal resistance (°C/W)
- θ_{CS} = Case to heatsink thermal resistance (°C/W)
- θ_{SA} = Heatsink to ambient thermal resistance (°C/W)

Other thermal parameters include

- Ψ_{JB} = Junction to board thermal characteristic parameter (°C/W)
- Ψ_{JC} = Junction to case thermal characteristic parameter (°C/W)

θ_{JC} measures the internal package resistance to heat conduction from the die surface, through the die mount material to the package exterior. θ_{JC} strongly depends on the package material's heat conductivity and geometrical considerations.

θ_{JA} measures the total package thermal resistance including θ_{JC}. θ_{JA} depends on the package material properties and such external conditions as convective efficiency and board mount conditions. For example, a package mounted on a socket may have a θ_{JA} value 20% higher than the same package mounted on a 4-layer board with power and ground planes.

In general θ_{MN} expresses the thermal resistance between point **M** and **N**. In the above expression the "source" and "end" points are indicated.

In situations where a heatsink is used with a heatsink compound, thermal resistance of heatsink is referenced as θ_{SA} (sink-to-ambient) and the attached material as θ_{CS} (case-to-heatsink). These thermal resistances may be added. For example, $\theta_{JA} = \theta_{JC} + \theta_{CS} + \theta_{SA}$, is an expression used in Heatsink situations with interface material resistance θ_{CS}.

Thermal Data Usage

The following are some data requirements for using thermal resistance in an application.

- Xilinx supplied data:
  - θ_{JA} — quoted from Xilinx database
  - θ_{JC} — quoted from Xilinx database
  - θ_{SA} — quoted by heatsink supplier
- Items that the user may need to supply.
  - T_J-max:
    - This may go as high as the absolute maximum Temperature for the package — typically 125°C to 135°C for plastic.
    - Beyond 85°C for commercial specified part, speed files may have to be derated. The temperature limit before derating is activated is higher for industrial grade and military temperature grade parts.
    - The user will need to pick a T_J-max for reliability considerations, and plan the thermal budget around that.
  - T_A: Ambient in a system
    - This is also another variable that the user can control. Typically this is set to approximately 45°C to 55°C.
- Items usually calculated:
  - Power dissipation. The thermal equation may be used to determine power range that can satisfy some given conditions.
  - Also if power is known, T_J-max may be calculated from the equations.
  - If the temperature on the top of a bare part is well monitored in a system (not the way θ_{JC} is measured) the thermal parameter Ψ_{JC} may be used to get junction temperature
  - Similarly a well monitored board temperature can be used to predict junction with the Ψ_{JB} parameter.

In non-heatsink situations, the following inequality formula should hold.

$$T_J(max) > \theta_{JA} * P_D + T_A$$

The two examples below illustrate the use of the above inequality formula. Specific packages have been used in the examples but any package; Quad, BGA, FGs, or even FlipChip based BGs will be applicable.

Example 1:

The manufacturer's goal is to achieve Tj (max) < 85°C

A module is designed for a Ta = 45°C max.

An XCV300 in a FG456 has a θ_{JA} = 16.5°C/watt. θ_{JC} = 2.0°C/Watt.

Given a XCV300 with a logic design with a rated power P_D of 2.0 Watts.

With this information, the maximum die temperature can be calculated as:

$$T_J = 45 + (16.5 \times 2.0) = 78°C.$$

The system manufacturer's goal of T_J < 85°C is met in this case.

Example 2:

A module has a T_A = 55°C max.

The Xilinx FPGA XC4013E is in a PQ240 package (HQ240 is also considered).

A logic design in XC4013E is determined to be 2.50 Watts. The module manufacturer's goal is to achieve T_J(max.) < 100°C.

Table 2 shows the package and thermal enhancement combinations required to meet the goal of T_J < 100°C.

Table 2: **Thermal Resistance for XC4013E in PQ240 and HQ240 Packages**

Device Name	Package	θ_{JA} still air	θ_{JA} (250 LFM)	θ_{JA} (500 LFM)	θ_{JA} (750 LFM)	θ_{JC}	Comments
XC4013E	PQ240	23.7	17.5	15.4	14.3	2.7	Cu, SMT 2L/0P
XC4013E	HQ240	12.5	8.6	6.9	6.2	1.5	4-Layer Board data

Notes:

1. Possible Solutions to meet the module requirements of 100°C :
   - 1a. Using the standard PQ240: T_J = 55 + (23.7 x 2.50) = 114.25°C.
   - 1b. Using standard PQ240 with 250 LFM forced air: T_J = 55 + (17.5 x 2.50) = 98.75°C
   - 2a. Using standard HQ240: T_J = 55 + (12.5 x 2.50) = 86.25°C
   - 2b. Using HQ240 with 250 LFM forced air: T_J = 55 + (8.6 x 2.50) = 76.5°C.

For all solutions, the junction temperature is calculated as: T_J = Power x θ_{JA} + T_A. All solutions meet the module requirement of less than 100°C, with the exception of the PQ240 package in still air. In general, depending on ambient and board temperatures conditions, and most importantly the total power dissipation, thermal enhancements — such as forced air cooling, heat sinking, etc. may be necessary to meet the T_J(max) conditions set.

Heatsink Calculation:

Example illustrating the use of heatsink:

Device is **XCV1000E-FG680** –

There is a need for external thermal enhancements

Supplied data from Xilinx on XCV1000E-FG680

Package Code	JA(0) °C/W	JC °C/W	JA-250 °C/W	JA-500 °C/W	JA-750 °C/W
FG680	10.6	0.9	7.5	6.1	5.6

- Customer requirements
  - Ta = 50°C
  - Power = 8.0 Watts (user's estimate)
  - User does not want to exceed T_J(max) of 100°C
- Determination with base Still Air data:
  - $T_J = T_A + (\theta_{JA}) * P$
  - T_J = 50 + 8 * 10.6 = 134.8°C
  - Unacceptable! θ_{JA} in still air will not work since the 134.8°C is beyond the stated goal of 100°C or less.
- Calculating acceptable Thermal resistance:
  - Determine what θ_{JA} will be required to stay below 100°C with the 8 Watts power?
  - Thermal budget = (T_J – T_A) = 50°C.
  - θ_{JA} = (50)/8 = 6.25°C/Watt.

- The package and any enhancement to it need to have an effective thermal resistance from the junction to ambient less than 6.25°C/Watt. That becomes the goal any thermal solution ought to meet.

- **Solution Options**:
  - The bare package with 500LFM (2.54 meters/s) of air will give θ_{JA} = 6.1°C/Watt. (from the data table above). That will be a workable option, if that much airflow will be tolerable.
  - Heatsink calculation. With a heatsink, heat will now pass through the package (θ_{JC}) then through an interface material (θ_{CS}), and from the heatsink to ambient (θ_{SA}). This can be expressed as follows:
    - $\theta_{JA} \leq \theta_{JC} + \theta_{CS} + \theta_{SA}$
    - $6.25 \leq 0.9+0.1+ \theta_{SA}$

    where
    - 6.25°C/Watt is the condition to be met
    - 0.9°C/Watt — θ_{JC} from data.
    - 0.1°C/Watt — θ_{CS} from interface material data.
  - From above $\theta_{SA} \leq 5.25$°C/Watt.
  - Objective will be to look for a Heatsink with θ_{SA} **< 5.25°C/Watt** that meet the physical constraints in the system.
  - Passive Heatsink with some air flow — 250 LFM (1.25m/s) can be selected.
  - Active heatsinks — small low profile heatsinks with DC fans may be possible to use.

Thermal Data Comparison

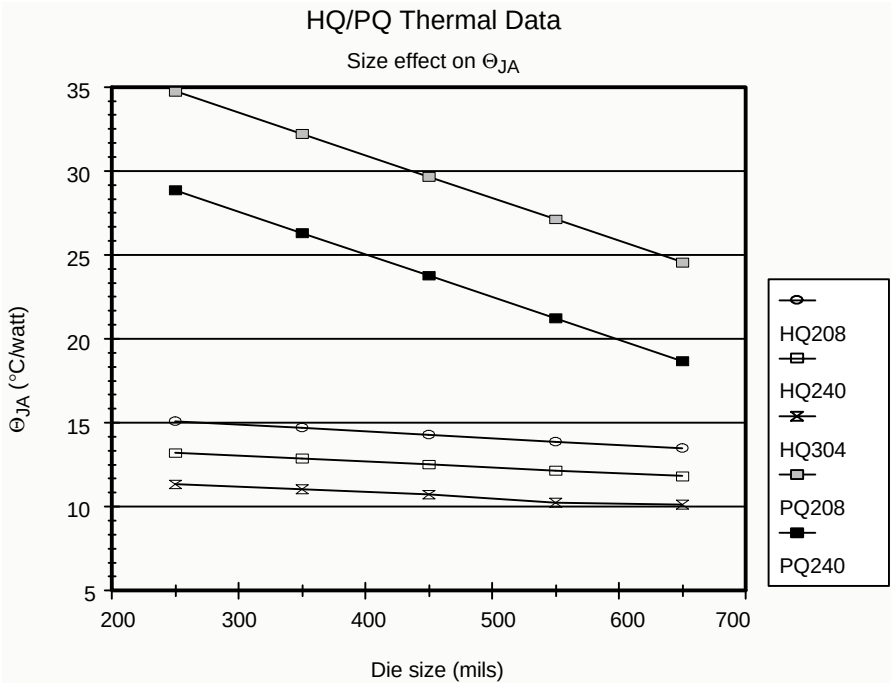


Figure 2: **HQ/PQ Thermal Data**

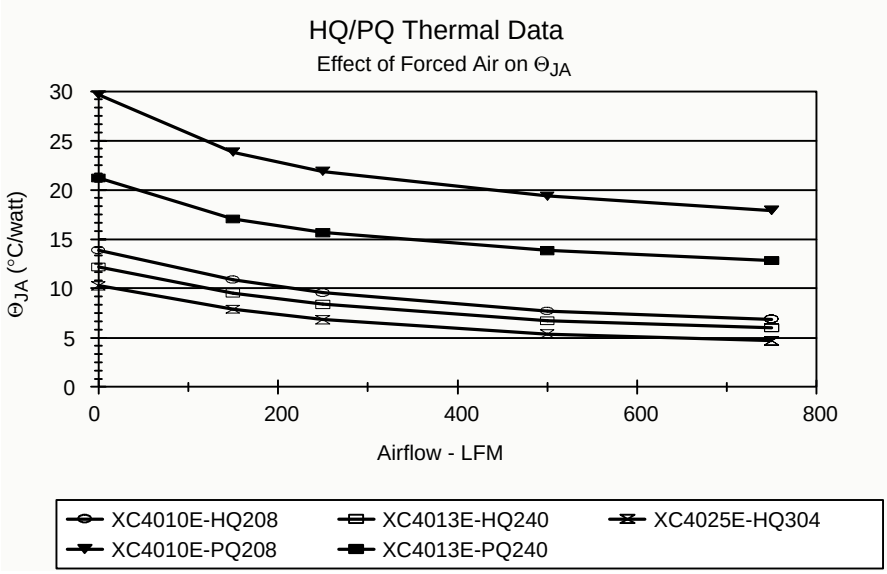


Figure 3: **HQ/PQ Thermal Data**

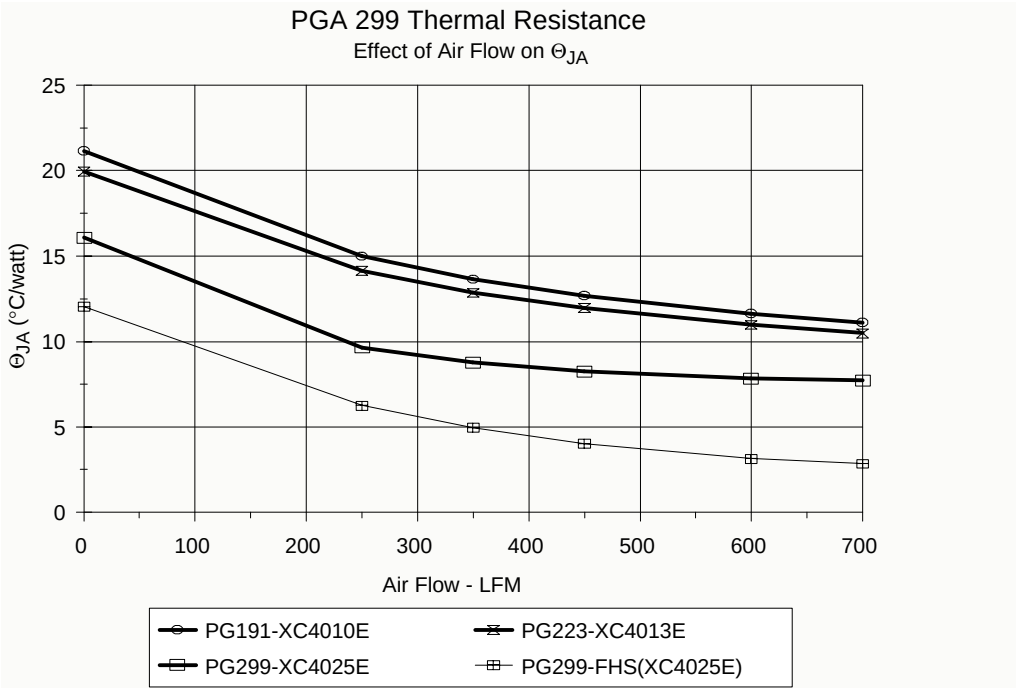


Figure 4: **PGA299 Thermal Resistance**

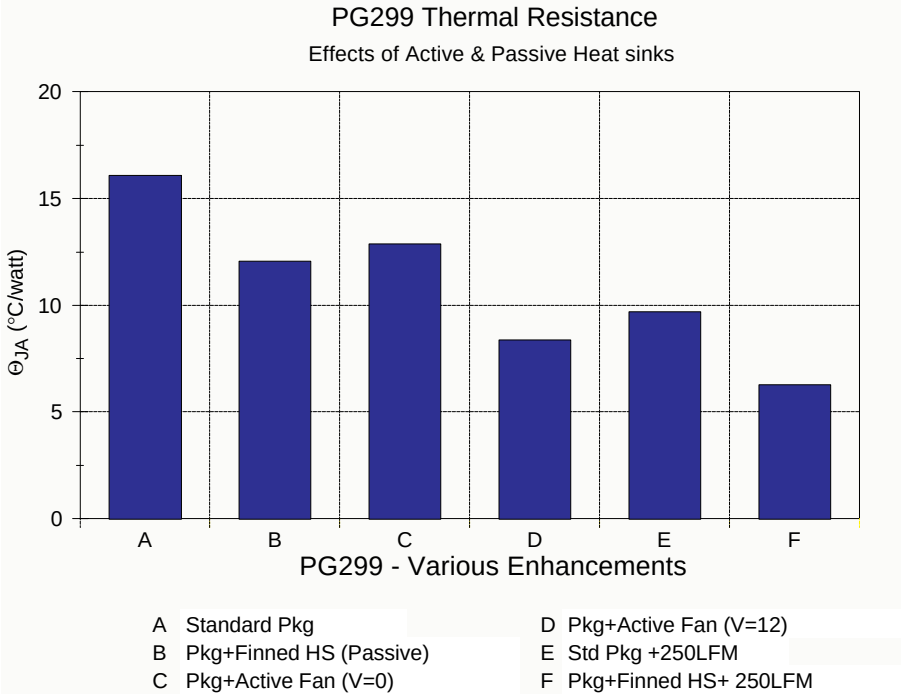


Figure 5: **PG299 Thermal Resistance**

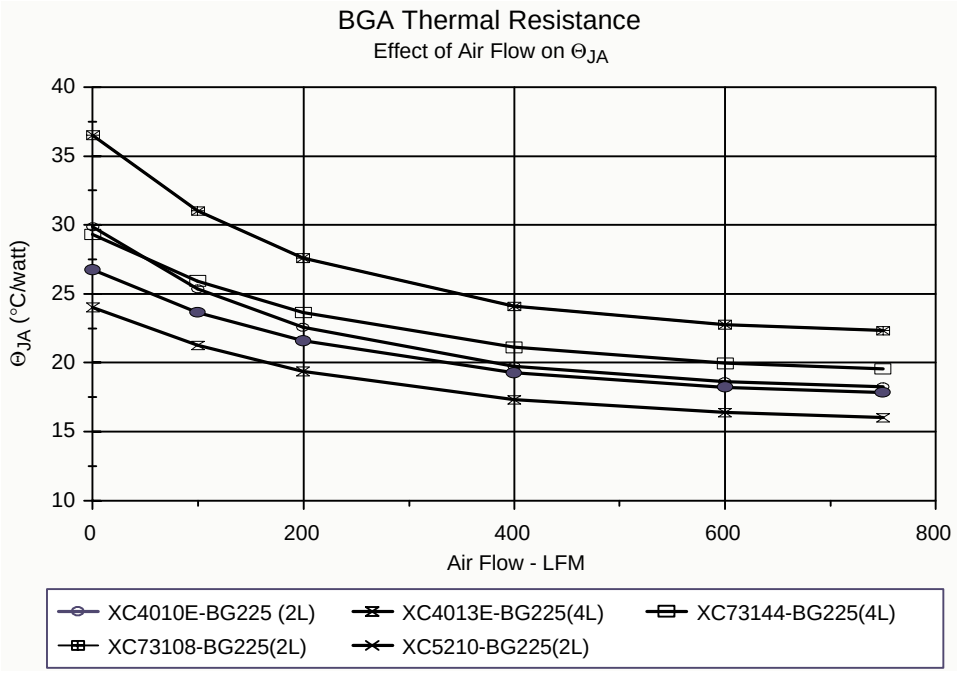


Figure 6: **BGA Thermal Resistance**

Some Power Management Options

Due to the variety of applications that the FPGA devices are used in, it is a challenge to anticipate the power requirements and thus the thermal management needs a particular user may have. While Xilinx programmable devices may not be the dominating power consumers in

some systems, it is conceivable to have high gate count FPGA devices that are exercised sufficiently to generate considerable amount of heat.

Figure 7: **Enhanced BGA with Low Profile Retainer Type Passive Heatsinks**

In general, high I/O and high gate count Virtex™ class devices stand the potential of being clocked to produce high wattage. Being aware of this potential in power needs, the package offering for these devices include medium and high power capable package options. This allows system designer to further enhance these high-end BGA packages to handle more power.

When the actual or estimated power dissipation appears to be more than the specification of the bare package, some thermal management options can be considered. The accompanying Thermal management chart illustrates the incremental nature of the recommendations — ranging from simple airflow to schemes that can include passive heatsinks, and active heatsinks.

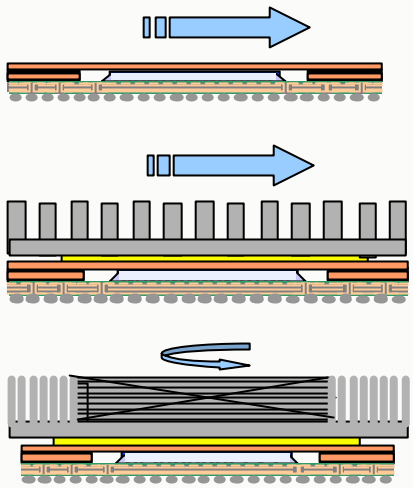
Low End 1-6 Watts	Bare Package with Moderate Air 8-12˚C/Watt	Bare Package. Package may be used with moderate airflow within a system.	
Mid Range 4-10 Watts	Passive H/S + Air 5-10˚C/Watt	Package used with various forms of Passive Heatsinks and Heat spreader techniques.	
High End 8-20 Watts	Active Heatsink 2-3˚C/Watt or better	Package used with Active Heatsinks TEC and Board level Heat spreader techniques.	

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Figure 8: **Thermal Management — Incremental Options**

The use of heatpipes, and even liquid-cooled heat plates may be considered in the extreme for some of these packages. Details on the engineering designs and analysis of some of these suggested considerations may require the help of thermal management consultants. The

references listed at the end of this section can provide heatsink solutions for industry standard packages.

Some of the options available in thermal management may include the following:

- A Xilinx lower voltage version of the equivalent circuit in the same or similar package. With the product and speed grade of choice, up to a 40% power reduction can be anticipated for a 5.0V to a 3.3V version. Not all products have equivalent lower voltage versions.
- Most high gate count Xilinx devices come in more than two package types. Explore thermally enhanced package options available for the same device. The Quad packages and some BGA packages have heat enhancement options. Typically 25% to 40% improvement in thermal performance can be expected from these heatsink embedded packages.
- In a system design, natural convection can be enhanced with venting in the system enclosure – This will effectively lower the Ta, and increase available thermal budget for moderate power dissipation.
- The use of forced air – fans will be the next step from the natural convection, and it is an effective way to improve thermal performance. As seen on the graphs and the calculations above, forced air (200-300 LFM) can reduce junction to ambient thermal resistance by up to 30%.
- For moderate power dissipation (2 to 5 Watts), the use of passive heatsinks and heatspreaders attached with thermally conductive double-sided tapes or retainers can offer quick solutions.

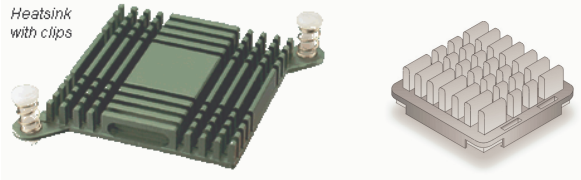

Figure 9: **Heatsink with Clips**

- The use of lightweight finned external passive heatsinks can be effective for dissipating up to 8 Watts on some packages. If implemented with forced air as well, the benefit can be a 40% to 50% reduction as illustrated in the XCV1000E-FG680 example. The more efficient external heatsinks tend to be tall and heavy. To help prevent component joint from heatsink induced stress the use of spring loaded pins or clips that transfer the mounting stress to a circuit board is advisable whenever a bulky heatsink is considered. The diagonals of some of these heatsinks may be designed (see accompanying picture) with extensions to allow direct connection to the board.
- Exposed Metal heatsink packages: All thermally enhanced BGAs with die facing down (including these package codes - BG352, BG432, BG560, FG680, FG860, and FlipChip BGAs) are offered with exposed metal heatsink at the top. These are considered high-end thermal packages and they lend themselves to the application of external heatsinks (passive or active) for further heat removal efficiency. Again precaution should be taken to prevent component damage when a bulky heatsink is attached.
- Active heatsinks may include simple heatsink incorporating a mini fan or even Peltier Thermoelectric Cooler (TECs) with a fan to carry away any heat generated. Any consideration to apply TEC in heat management should require consultation with experts in using the device since these devices can be reversed and cause damage to components. Also condensation can be an issue.
- Molded packages (FG456, FG676, FG1156, PQs etc) without exposed metal at the top may also use these heatsinks at the top for further heat reduction. These BGA packages are similar in construction to those used in Graphic cards in the PC applications, and heatsinks used for those applications can easily be used for these packages as well. In

this case the Junction to Case resistance will be the limiting consideration.

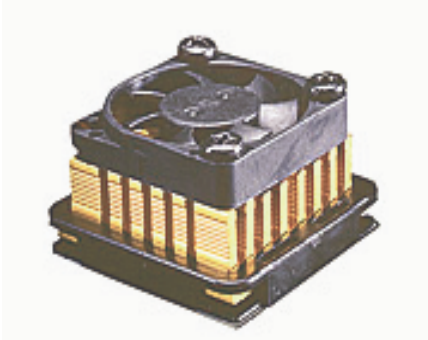

Figure 10: **Example of Active Heatsink for BGA (Malico)**

- Outside the package itself, the board on which the package sits can have a significant impact on thermal performance. Board designs may be implemented to take advantage of the board's ability to spread heat. Heat flows to the outside of a package and is sunk into the board to be conducted away – through heatpipes or by normal convection. The effect of the board will be dependent on the size and how it conducts heat. Board size, the level of copper traces on it, the number of buried copper planes all lower the junction-to-ambient thermal resistance for a package mounted on it. Some of the heatsink packages – like HQ, with the exposed heatsink on the board side can be glued to the board with thermal compound to enhance heat removal into the board. BGA packages with full matrix of balls can be cooled with this scheme. Users need to be aware that a direct heat path to the board from a component also exposes the component to the effect of other heat sources – particularly if the board is not cooled effectively. An otherwise cooler component can be heated by other heat contributing components on the board.

References

The following websites have additional information on heat management. The sites carry the contact information:

Websites for Heatsink Sources

- http:// www.wakefield.com
- http:// www.aavid.com or www.thermalloy.com
- http://www.chipcoolers.com
- http:// www.metalsgroup.com
- http://www.malico.com.tw
- http://www.pinfin.com
- http:// www.intricast.com
- http:// www.innovalue.com
- http://www.alphanovatech.com
- http:// www.tennmax.com
- GlobalWin: http://www.globalwin.com.tw
- http://www.avc.com.tw
- ALPHA: http://www.micforg.co.jp
- COFAN USA http://www.cofan-usa.com

Websites for interface material sources

- Power Devices — http://www.powerdevices.com
- Chomerics — http://www.chomerics.com
- Bergquist Company — http://www.bergquistcompany.com

- AOS Thermal Compound — http://www.aosco.com

Xilinx does not endorse these vendors nor their products. They are listed here for reference only. Any materials or services received from the vendors should be evaluated for compatibility with Xilinx components.

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
12/19/01	1.0	Initial Xilinx release.
07/26/02	1.1	Fixed packaging code on page 10 from FG6080 to FG680. Added disclaimer on page 1.