

Xilinx Lead Free Packages

Introduction

Since the beginning of 2001, Xilinx has been proactively working with our suppliers, customers, and various industry consortia to understand, develop and qualify suitable material sets and processes for lead free applications. Our initiative to develop lead free packaging solutions is in a response to possible legislative mandates to ban lead from electronic products and to meet the growing needs of our valued customers to supply environmentally friendly products.

Product Introduction Schedule

Xilinx will be offering lead free products in phases. Initially, only a handful of selected devices/packages will be offered and mainly to our beta customers. Low volume production of limited PQFPs and BGAs products will begin in first quarter of 2003. The list will grow to include other devices/packages based on strategic impact. Customers are encouraged to discuss their lead free requirements with Xilinx sales representatives.

Part Number

Lead free products are differentiated from conventional products by the package code. Hence, lead free products have different part numbers. No unique character or logo will be marked on the part. Lead free parts can be identified by the package code that is marked on the part. The package code will incorporate an extra "G" character (i.e., TQ144 is the package code for conventional TQFP 144Ld product. TQG144 is the package code for lead-free TQFP 144ld product).

Qualification

Xilinx lead free packages are currently qualified per JEDEC level 3 moisture resistance with peak reflow temperature of 260°C. Reliability tests include temperature cycles and THB. Additionally, Xilinx works with suppliers and partners to perform board level and solderability tests. Data for these tests are available upon request.

Material Sets

By collaborating with our suppliers, Xilinx sources the best material sets for lead free applications. The material sets must be reliable and robust to meet the requirement of higher reflow temperature (up to 260°C max.), which is necessary for lead free soldering.

Currently, the mold compound that Xilinx uses for lead free packaging is "green." Sumitomo's G700/G770 family of mold compounds is Br/Sb/Cd/PBB/PBDE free and does not use flame retardant.

For the solder finish/material, the leaded packages have pure matte tin plating finish and the array packages have Sn/Ag/Cu solder balls. These materials are industry preferred materials and are chosen due to their availability, lower cost, and reliability.

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Table 1 summarizes the material sets being used in Xilinx lead free packaging.

Table 1: Lead Free Material Se

Package	Mold Compound	Die Attach	Plating/Solder Ball Alloy
VQGs, TQGs, PQGs	Sumitomo G700	Ablebond 3230	100% Matte Sn
CSG48	Sumitomo G770	Ablebond 2300	Sn3.9Ag0.6Cu
CSG144	Sumitomo G770	Ablebond 2025	Sn3.9Ag0.6Cu
BGG/FGG (Cavity Up)	Sumitomo G770	Ablebond 2300	Sn3.9Ag0.6Cu
BGG/FGG (Cavity Down, Copper based)	Dexter CBO-260AT	Hitachi EN4900-1	Sn3.9Ag0.6Cu

Material Properties

The lead-free material sets are selected for their superior properties and low moisture absorption. Table 2 summarizes the material property data for each material.

Table 2: Material Properties

	Mold Compound/Encapsulant			Die Attach			Plating/Solder Ball	
Package	G770	G700	CBO-260AT	A/B 2300	A/B 3230	EN4900-1	100Sn	SnAgCu
CTE ₁ (ppm/°C)	8	12	17	60	80	127	26	-
CTE ₂ (ppm/°C)	37	49	67	129	205	158	-	-
Tg (°C)	130	130	149	0.8	37	19	232 (melting point)	217 (melting point)
Thermal Conductivity (W/m• °C)	0.88	0.88	0.70	0.60	1.40	4	73	57
Modulus (MPa) -25°C	25480	18620	12700	1800	2900	350	-	-
Modulus (MPa) - 240°C	588	588	600	240	90	N/A	-	-

Solder Reflow Guideline (SMT)

SnAgCu alloy of Sn3.9Ag0.6Cu is currently the industry's widely accepted soldering alloy for lead-free solder reflow applications due to its lower melting temperature (217°C), lower cost, and good long term reliability. Data from various sources indicate that the SnAgCu system has equal or better thermal/mechanical fatigue life performance compared to eutectic tin/lead solder. However, this alloy has a higher melting temperature (217°C) with peak temperature during reflow ranging from 235-260°C. Thus, assembly processes must be optimized accordingly to achieve the best yields and reliability.

Optimal Profile

The optimal profile must take into account the solder paste/flux used, the size of the board, the density of the components on the board, and the mix between large components and smaller, lighter components. Profiles should be established for all new board designs using thermocouples at multiple locations on the component. In addition, if there are mixture of devices on the board, then the profile should be checked at various locations on the board to ensure that the minimum reflow temperature is reached to reflow the larger components and at the same time, the temperature does not exceed the threshold temperature that may damage the smaller, heat sensitive components.

In general, a gradual, linear ramp into a spike has been shown by various sources to be the optimal reflow profile for lead free solders (Figure 1). This profile has been shown to yield better wetting and less thermal shock than conventional ramp-soak-spike profile for tin/lead system. Also, most sources have indicated that SnAgCu can already reach full liquidus temperature at 235°C. Thus, it may not be necessary to ramp to peak temperature of 260°C. Futhermore, reflowing at high peak temperature (260°C and above) may damage the heat sensitive components and cause the board to warp. Hence, it is recommended to use a reflow profile with the lowest peak temperature possible.

For sophisticated boards with a large mix of large and small components, it is critical to minimize the delta T across the board (less than 10°C) to minimize board warpage and thus, attain higher assembly yields. This is accomplished by using a slower rate in the warm-up and preheating stages. A heating rate of less than 1°C/sec during the initial stage, in combination with a heating rate of not more than 3°C/sec throughout the rest of the profile is recommended.

Aside from the board, it is also important to minimize the temperature gradient on the component, between top surface and bottom side, especially during the cooling down phase. In fact, cooling is a crucial part of the reflow process and must be optimized accordingly. While a slow cooling rate may result in high assembly yields, it could lead to formation of thick intermetallic layers with large grain size; thereby, reducing the solder joint strength. On the other hand, faster cooling rate leads to smaller solder joint grain size, and hence resulting in higher solder joint fatigue resistance. However, overly aggressive cooling on stiff packages with large thermal mass may lead to cracking or package warpage because of the differential cooling effects between the top surface and bottom side of the component and between the component and the PCB materials.

The key is to have an optimized cooling with minimal temperature differential between the top surface of the package and the solder joint area. The temperature differential between the top surface of the component and the solder balls should be maintained at less than 7°C during the critical region of the cooling down phase of the reflow process. This critical region is the phase in which the balls are not completely solidified to the board yet, usually between the 200-217°C range. The best solution may be to divide the cooling section into multiple zones, with each zone operating at different temperatures to efficiently cool the parts.

Table 3 and Figure 1 provide guideline for profiling lead free solder reflow.

Profile Feature	Convection, IR/Convection
Ramp-up rate	1-3°C/second
Preheat Temperature	60-120 seconds
125-175°C	
Temperature maintained above 217°C	45-120 seconds
Time within 5°C of actual peak temperature	10-20 seconds
Peak Temperature	235°C min., 245°C typical, 260°C max. (depends on solder paste, board size, components mixture)
Ramp-down Rate	1-3°C/second
Time 50°C to Peak Temperature	3.5 minutes min, 5.0 minutes typical, 6 minutes max

Table 3: Guideline for Profiling Lead Free Solder Reflow



References

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Revision History

The following table shows the revision history for this document.

Date	Version	Revision		
12/09/02	1.0	Initial Xilinx release.		