XAPP628 (v1.0) December 4, 2002

Interfacing with the IDT TeraSync FIFO

Summary

The Virtex™-II series of FPGAs provide access and interface to a variety of on-chip and off-chip devices. In addition to the on-chip distributed RAM and block RAM features, Virtex-II FPGAs can interface to a variety of external high-speed memory devices. The combination of the high-speed selectable I/O resources and on-chip Digital Clock Manager (DCM) circuits enable a high-bandwidth interface to a high-speed, high-density FIFO. This application note presents an overview of a general interface between an IDT TeraSync™ FIFO and the Virtex-II FPGA.

Introduction

The IDT TeraSync FIFO delivers high-performance, low power (2.5V supply), high speeds (up to 225 MHz), high density (9 Mb), and flexible bus widths of x9, x18, x36, or x72. Other features of the TeraSync FIFO include selectable LVTTL/HSTL I/Os, echo read clock and enable, retransmit from mark, dedicated serial clock, small BGA packaging, and JTAG boundary scan functionality. All of these features can be easily implemented using the flexibility of the Virtex-II architecture. Before read and write operations can begin, some features in the TeraSync FIFO must be programmed during and after master reset. These features include selectable bus-matching widths, programmable offset registers, and selectable timing modes. By interfacing with all of the TeraSync FIFO inputs, the Virtex-II FPGA implements all the TeraSync FIFO features. This application note and accompanying reference design describes an interface between the Virtex-II device (XC2V1000) and the IDT TeraSync FIFO (IDT72T36125). Sample code is available in the reference design file for initializing the TeraSync FIFO and initiating read and write operations.

TeraSync FIFO at a Glance

- Up to 225 MHz high-speed operation
- Memory density options: 32 Kb, 64 Kb, 128 Kb, 256 Kb, 512 Kb, 1M, 2M, 5M, 9M
- x9, x18, x36 bus wide data port options
- User selectable HSTL/LVTTL inputs and/or outputs
- Echo Read Clock and Enable available for source synchronous clocking
- Mark and Retransmit option which resets read pointer to user marked position
- Programmable Almost Empty, Almost Full Flags to user defined values
- 208-pin or 240-pin Plastic Ball Grid Array (PBGA) with JTAG functionality
- Write Chip Select and Read Chip Select to control the read and write port individually
- Separate SCLK for serial programming of flag offsets
- Selectable timing modes: IDT Standard Mode or First Word Fall Through (FWFT) Mode
- Separate Output Enable control for putting data outputs into high-impedance

TeraSync Architecture

The IDT72T36125 FIFO is a 2.5V, 9 Mb deep, 36-bit wide device capable of operating up to 225 MHz. Figure 1 shows the overall architecture of this device.

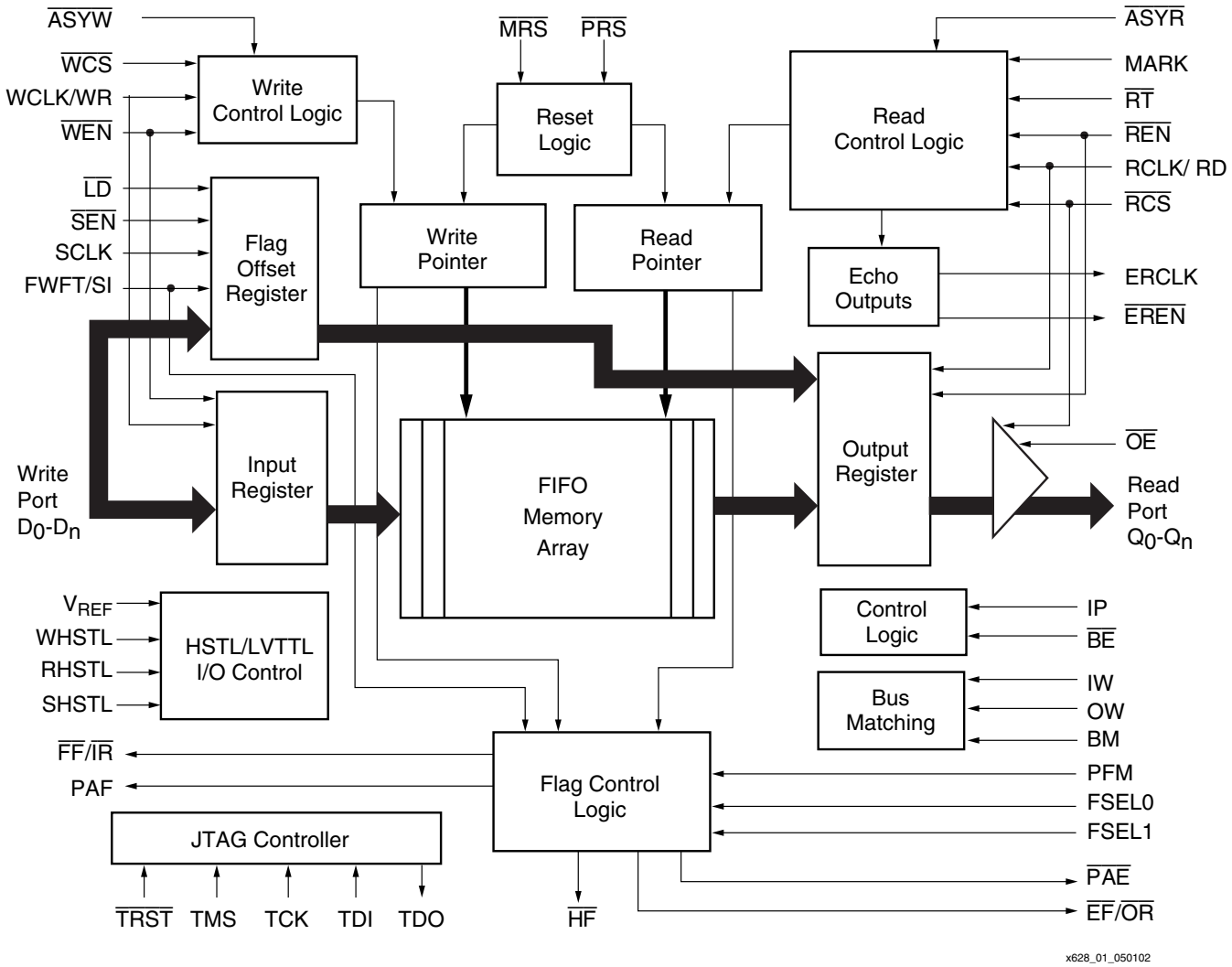

Figure 1: **Block Diagram of IDT's TeraSync FIFO**

The device has a data input port (D_n) and a data output port (Q_n), either can assume a 36-bit, 18-bit, or 9-bit bus width. The three input clocks are the read clock, write clock, and serial clock. All can be run independently and at different frequencies. Two read port enable signals, read enable and read chip select, control activity of the read port. Also, two write enable signals, write enable and write chip select, control activity of the write port.

By setting the state of the external control pins IW, OW, and BM, the device is capable of bus-matching. Any combination in 9-bit factors are possible, but one of the ports must be 36-bits wide. There are a total of five status flags: empty, full, half, partial empty, and partial full. By programming the offset registers, the last two, partial empty and partial full, are user programmable to a certain value. A specific location can be marked within the RAM array by the device. Data can be retransmitted starting from the marked location. In high-speed applications where data setup and hold times are stringent, an echo read clock and enable is available to synchronously align the input clock with output data. The echo enable is also used as an indicator guaranteeing data will be valid for reading.

Master Reset

The first operation to be performed before activation of the FIFO is a master reset. A master reset is required before the FIFO can be operational. It initializes the internal read and write pointers to the first location in the RAM array, as well as clearing all internal registers to zero. During master reset, input signals FWFT/SI, $\overline{LD}$, FSEL0, FSEL1, IP, PFM, $\overline{ASYR}$, $\overline{ASYW}$, $\overline{BE}$, $\overline{SEN}$, $\overline{RT}$, BM, IW, OW, WHSTL, RHSTL, SHSTL must be at a known state. The state of these signals initializes certain features within the FIFO. The master reset pulse is held Low for 10 clock cycles (30 ns minimum) to ensure proper reset. Once a proper reset is accomplished, the $\overline{PAF}$ should be High and $\overline{PAE}$ = Low, $\overline{EF}$/$\overline{OR}$ = Low and $\overline{FF}$/$\overline{IR}$ = High (in the IDT standard mode). The flowchart in Figure 2 shows the FIFO's order of operation.

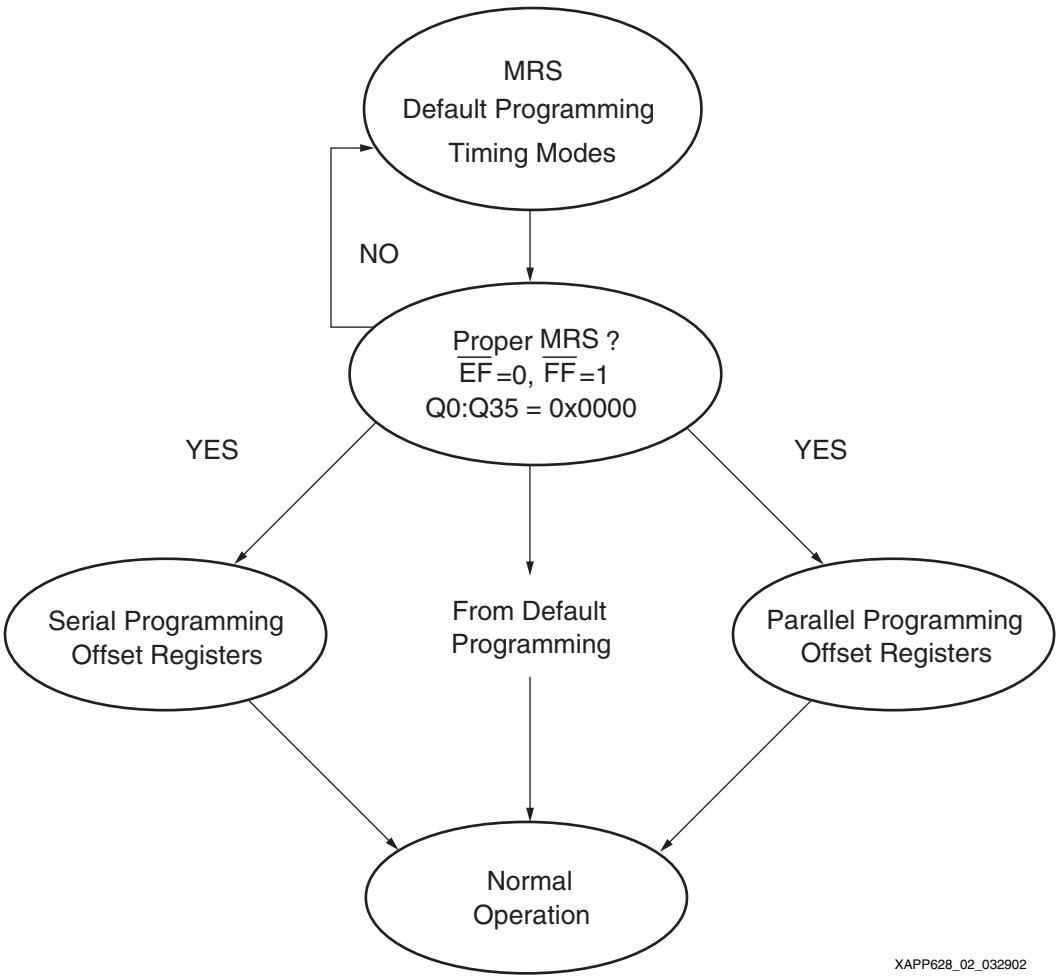

Figure 2: **TeraSync FIFO Initialization Flowchart**

Four signals must be held High during master reset: read enable ($\overline{REN}$), write enable ($\overline{WEN}$), retransmit ($\overline{RT}$), and serial enable ($\overline{SEN}$). Ten input signals are available to be tied to a known state. Table 1 summarizes the FPGAs controlling input signals.

Table 1: **How to Connect Input Signals**

FPGA Controlled	Tied to a Known State
$\overline{MRS}$, $\overline{PRS}$, $\overline{REN}$, $\overline{RCS}$, $\overline{WEN}$, $\overline{WCS}$, $\overline{OE}$, FWFT/SI, $\overline{ASYR}$, $\overline{ASYW}$, $\overline{LD}$, PFM, $\overline{SEN}$, FSEL0, FSEL1, $\overline{RT}$, MARK	OW, IW, BM, WHSTL, RHSTL, SHSTL, $\overline{BE}$, IP

Programming Flag Offsets

The Almost Full and Almost Empty flag offset values are user programmable. Programming the flag offsets should occur either during or right after master reset. There are three ways to program the offset values: either by serial loading, parallel loading, or using default settings. Serial and parallel programming occurs after master reset, provided a proper master reset is initialized. Default programming must occur during master reset. The values are selected based on the state of the FSEL0, FSEL1, and $\overline{LD}$ signals. Figure 3 shows the relevant signals for master reset and default programming flag offsets.

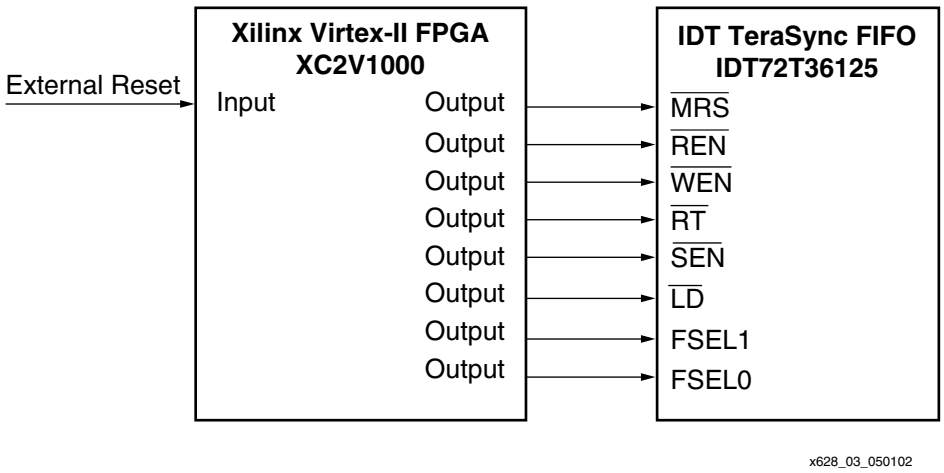

Figure 3: **Relevant Signals for Master Reset and Default Programming Controlled by an FPGA**

Default Programming

Offset values can be programmed to one of the eight default values associated with the TeraSync FIFO by setting the OW, IW, and BM pins to a defined state. The eight offset values available are listed in Table 2 of the IDT TeraSync data sheet. The sample Verilog code (1) for master reset and default programming is included in the reference design file on the IDT web site.

Serial Programming

Offset values can be programmed to a specific value using serial programming. This is achieved by using a combination of the $\overline{LD}$, $\overline{SEN}$, SCLK, and SI input pins. Serial programming can occur only after a proper master reset is accomplished. Data from the SI input are written one bit per each rising edge of SCLK when $\overline{LD}$ and $\overline{SEN}$ are Low. The total number of bits required to program the offset registers varies depending on the density of the device. For a list of the total number of bits, please refer to Figure 3 in the TeraSync 36-bit FIFO data sheet.

In serial programming, individual registers cannot be programmed selectively. The empty offset register is programmed first followed by the full offset register, all in one continuous cycle before setting the $\overline{LD}$ and/or $\overline{SEN}$ to inactive. Figure 4 is a block diagram of signals associated with serial and parallel programming along with sample Verilog code (2) for serial programming of the IDT72T36125 $\overline{PAE}$ and $\overline{PAF}$ offset registers in IDT standard mode is included in the reference design file on the IDT web site. The offset registers can not be read serially.

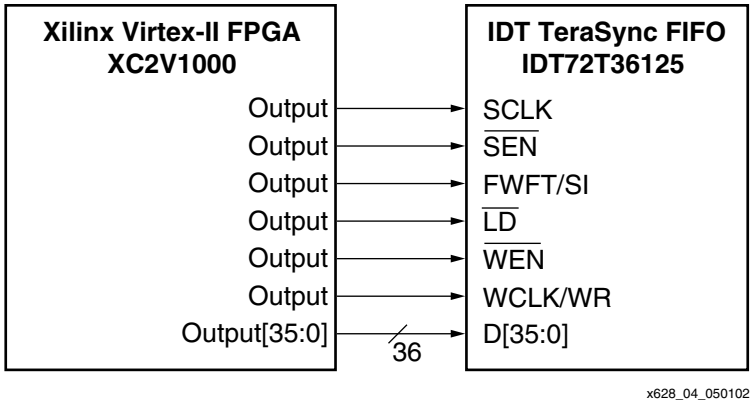

Figure 4: **Signals Relevant for Serial and Parallel Programming of PAE and PAF Registers**

Parallel Programming

Another method of programming the offset registers is parallel programming. This is achieved by using a combination of the LD, WCLK, WEN and data input pins D[35:0]. Similar to serial programming, parallel programming can occur only after a proper master reset is accomplished. In parallel programming, data from the input ports D[35:0] are written into the offset registers on every rising edge of WCLK when LD and WEN are deasserted Low. The implementation of bus-matching and the density of the FIFO determines the number of write cycles.

For a 36-bit input bus width, two write cycles are required to program the offset register. The first write-cycle programs the PAE offset register and the second programs the PAF offset register. If bus-matching is implemented, then the number of writes will vary depending on the bus-width selected and the density of the FIFO. A programming sequence summary of the offset flag is listed in Figure 3 of the TeraSync 36-bit FIFO data sheet. The sample Verilog code (3), associated with parallel programming of the IDT72T36125 with an x36 input and an x36 output bus configuration for parallel programming of PAE and PAF offset registers in IDT standard mode is included in the reference design file on the IDT web site.

NORMAL OPERATION

The normal operation of the TeraSync FIFO includes a standard first-in-first-out data sequence with clocked read and write controls. There are two possible timing modes of operation with these devices: IDT Standard mode and First-Word-Fall-Through (FWFT) mode. The TeraSync data sheet gives a full explanation of these two timing modes.

IDT Standard Mode

IDT Standard mode is selected during master reset by setting the FWFT/SI pin High. Once the timing mode is selected, read and write operations can begin. In this mode, the flag boundaries used are $\overline{EF}$ and $\overline{FF}$. The sample Verilog code (1) for master reset and default programming, included in the reference design file on the IDT web site, demonstrates how to set the device in IDT standard mode.

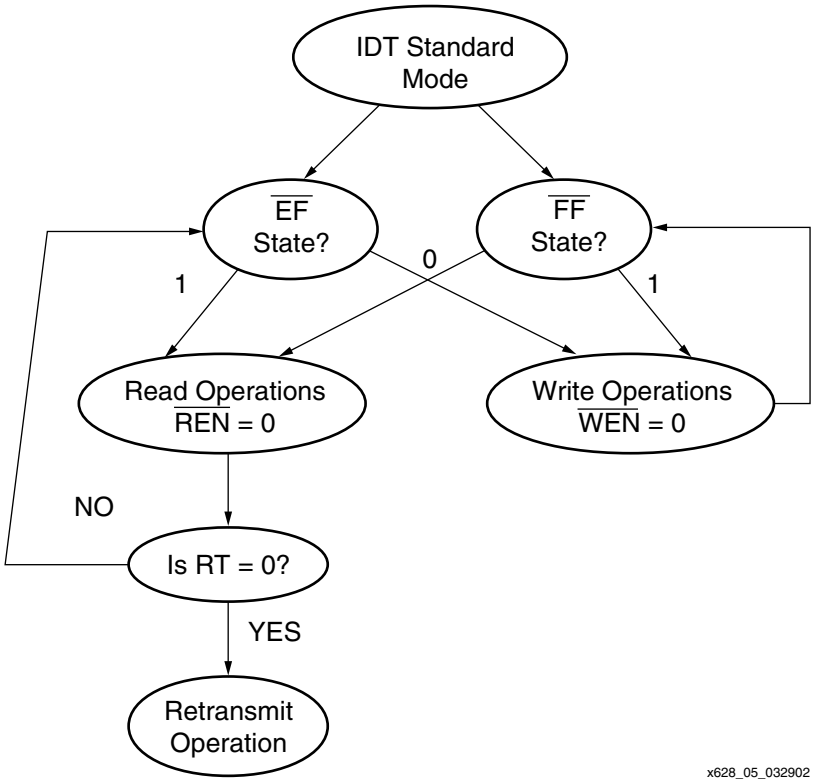

Figure 5: **Flowchart for Read and Write Operations in IDT Standard Mode**

Read Operation in IDT Standard Mode

Data stored in the FIFO can be read out from the output bus Q[35:0]. The signals associated with read operations are: $\overline{REN}$, RCLK, $\overline{RCS}$, and $\overline{EF}$. To initiate a read operation, set $\overline{REN}$ to Low. Data is loaded from the RAM array into the output register on the rising edge of every RCLK as long as the $\overline{EF}$ signal is not Low. In IDT Standard mode, every word read must be requested using $\overline{REN}$ provided as long as the $\overline{RCS}$ signal is Low. $\overline{RCS}$ provides synchronous enable control of the Read port. If it is inactive, the output bus will be 3-stated. The sample Verilog code (4) for single Read operation in IDT standard mode is included in the reference design file on the IDT web site. Figure 6 is a block diagram of the associated signals for implementing the read operation of the TeraSync FIFO.

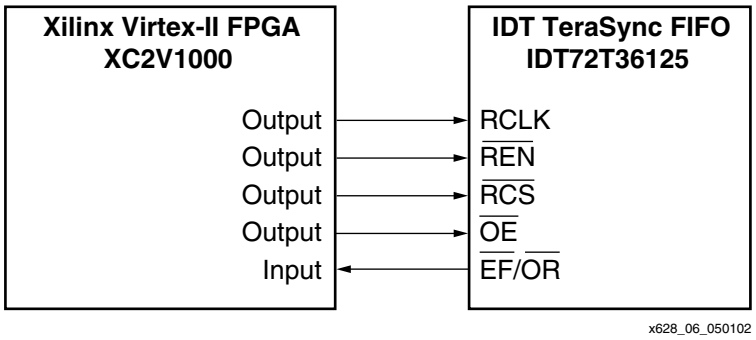

Figure 6: **Signals Relevant for Read Operations in IDT Standard Mode**

If planning on using only one signal for controlling the output enables, then it is recommended that the output enable signal OE be tied to GND and designate RCS as the enable control signal.

Write Operation in IDT Standard Mode

Data is written into the FIFO from the data input bus D[35:0]. The signals associated with the write operation are: $\overline{WEN}$, WCLK, $\overline{WCS}$, and $\overline{FF}$. To initiate a Write operation, set $\overline{WEN}$ to Low to load data into the RAM array from the input data bus on the rising edge of every WCLK as long as $\overline{FF}$ is not Low. $\overline{WCS}$ provides synchronous control of the Write port. If it is inactive, then the input port will be disabled and no data will be written into the FIFO. The sample Verilog code (5) for single Write operation in IDT standard mode is included in the reference design file on the IDT web site. Figure 7 is a block diagram of the associated signals for implementing the Write operation of the TeraSync FIFO.

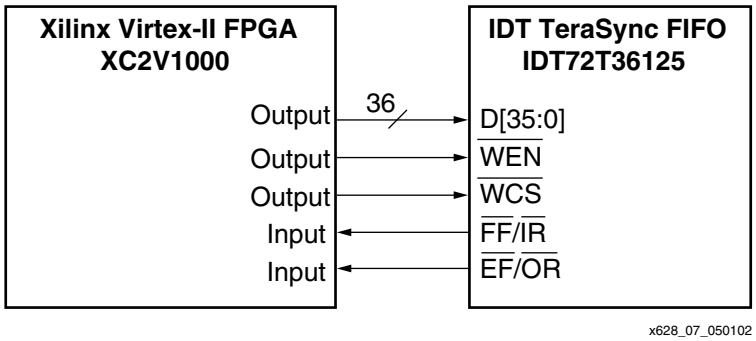

Figure 7: **Signals Relevant for Write Operations**

Sample code (4) and (5) are functions for executing a single Read and Write operation. It is up to the designer to determine the amount of Reads and Writes into the device. The sample Verilog code (6) for burst Write and Read operation is included in the reference design file on the IDT web site. First the operation Writes to Full and then Reads to empty for a certain number of iterations.

FWFT Mode

FWFT mode is selected during master reset by setting the FWFT/SI pin Low. Once the timing mode has been selected, read and write operations can begin. In this mode, the flag boundaries use are $\overline{IR}$ and $\overline{OR}$. To set the device in FWFT mode, follow modify the default *prog* case statement in the Verilog Sample Code (1) to fwft_si ≤ 1. Figure 8 is a flowchart for Read and Write Operations in the FWFT mode of the TeraSync FIFO.

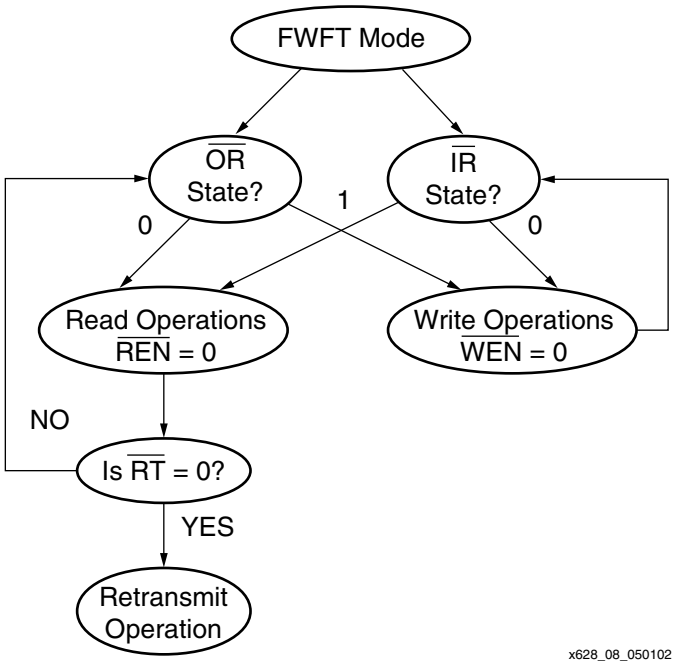

Figure 8: **Flowchart for Read and Write Operations in the FWFT Mode**

Read Operation in FWFT Mode

Data stored in the FIFO can be read out from the output bus Q[35:0]. The signals associated with read operations are: REN, RCLK, RCS, and OR. To initiate a read operation, set REN to Low, and data will be loaded from the RAM array into the output register on the rising edge of every RCLK provided that OR is Low. In FWFT mode, the first word written to an empty FIFO automatically goes to the output bus on the third rising edge of RCLK after the first write. REN and RCS are not required to go Low for the first word to fall through to the output register. Every word after the first word will require that REN and RCS go Low in order to be read out. RCS provides synchronous enable control of the read port. If it is inactive, the output bus will be 3-stated. Figure 8 shows the block diagram for the Read operation. The Verilog code (7) for Read operations in FWFT mode is very similar to IDT Standard mode. The only difference is the status flag relating to the read port is OR instead of EF. Sample Verilog code (7) for single Read operation in FWFT mode is included in the reference design file on the IDT web site.

If planning on using only one signal for controlling the output enables, then it is recommended that the output enable signal OE be tied to GND and designate RCS as the enable control signal.

Write Operation in FWFT Mode

Data is written into the FIFO from the data input bus D[35:0]. The signals associated with the write operation are: WEN, WCLK, WCS, and IR. To initiate a write operation, set WEN to Low, and data will be loaded into the RAM array from the input data bus on the rising edge of every WCLK provided that IR is Low. WCS provides synchronous control of the write port. If it is inactive, then the input port will be disabled and no data will be written into the FIFO. Figure 8 shows the block diagram for the Write operation. The Verilog code (8) for Write operations in FWFT mode is very similar to IDT Standard mode. The only difference being the status flag relating to the write port is IR instead of FF. The a sample Verilog code (8) for Write operations in FWFT mode is included in the reference design file on the IDT web site.

Special Features

Retransmit

One of the special features of the TeraSync FIFO is the mark and retransmit operation. This allows data in the FIFO to be read repeatedly starting at a user-selected position. To mark a location in memory where data will begin retransmitting, enable MARK to High at a rising edge of RCLK. Once a location is marked, a retransmit operation can take place. To retransmit data, set the retransmit signal ($\overline{RT}$) Low for a rising edge of RCLK to set the device in retransmit mode. At that point the Empty Flag will go Low, once the Empty Flag returns to High retransmit setup is complete.

The read enable must be disabled (set High) during retransmit setup. Once setup is complete, enabling read enable (set Low) and at every rising edge of RCLK data will be retransmitted, starting from the marked location in the FIFO RAM to the location of the read pointer prior to retransmit. Figure 9 diagrams the mark and retransmit feature.

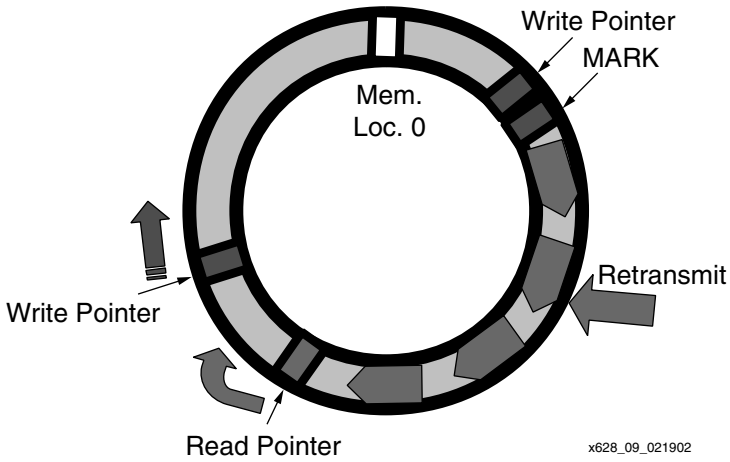

Figure 9: **MARK and Retransmit Operation**

The write pointer cannot be incriminated past the MARK point. There must be at least 32 bytes between the Write pointer and MARK location when retransmit is requested. Figure 10 is a block diagram for implementing this feature. The a sample Verilog code (9) for MARK and retransmit is included in the reference design file on the IDT web site.

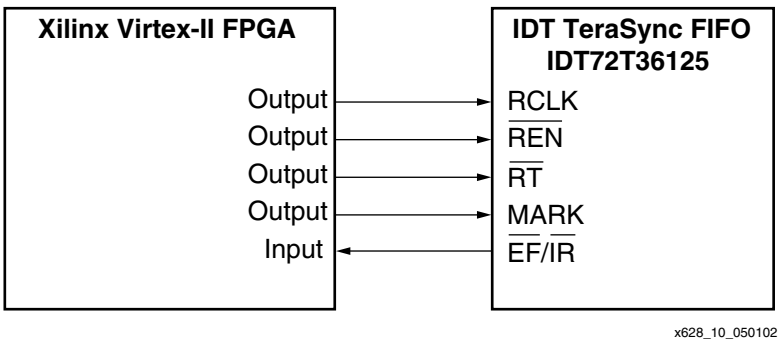

Figure 10: **Signals Relevant for MARK and Retransmit**

Reference Design

There are a wide variety of applications to utilize a Virtex-II FPGA with a TeraSync FIFO. The reference design for this application note includes an Optical Fiber Test System used in SONET. This design tests and verifies data for a fiber optic cable line. Figure 11 is a block diagram of this application.

A data pattern is generated by the Flash ROM where it is sent to the TeraSync FIFO in the transmit port. The 2.5V TeraSync FIFO core is ideal since this application strictly uses a single voltage source. Bus-matching is utilized since the TI SerDes has only 16 inputs. The Virtex-II FPGA controls the Read and Write signals to the FIFO. The transmit FIFO also utilizes the MARK and Retransmit feature. During a trigger and repeat mode, the same pattern will be transmitted from the FIFO and repeated until the end of the packet is designated by the two extra control bits. Thus, the two extra bits in the transmit port are used as packet markers for retransmit purposes. The 16-bit data entering the SerDes is serialized and sent out at a 2.4 Gb/s serial data rate. The data is then connected to the receive side of the transceiver where it is deserialized and sent back into the FIFO. The receive FIFO uses bus-matching to output 36-bit data required by the system bus. The system bus then verifies the data.

The reference design in Verilog code is available on the IDT web site at:

http://www.idt.com/docs/TeraSync_Verilog_Example.txt

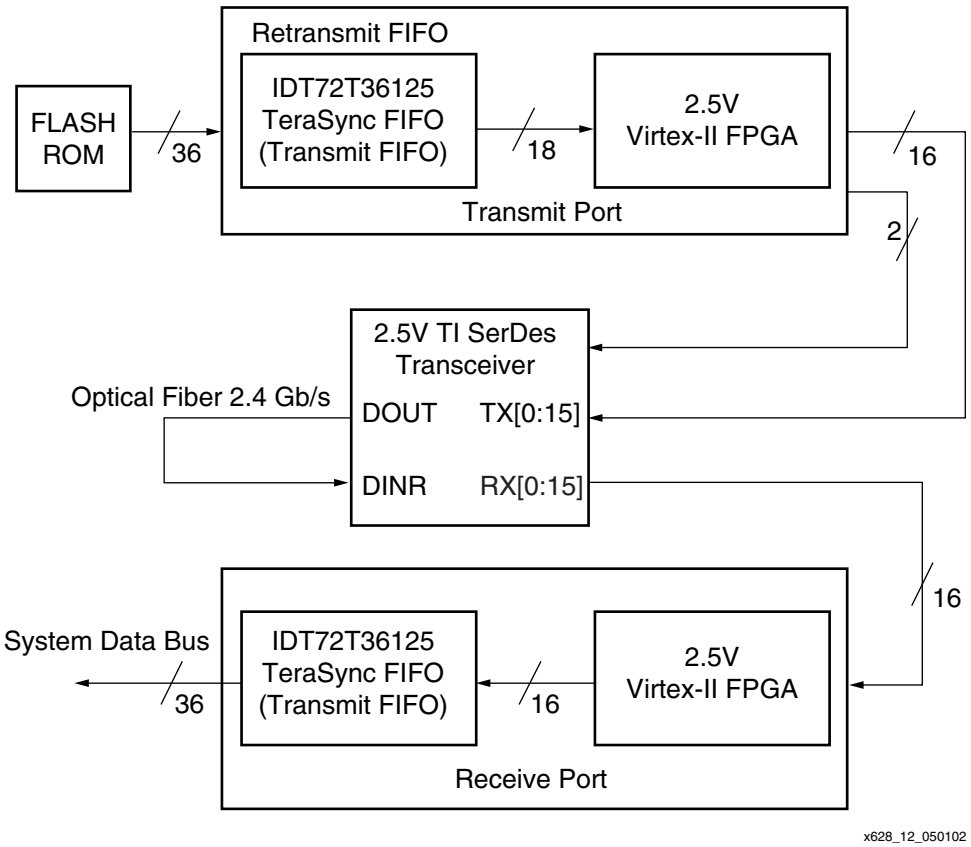

Figure 11: **Optical Fiber Test System Block Diagram**

Conclusion

The Virtex-II FPGA is a great resource for initializing and implementing features in IDT's TeraSync FIFO. The Virtex-II FPGA can initiate many of the standard operations and special features in the TeraSync FIFO through Verilog programming. The flexibility, advanced features, and ease of use make the Virtex-II FPGA an ideal candidate to interface with the TeraSync FIFO.

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
12/04/02	1.0	Initial Xilinx release.