

Features

- 36 macrocells with 800 usable gates
- Available in small footprint packages
 - 44-pin PLCC (34 user I/O pins)
 - 44-pin VQFP (34 user I/O pins)
 - 48-pin CSP (36 user I/O pins)
- Optimized for high-performance 2.5V systems
 - Low power operation
 - Multi-voltage operation
- Advanced system features
 - In-system programmable
 - Superior pin-locking and routability with Fast CONNECT™ II switch matrix
 - Extra wide 54-input Function Blocks
 - Up to 90 product-terms per macrocell with individual product-term allocation
 - Local clock inversion with three global and one product-term clocks
 - Individual output enable per output pin
 - Input hysteresis on all user and boundary-scan pin inputs
 - Bus-hold circuitry on all user pin inputs
 - Full IEEE Standard 1149.1 boundary-scan (JTAG)
- Fast concurrent programming
- Slew rate control on individual outputs
- Enhanced data security features
- Excellent quality and reliability
 - 20 year data retention
 - ESD protection exceeding 2,000V
- Pin-compatible with 3.3V-core XC9536XL device in the 44-pin PLCC, 44-pin VQFP, and 48-pin CSP packages

Description

The XC9536XV is a 2.5V CPLD targeted for high-performance, low-voltage applications in leading-edge communications and computing systems. It is comprised of two 54V18 Function Blocks, providing 800 usable gates with propagation delays of 5 ns. See [Figure 2](#) for architecture overview.

Power Estimation

Power dissipation in CPLDs can vary substantially depending on the system frequency, design application and output loading. To help reduce power dissipation, each macrocell in a XC9500XV device may be configured for low-power mode (from the default high-performance mode). In addition, unused product-terms and macrocells are automatically deactivated by the software to further conserve power.

For a general estimate of I_{CC} , the following equation may be used:

$$P_{TOTAL} = P_{INT} + P_{IO} = I_{CCINT} \times V_{CCINT} + P_{IO}$$

Separating internal and I/O power here is convenient because XC9500XV CPLDs also separate the corresponding power pins. P_{IO} is a strong function of the load capacitance driven, so it is handled by $I = CVf$. I_{CCINT} is another situation that reflects the actual design considered and the internal switching speeds. An estimation expression for I_{CCINT} (taken from simulation) is:

$$I_{CCINT}(mA) = MC_{HS}(0.122 \times PT_{HS} + 0.238) + MC_{LP}(0.042 \times PT_{LP} + 0.171) + 0.04(MC_{HS} + MC_{LP}) \times f_{MAX} \times MC_{TOG}$$

where:

MC_{HS} = # macrocells used in high speed mode

MC_{LP} = #macrocells used in low power mode

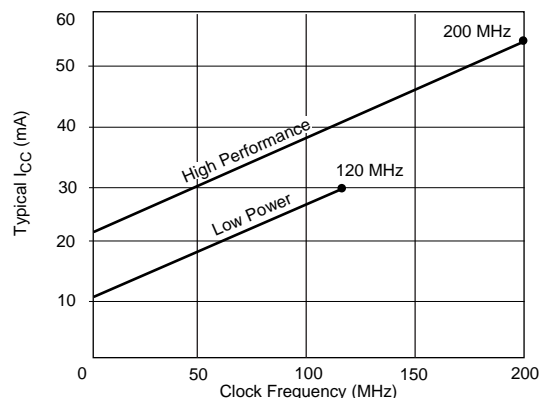
PT_{HS} = average p-terms used per high speed macrocell

PT_{LP} = average p-terms used over low power macrocell

f_{MAX} = max clocking frequency in the device

MC_{TOG} = % macrocells toggling on each clock (12% is frequently a good estimate)

This calculation was derived from laboratory measurements of an XC9500XV part filled with 16-bit counters and allowing a single output (the LSB) to be enabled. The actual I_{CC} value varies with the design application and should be verified during normal system operation. [Figure 1](#) shows the above estimation in a graphical form. For a more detailed discussion of power consumption in this device, see Xilinx application note [XAPP361, "Planning for High Speed XC9500XV Designs."](#)



DS053_01_121501

Figure 1: Typical I_{CC} vs. Frequency for XC9536XV

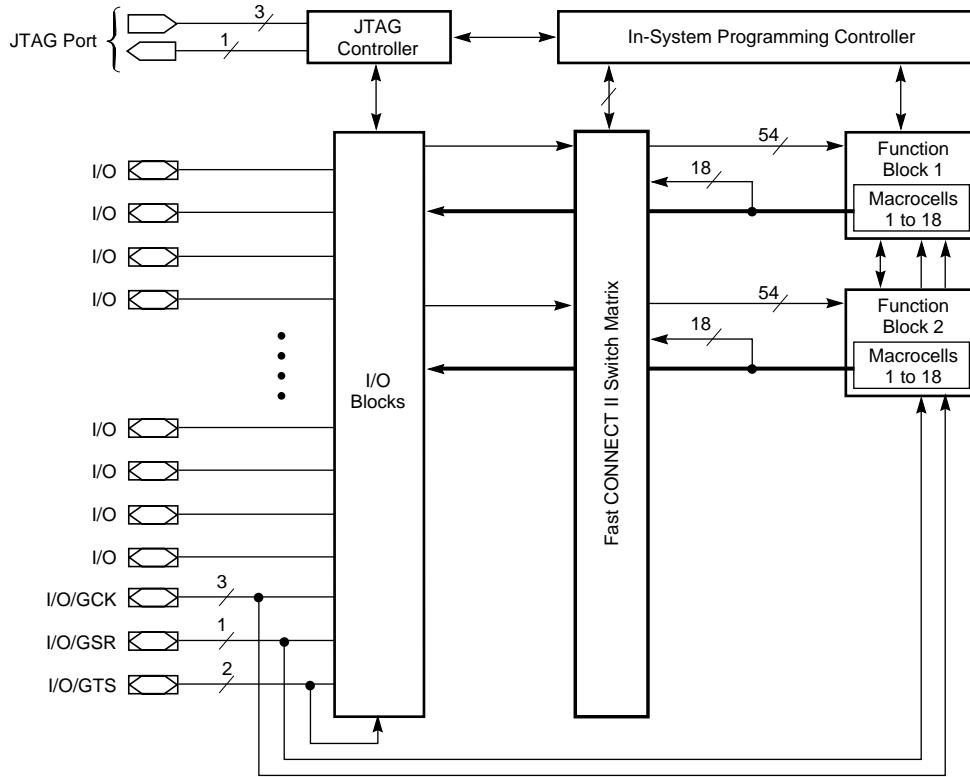


Figure 2: XC9536XV Architecture

Function block outputs (indicated by the bold line) drive the I/O Blocks directly.

Absolute Maximum Ratings

| Symbol | Description | Value | Units |
|------------|---|-------------|-------|
| V_{CC} | Supply voltage relative to GND | -0.5 to 2.7 | V |
| V_{CCIO} | Supply voltage for output drivers | -0.5 to 3.6 | V |
| V_{IN} | Input voltage relative to GND ⁽¹⁾ | -0.5 to 3.6 | V |
| V_{TS} | Voltage applied to 3-state output ⁽¹⁾ | -0.5 to 3.6 | V |
| T_{STG} | Storage temperature (ambient) | -65 to +150 | °C |
| T_{SOL} | Maximum soldering temperature (10s @ 1/16 in. = 1.5 mm) | +260 | °C |
| T_J | Junction temperature | +150 | °C |

Notes:

- Maximum DC undershoot below GND must be limited to either 0.5V or 10 mA, whichever is easier to achieve. During transitions, the device pins may undershoot to -2.0V or overshoot to +3.6V, provided this over- or undershoot lasts less than 10 ns and with the forcing current being limited to 200 mA.
- Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.

Recommended Operation Conditions

| Symbol | Parameter | | Min | Max | Units |
|-------------|--|---|------|------------|-------|
| V_{CCINT} | Supply voltage for internal logic and input buffers | Commercial $T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$ | 2.37 | 2.62 | V |
| | | Industrial $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$ | 2.37 | 2.62 | |
| V_{CCIO} | Supply voltage for output drivers for 3.3V operation | | 3.0 | 3.6 | V |
| | Supply voltage for output drivers for 2.5V operation | | 2.37 | 2.62 | V |
| | Supply voltage for output drivers for 1.8V operation | | 1.71 | 1.89 | V |
| V_{IL} | Low-level input voltage | | 0 | 0.8 | V |
| V_{IH} | High-level input voltage | | 1.7 | 3.6 | V |
| V_O | Output voltage | | 0 | V_{CCIO} | V |

Quality and Reliability Characteristics

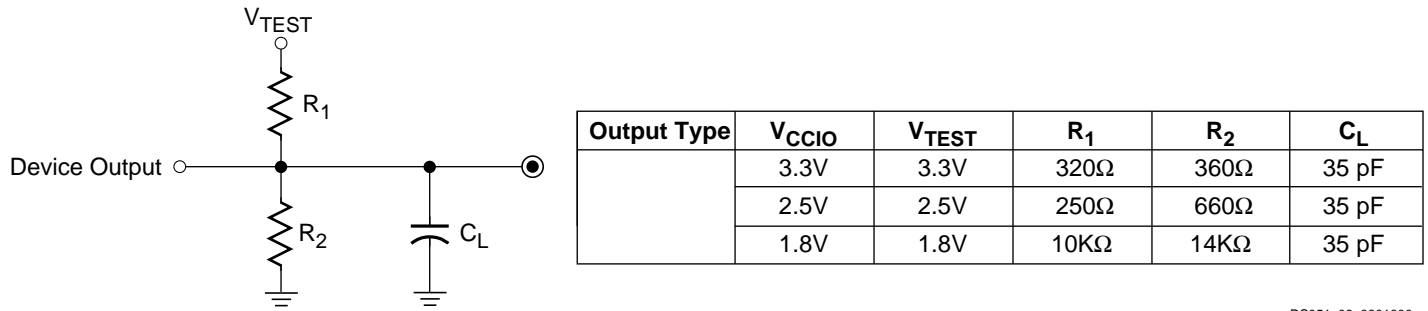
| Symbol | Parameter | Min | Max | Units |
|-----------|----------------------------------|-------|-----|--------|
| T_{DR} | Data Retention | 20 | - | Years |
| N_{PE} | Program/Erase Cycles (Endurance) | 1,000 | - | Cycles |
| V_{ESD} | Electrostatic Discharge (ESD) | 2,000 | - | Volts |

DC Characteristics (Over Recommended Operating Conditions)

| Symbol | Parameter | Test Conditions | Min | Max | Units |
|----------|--|---|----------------|-----------|---------|
| V_{OH} | Output high voltage for 3.3V outputs | $I_{OH} = -4.0$ mA | 2.4 | - | V |
| | Output high voltage for 2.5V outputs | $I_{OH} = -1.0$ mA | 2.0 | - | V |
| | Output high voltage for 1.8V outputs | $I_{OH} = -100$ μ A | 90% V_{CCIO} | - | V |
| V_{OL} | Output low voltage for 3.3V outputs | $I_{OL} = 8.0$ mA | - | 0.4 | V |
| | Output low voltage for 2.5V outputs | $I_{OL} = 1.0$ mA | - | 0.4 | V |
| | Output low voltage for 1.8V outputs | $I_{OL} = 100$ μ A | - | 0.4 | V |
| I_{IL} | Input leakage current | $V_{CC} = 2.62$ V $V_{CCIO} = 3.6$ V $V_{IN} = GND$ or 3.6V | - | ± 10 | μ A |
| I_{IH} | Input high-Z leakage current | $V_{CC} = 2.62$ V $V_{CCIO} = 3.6$ V $V_{IN} = GND$ or 3.6V | - | ± 10 | μ A |
| | | $V_{CC} \text{ min} < V_{IN} < 3.6$ V | - | ± 150 | μ A |
| C_{IN} | I/O capacitance | $V_{IN} = GND$ $f = 1.0$ MHz | - | 10 | pF |
| I_{CC} | Operating Supply Current (low power mode, active) | $V_I = GND$, No load $f = 1.0$ MHz | 7 | | mA |

AC Characteristics

| Symbol | Parameter | XC9536XV-5 | | XC9536XV-7 | | Units |
|--------------|--|------------|-------|------------|-------|-------|
| | | Min | Max | Min | Max | |
| T_{PD} | I/O to output valid | - | 5.0 | - | 7.5 | ns |
| T_{SU} | I/O setup time before GCK | 3.5 | - | 4.8 | - | ns |
| T_H | I/O hold time after GCK | 0 | - | 0 | - | ns |
| T_{CO} | GCK to output valid | - | 3.5 | - | 4.5 | ns |
| f_{SYSTEM} | Multiple FB internal operating frequency | - | 222.2 | - | 125.0 | MHz |
| T_{PSU} | I/O setup time before p-term clock input | 1.0 | - | 1.6 | - | ns |
| T_{PH} | I/O hold time after p-term clock input | 2.5 | - | 3.2 | - | ns |
| T_{PCO} | P-term clock output valid | - | 6.0 | - | 7.7 | ns |
| T_{OE} | GTS to output valid | - | 4.0 | - | 5.0 | ns |
| T_{OD} | GTS to output disable | - | 4.0 | - | 5.0 | ns |
| T_{POE} | Product term OE to output enabled | - | 7.0 | - | 9.5 | ns |
| T_{POD} | Product term OE to output disabled | - | 7.0 | - | 9.5 | ns |
| T_{AO} | GSR to output valid | - | 10.0 | - | 12.0 | ns |
| T_{PAO} | P-term S/R to output valid | - | 10.7 | - | 12.6 | ns |
| T_{WLH} | GCK pulse width (High or Low) | 2.2 | - | 4.0 | - | ns |
| T_{PLH} | P-term clock pulse width (High or Low) | 5.0 | - | 6.5 | - | ns |



DS051_03_0601000

Figure 3: AC Load Circuit

Internal Timing Parameters

| Symbol | Parameter | XC9536XV-5 | | XC9536XV-7 | | Units |
|---|---|------------|-----|------------|-----|-------|
| | | Min | Max | Min | Max | |
| Buffer Delays | | | | | | |
| T _{IN} | Input buffer delay | - | 2.0 | - | 2.3 | ns |
| T _{GCK} | GCK buffer delay | - | 1.2 | - | 1.5 | ns |
| T _{GSR} | GSR buffer delay | - | 2.0 | - | 3.1 | ns |
| T _{GTS} | GTS buffer delay | - | 4.0 | - | 5.0 | ns |
| T _{OUT} | Output buffer delay | - | 2.1 | - | 2.5 | ns |
| T _{EN} | Output buffer enable/disable delay | - | 0 | - | 0 | ns |
| Product Term Control Delays | | | | | | |
| T _{PTCK} | Product term clock delay | - | 1.7 | - | 2.4 | ns |
| T _{PTSR} | Product term set/reset delay | - | 0.7 | - | 1.4 | ns |
| T _{PTTS} | Product term 3-state delay | - | 5.0 | - | 7.2 | ns |
| Internal Register and Combinatorial Delays | | | | | | |
| T _{PDI} | Combinatorial logic propagation delay | - | 0.2 | - | 1.3 | ns |
| T _{SUI} | Register setup time | 2.0 | - | 2.6 | - | ns |
| T _{HI} | Register hold time | 1.5 | - | 2.2 | - | ns |
| T _{ECSU} | Register clock enable setup time | 2.0 | - | 2.6 | - | ns |
| T _{ECHO} | Register clock enable hold time | 1.5 | - | 2.2 | - | ns |
| T _{COI} | Register clock to output valid time | - | 0.2 | - | 0.5 | ns |
| T _{AOI} | Register async. S/R to output delay | - | 5.9 | - | 6.4 | ns |
| T _{RAI} | Register async. S/R recover before clock | 5.0 | - | 7.5 | - | ns |
| T _{LOGI} | Internal logic delay | - | 0.7 | - | 1.4 | ns |
| T _{LOGILP} | Internal low power logic delay | - | 5.7 | - | 6.4 | ns |
| Feedback Delays | | | | | | |
| T _F | Fast CONNECT II feedback delay | - | 1.6 | - | 3.5 | ns |
| Time Adders | | | | | | |
| T _{PTA} | Incremental product term allocator delay | - | 0.7 | - | 0.8 | ns |
| T _{PTA2} | Adjacent macrocell p-term allocator delay | - | 0.3 | - | 0.3 | ns |
| T _{SLEW} | Slew-rate limited delay | - | 3.0 | - | 4.0 | ns |

XC9536XV I/O Pins

| Function Block | Macrocell | PC44 | VQ44 | CS48 | BScan Order | Function Block | Macrocell | PC44 | VQ44 | CS48 | BScan Order |
|----------------|-----------|------------------|-------------------|-------------------|-------------|----------------|-----------|-------------------|-------------------|-------------------|-------------|
| 1 | 1 | 2 | 40 | D6 | 105 | 2 | 1 | 1 | 39 | D7 | 51 |
| 1 | 2 | 3 | 41 | C7 | 102 | 2 | 2 | 44 | 38 | E5 | 48 |
| 1 | 3 | 5 ⁽¹⁾ | 43 ⁽¹⁾ | B7 ⁽¹⁾ | 99 | 2 | 3 | 42 ⁽¹⁾ | 36 ⁽¹⁾ | E6 ⁽¹⁾ | 45 |
| 1 | 4 | 4 | 42 | C6 | 96 | 2 | 4 | 43 | 37 | E7 | 42 |
| 1 | 5 | 6 ⁽¹⁾ | 44 ⁽¹⁾ | B6 ⁽¹⁾ | 93 | 2 | 5 | 40 ⁽¹⁾ | 34 ⁽¹⁾ | F6 ⁽¹⁾ | 39 |
| 1 | 6 | 8 | 2 | A6 | 90 | 2 | 6 | 39 ⁽¹⁾ | 33 ⁽¹⁾ | G7 ⁽¹⁾ | 36 |
| 1 | 7 | 7 ⁽¹⁾ | 1 ⁽¹⁾ | A7 ⁽¹⁾ | 87 | 2 | 7 | 38 | 32 | G6 | 33 |
| 1 | 8 | 9 | 3 | C5 | 84 | 2 | 8 | 37 | 31 | F5 | 30 |
| 1 | 9 | 11 | 5 | B5 | 81 | 2 | 9 | 36 | 30 | G5 | 27 |
| 1 | 10 | 12 | 6 | A4 | 78 | 2 | 10 | 35 | 29 | F4 | 24 |
| 1 | 11 | 13 | 7 | B4 | 75 | 2 | 11 | 34 | 28 | G4 | 21 |
| 1 | 12 | 14 | 8 | A3 | 72 | 2 | 12 | 33 | 27 | E3 | 18 |
| 1 | 13 | 18 | 12 | B2 | 69 | 2 | 13 | 29 | 23 | F2 | 15 |
| 1 | 14 | 19 | 13 | B1 | 66 | 2 | 14 | 28 | 22 | G1 | 12 |
| 1 | 15 | 20 | 14 | C2 | 63 | 2 | 15 | 27 | 21 | F1 | 9 |
| 1 | 16 | 22 | 16 | C3 | 60 | 2 | 16 | 26 | 20 | E2 | 6 |
| 1 | 17 | 24 | 18 | D2 | 57 | 2 | 17 | 25 | 19 | E1 | 3 |
| 1 | 18 | - | - | D3 | 54 | 2 | 18 | - | - | E4 | 0 |

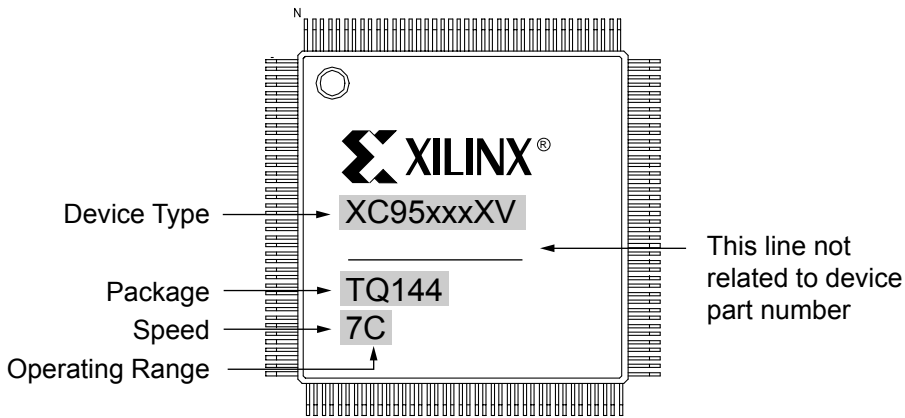
Notes:

1. Global control pin.

XC9536XV Global, JTAG and Power Pins

| Pin Type | PC44 | VQ44 | CS48 |
|-----------------------------------|------------|-----------|------------|
| I/O/GCK1 | 5 | 43 | B7 |
| I/O/GCK2 | 6 | 44 | B6 |
| I/O/GCK3 | 7 | 1 | A7 |
| I/O/GTS1 | 42 | 36 | E6 |
| I/O/GTS2 | 40 | 34 | F6 |
| I/O/GSR | 39 | 33 | G7 |
| TCK | 17 | 11 | A1 |
| TDI | 15 | 9 | B3 |
| TDO | 30 | 24 | G2 |
| TMS | 16 | 10 | A2 |
| V _{CCINT} 2.5V | 21, 41 | 15, 35 | C1, F7 |
| V _{CCIO} 1.8vV/2.5V/3.3V | 32 | 26 | G3 |
| GND | 10, 23, 31 | 4, 17, 25 | A5, D1, F3 |
| No Connects | - | - | C4, D4 |

Device Part Marking and Ordering Combination Information



Sample package with part marking.

| Device Ordering and Part Marking Number | Speed (pin-to-pin delay) | Pkg. Symbol | No. of Pins | Package Type | Operating Range ⁽¹⁾ |
|---|--------------------------|-------------|-------------|----------------------------------|--------------------------------|
| XC9536XV-5PC44C | 5 ns | PC44 | 44-pin | Plastic Lead Chip Carrier (PLCC) | C |
| XC9536XV-5VQ44C | 5 ns | VQ44 | 44-pin | Quad Flat Pack (VQFP) | C |
| XC9536XV-5CS48C | 5 ns | CS48 | 48-ball | Chip Scale Package (CSP) | C |
| XC9536XV-7PC44C | 7.5 ns | PC44 | 44-pin | Plastic Lead Chip Carrier (PLCC) | C |
| XC9536XV-7VQ44C | 7.5 ns | VQ44 | 44-pin | Quad Flat Pack (VQFP) | C |
| XC9536XV-7CS48C | 7.5 ns | CS48 | 48-ball | Chip Scale Package (CSP) | C |
| XC9536XV-7PC44I | 7.5 ns | PC44 | 44-pin | Plastic Lead Chip Carrier (PLCC) | I |
| XC9536XV-7VQ44I | 7.5 ns | VQ44 | 44-pin | Quad Flat Pack (VQFP) | I |
| XC9536XV-7CS48I | 7.5 ns | CS48 | 48-ball | Chip Scale Package (CSP) | I |

Notes:

1. C = Commercial: T_A = 0° to +70°C; I = Industrial: T_A = -40° to +85°C.

Revision History

| Date | Revision No. | Description |
|----------|--------------|--|
| 02/01/00 | 1.1 | Initial Xilinx release. Advance information specification. |
| 01/29/01 | 2.0 | Added -3 performance specification and VQ44 package. Deleted VQ64 package. Updated I_{CC} vs. Frequency Figure 1 . |
| 05/15/01 | 2.1 | Updated I_{CC} formula, Recommended Operation Conditions, -3, -4, and -5 AC Characteristics and Internal Timing Parameters |
| 08/27/01 | 2.2 | Changed V_{CCIO} 3.3V from 3.13 to 3.0 (min), 3.46 to 3.60 (max); DC characteristics: I_{IL} - added "low" current, I_{IH} - changed to "Input leakage high current"; Internal Timing: -3 T_{CGK} from 0.3 to 0.8; -5 T_{AOI} from 6.5 to 5.9. |
| 05/31/02 | 2.3 | Updated I_{CC} equation on page 1. Removed -3 device. Changed to Preliminary. Added C4 and D4 as NCs in the CS48 package pinouts. Added second test condition and max measurement to I_{IH} DC Characteristics. Added Part Marking Information to Ordering Information. Removed -4 device. |