Spartan-IIE 1.8V FPGA Family: Introduction and Ordering Information

DS077-1 (v2.0) November 18, 2002

Product Specification

Introduction

The Spartan™-IIE 1.8V Field-Programmable Gate Array family gives users high performance, abundant logic resources, and a rich feature set, all at an exceptionally low price. The seven-member family offers densities ranging from 50,000 to 600,000 system gates, as shown in Table 1. System performance is supported beyond 200 MHz.

Spartan-IIE devices deliver more gates, I/Os, and features per dollar than other FPGAs by combining advanced process technology with a streamlined architecture based on the proven Virtex™-E platform. Features include block RAM (to 288K bits), distributed RAM (to 221,184 bits), 19 selectable I/O standards, and four DLLs (Delay-Locked Loops). Fast, predictable interconnect means that successive design iterations continue to meet timing requirements.

The Spartan-IIE family is a superior alternative to mask-programmed ASICs. The FPGA avoids the initial cost, lengthy development cycles, and inherent risk of conventional ASICs. Also, FPGA programmability permits design upgrades in the field with no hardware replacement necessary (impossible with ASICs).

Features

- Second generation ASIC replacement technology
  - Densities as high as 15,552 logic cells with up to 600,000 system gates
  - Streamlined features based on Virtex-E architecture
  - Unlimited in-system reprogrammability
  - Very low cost
- System level features
  - SelectRAM+™ hierarchical memory:
    - 16 bits/LUT distributed RAM
    - Configurable 4K-bit true dual-port block RAM
    - Fast interfaces to external RAM
  - Fully 3.3V PCI compliant to 64 bits at 66 MHz and CardBus compliant
  - Low-power segmented routing architecture
  - Dedicated carry logic for high-speed arithmetic
  - Efficient multiplier support
  - Cascade chain for wide-input functions
  - Abundant registers/latches with enable, set, reset
  - Four dedicated DLLs for advanced clock control
    - Eliminate clock distribution delay
    - Multiply, divide, or phase shift
  - Four primary low-skew global clock distribution nets
  - IEEE 1149.1 compatible boundary scan logic
- Versatile I/O and packaging
  - Low cost packages available in all densities
  - Family footprint compatibility in common packages
  - 19 high-performance interface standards
    - LVTTL, LVCMOS, HSTL, SSTL, AGP, CTT, GTL
    - LVDS and LVPECL differential I/O
  - Up to 205 differential I/O pairs that can be input, output, or bidirectional
- Fully supported by powerful Xilinx ISE development system
  - Fully automatic mapping, placement, and routing
  - Integrated with design entry and verification tools
  - Extensive IP library including DSP functions and soft processors

Table 1: **Spartan-IIE FPGA Family Members**

Device	Logic Cells	Typical System Gate Range (Logic and RAM)	CLB Array (R x C)	Total CLBs	Maximum Available User I/O(1)	Maximum Differential I/O Pairs	Distributed RAM Bits	Block RAM Bits
XC2S50E	1,728	23,000 - 50,000	16 x 24	384	182	83	24,576	32K
XC2S100E	2,700	37,000 - 100,000	20 x 30	600	202	86	38,400	40K
XC2S150E	3,888	52,000 - 150,000	24 x 36	864	265	114	55,296	48K
XC2S200E	5,292	71,000 - 200,000	28 x 42	1,176	289	120	75,264	56K
XC2S300E	6,912	93,000 - 300,000	32 x 48	1,536	329	120	98,304	64K
XC2S400E	10,800	145,000 - 400,000	40 x 60	2,400	410	172	153,600	160K
XC2S600E	15,552	210,000 - 600,000	48 x 72	3,456	514	205	221,184	288K

Notes:

1. User I/O counts include the four global clock/user input pins. See details in Table 3, page 3

General Overview

The Spartan-IIE family of FPGAs have a regular, flexible, programmable architecture of Configurable Logic Blocks (CLBs), surrounded by a perimeter of programmable Input/Output Blocks (IOBs). There are four Delay-Locked Loops (DLLs), one at each corner of the die. Two columns of block RAM lie on opposite sides of the die, between the CLBs and the IOB columns. The XC2S400E has four columns and the XC2S600E has six columns of block RAM. These functional elements are interconnected by a powerful hierarchy of versatile routing channels (see Figure 1).

Spartan-IIE FPGAs are customized by loading configuration data into internal static memory cells. Unlimited reprogramming cycles are possible with this approach. Stored values in these cells determine logic functions and interconnections implemented in the FPGA. Configuration data can be read from an external serial PROM (master serial mode), or written into the FPGA in slave serial, slave parallel, or Boundary Scan modes. Low-cost configuration PROMs include the XC17S00A and XC17V00 serial PROMs and the in-system programmable XC18V00 PROMs.

Spartan-IIE FPGAs are typically used in high-volume applications where the versatility of a fast programmable solution adds benefits. Spartan-IIE FPGAs are ideal for shortening product development cycles while offering a cost-effective solution for high volume production.

Spartan-IIE FPGAs achieve high-performance, low-cost operation through advanced architecture and semiconductor technology. Spartan-IIE devices provide system clock rates beyond 200 MHz. Spartan-IIE FPGAs offer the most cost-effective solution while maintaining leading edge performance. In addition to the conventional benefits of high-volume programmable logic solutions, Spartan-IIE FPGAs also offer on-chip synchronous single-port and dual-port RAM (block and distributed form), DLL clock drivers, programmable set and reset on all flip-flops, fast carry logic, and many other features.

Spartan-IIE Family Compared to Spartan-II Family

- Higher density and more I/O
- Higher performance
- Unique pinouts in cost-effective packages
- Differential signaling
  - LVDS, Bus LVDS, LVPECL
- V_{CCINT} = 1.8V
  - Lower power
  - 5V tolerance with external resistor
  - 3V tolerance directly
- PCI, LVTTL, and LVCMOS2 input buffers powered by V_{CCO} instead of V_{CCINT}
- Unique larger bitstream

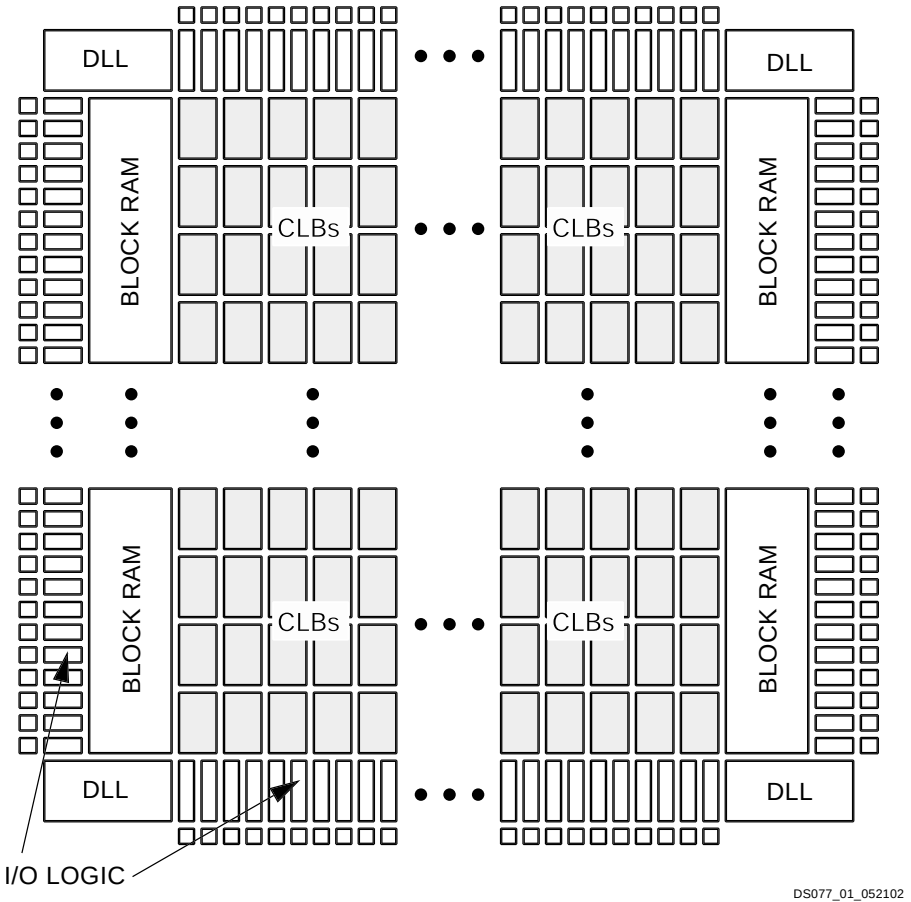


Figure 1: **Basic Spartan-IIE Family FPGA Block Diagram**

Spartan-IIE Product Availability

Table 2 shows the package and speed grades available for Spartan-IIE family devices. Table 3 shows the maximum user I/Os available on the device and the number of user I/Os available for each device/package combination.

Table 2: **Spartan-IIE Package and Speed Grade Availability**

Device	Pins	144	208	256	456	676
	Type	Plastic TQFP	Plastic PQFP	Fine Pitch BGA	Fine Pitch BGA	Fine Pitch BGA
	Code	TQ144	PQ208	FT256	FG456	FG676
XC2S50E	-6	C, I	C, I	C, I	-	-
	-7	C	C	C	-	-
XC2S100E	-6	C, I	C, I	C, I	C, I	-
	-7	C	C	C	C	-
XC2S150E	-6	-	C, I	C, I	C, I	-
	-7	-	C	C	C	-
XC2S200E	-6	-	C, I	C, I	C, I	-
	-7	-	C	C	C	-
XC2S300E	-6	-	C, I	C, I	C, I	-
	-7	-	C	C	C	-
XC2S400E	-6	-	-	(C, I)	(C, I)	(C, I)
	-7	-	-	(C)	(C)	(C)
XC2S600E	-6	-	-	-	(C, I)	(C, I)
	-7	-	-	-	(C)	(C)

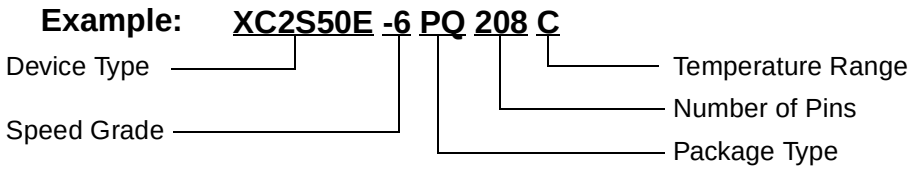
Notes:
1. C = Commercial, T_J = 0° to +85°C; I = Industrial, T_J = –40°C to +100°C.
2. Parentheses indicate product not yet released. Contact sales for availability.

Table 3: **Spartan-IIE User I/O Chart**

Device	Maximum User I/O	Available User I/O According to Package Type				
		TQ144	PQ208	FT256	FG456	FG676
XC2S50E	182	102	146	182	-	-
XC2S100E	202	102	146	182	202	-
XC2S150E	265	-	146	182	265	-
XC2S200E	289	-	146	182	289	-
XC2S300E	329	-	146	182	329	-
XC2S400E	410	-	-	182	329	410
XC2S600E	514	-	-	-	329	514

Notes:
1. User I/O counts include the four global clock/user input pins.

Ordering Information



Device Ordering Options

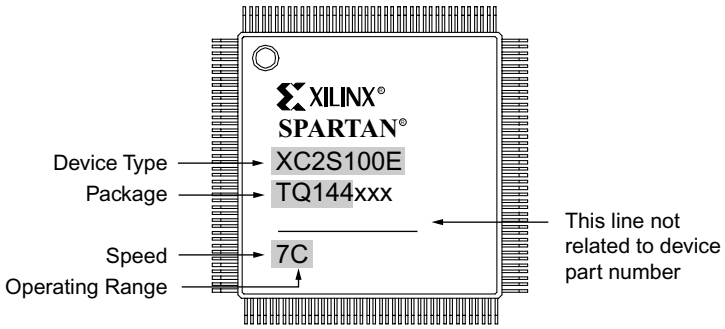
Device
XC2S50E
XC2S100E
XC2S150E
XC2S200E
XC2S300E
XC2S400E
XC2S600E

Speed Grade	
-6	Standard Performance
-7	Higher Performance

Package Type / Number of Pins	
TQ144	144-pin Plastic Thin QFP
PQ208	208-pin Plastic QFP
FT256	256-ball Fine Pitch BGA
FG456	456-ball Fine Pitch BGA
FG676	676-ball Fine Pitch BGA

Temperature Range (T_J)	
C = Commercial	0°C to +85°C
I = Industrial	–40°C to +100°C

Device Part Marking



Sample package with part marking.

The Spartan-IIE Family Data Sheet

DS077-1, ***Spartan-IIE 1.8V FPGA Family: Introduction and Ordering Information*** (Module 1)

DS077-2, ***Spartan-IIE 1.8V FPGA Family: Functional Description*** (Module 2)

DS077-3, ***Spartan-IIE 1.8V FPGA Family: DC and Switching Characteristics*** (Module 3)

DS077-4, ***Spartan-IIE 1.8V FPGA Family: Pinout Tables*** (Module 4)

Revision History

Date	Version No.	Description
11/15/01	1.0	Initial Xilinx release.
06/27/02	1.1	Updated -7 availability.
11/18/02	2.0	Added XC2S400E and XC2S600E. Corrected XC2S150E max I/O count and XC2S50E differential I/O count and updated availability.