Virtex-II Pro™ Platform FPGAs: DC and Switching Characteristics

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Advance Product Specification

Virtex-II Pro Electrical Characteristics

Virtex-II Pro devices are provided in -7, -6, and -5 speed grades, with -7 having the highest performance.

Virtex-II Pro DC and AC characteristics are specified for both commercial and industrial grades. Except the operating temperature range or unless otherwise noted, all the DC and AC electrical parameters are the same for a particular speed grade (that is, the timing characteristics of a -6 speed grade industrial device are the same as for a -6 speed grade commercial device). However, only selected speed grades and/or devices might be available in the industrial range.

All supply voltage and junction temperature specifications are representative of worst-case conditions. The parameters included are common to popular designs and typical applications. Contact Xilinx for design considerations requiring more detailed information.

All specifications are subject to change without notice.

Virtex-II Pro DC Characteristics

Table 1: **Absolute Maximum Ratings**

Symbol	Description		Units
V_{CCINT}	Internal supply voltage relative to GND	–0.5 to 1.6	V
V_{CCAUX}	Auxiliary supply voltage relative to GND	–0.5 to 3.0	V
V_{CCO}	Output drivers supply voltage relative to GND	–0.5 to 3.75	V
V_{BATT}	Key memory battery backup supply	–0.5 to 3.0	V
V_{REF}	Input reference voltage	–0.3 to 3.75	V
V_{IN}	3.3V I/O input voltage relative to GND (user and dedicated I/Os)	–0.3 to 3.75	V
	2.5V or below I/O input voltage relative to GND (user and dedicated I/Os)	–0.5 to V_{CCO} + 0.5	V
V_{TS}	Voltage applied to 3-state 3.3V output (user and dedicated I/Os)	–0.3 to 3.75	V
	Voltage applied to 3-state 2.5V or below output (user and dedicated I/Os)	–0.5 to V_{CCO} + 0.5	V
$V_{CCAUXRX}$	Auxilliary supply voltage relative to analog ground, GNDA (RocketIO pins)	–0.5 to 3.0	V
$V_{CCAUXTX}$	Auxilliary supply voltage relative to analog ground, GNDA (RocketIO pins)	–0.5 to 3.0	V
V_{TTX}	Terminal transmit supply voltage relative to GND (RocketIO pins)	–0.5 to 3.0	V
V_{TRX}	Terminal receive supply voltage relative to GND (RocketIO pins)	–0.5 to 3.0	V
T_{STG}	Storage temperature (ambient)	–65 to +150	°C
T_{SOL}	Maximum soldering temperature	+220	°C
T_J	Operating junction temperature	+125(2)	°C

Notes:

1. Stresses beyond those listed under Absolute Maximum Ratings might cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time might affect device reliability.
2. For 3.3V operation, T_J must be less than 100°C.

Table 2: **Recommended Operating Conditions**

Symbol	Description		Min	Max	Units
V_{CCINT}	Internal supply voltage relative to GND, T_J = 0 °C to +85°C	Commercial	1.425	1.575	V
	Internal supply voltage relative to GND, T_J = –40°C to +100°C	Industrial	1.425	1.575	V
V_{CCAUX}(1,2)	Auxiliary supply voltage relative to GND, T_J = 0 °C to +85°C	Commercial	2.375	2.625	V
	Auxiliary supply voltage relative to GND, T_J = –40°C to +100°C	Industrial	2.375	2.625	V
V_{CCO}(3)	Supply voltage relative to GND, T_J = 0 °C to +85°C	Commercial	1.2	3.45(5)	V
	Supply voltage relative to GND, T_J = –40°C to +100°C	Industrial	1.2	3.45(5)	V
V_{IN}	3.3V supply voltage relative to GND, T_J = 0 °C to +85°C	Commercial	GND – 0.2	3.45(5)	V
	3.3V supply voltage relative to GND, T_J = –40°C to +100°C	Industrial	GND – 0.2	3.45(5)	V
	2.5V and below supply voltage relative to GND, T_J = 0 °C to +85°C	Commercial	GND – 0.2	V_{CCO} + 0.2	V
	2.5V and below supply voltage relative to GND, T_J = –40°C to +100°C	Industrial	GND – 0.2	V_{CCO} + 0.2	V
V_{BATT}(4)	Battery voltage relative to GND, T_J = 0 °C to +85°C	Commercial	1.0	2.63	V
	Battery voltage relative to GND, T_J = –40°C to +100°C	Industrial	1.0	2.63	V
$V_{CCAUXRX}$,(6) $V_{CCAUXTX}$(6)	Auxilliary supply voltage relative to GNDA	Commercial	2.375	2.625	V
	Auxilliary supply voltage relative to GNDA	Industrial	2.375	2.625	V
V_{TTX}, V_{TRX}	Terminal supply voltage relative to GND	Commercial	1.8	2.625	V
	Terminal supply voltage relative to GND	Industrial	1.8	2.625	V

Notes:
1. For LVDS operation, V_{CCAUX} min is 2.37V and max is 2.63V.
2. Recommended maximum voltage droop for V_{CCAUX} is 10 mV/ms.
3. Configuration data is retained even if V_{CCO} drops to 0V.
4. If battery is not used, do not connect V_{BATT}.
5. For PCI and PCI-X, refer to **XAPP653**, available on the Xilinx website at **www.xilinx.com**.
6. **IMPORTANT!** All unused RocketIO transceivers in the FPGA must be connected to power and ground. If RocketIO transceivers in the FPGA are used, refer to the information on power filtering in the ***RocketIO Transceiver User Guide***. Unused transceivers can be powered by any 2.5V source, and passive filtering is not required.

Table 3: **DC Characteristics Over Recommended Operating Conditions**

Symbol	Description	Device	Min	Typ	Max	Units
V_{DRINT}	Data retention V_{CCINT} voltage (below which configuration data might be lost)	All	1.25			V
V_{DRI}	Data retention V_{CCAUX} voltage (below which configuration data might be lost)	All	2.0			V
I_{REF}	V_{REF} current per pin	All				µA
I_L	Input or output leakage current per pin	All				µA
C_{IN}	Input capacitance (sample tested)	All			10	pF
I_{RPU}	Pad pull-up (when selected) @ V_{in} = 0V, V_{CCO} = 2.5V (sample tested)	All				µA
I_{RPD}	Pad pull-down (when selected) @ V_{in} = 2.5V (sample tested)	All				µA
I_{BATT}	Battery supply current	All		100		nA
$I_{CCAUXTX}$	Operating $V_{CCAUXTX}$ supply current			60		mA
$I_{CCAUXRX}$	Operating $V_{CCAUXRX}$ supply current			35		mA
I_{TTX}	Operating I_{TTX} supply current when transmitter is AC coupled			30		mA
	Operating I_{TTX} supply current when transmitter is DC coupled			15		mA
I_{TRX}	Operating I_{TRX} supply current when receiver is AC coupled					mA
	Operating I_{TRX} supply current when receiver is DC coupled			15		mA
P_{CPU}	Power dissipation of PowerPC® 405 processor block			0.9		mW / MHz
P_{RXTX}	Power dissipation of RocketIO @ 3.125 Gb/s per channel			350		mW
	Power dissipation of RocketIO @ 2.5 Gb/s per channel			310		mW
	Power dissipation of RocketIO @ 1.25 Gb/s per channel			230		mW

Table 4: **Quiescent Supply Current**

Symbol	Description	Device	Min	Typ	Max	Units
I_{CCINTQ}	Quiescent V_{CCINT} supply current	XC2VP2				mA
		XC2VP4		150		mA
		XC2VP7		200		mA
		XC2VP20				mA
		XC2VP30				mA
		XC2VP40				mA
		XC2VP50				mA
		XC2VP70				mA
		XC2VP100				mA
		XC2VP125				mA
I_{CCOQ}	Quiescent V_{CCO} supply current	XC2VP2				mA
		XC2VP4		2		mA
		XC2VP7		2		mA
		XC2VP20				mA
		XC2VP30				mA
		XC2VP40				mA
		XC2VP50				mA
		XC2VP70				mA
		XC2VP100				mA
		XC2VP125				mA
I_{CCAUXQ}	Quiescent V_{CCAUX} supply current	XC2VP2				mA
		XC2VP4		5		mA
		XC2VP7		5		mA
		XC2VP20				mA
		XC2VP50				mA
		XC2VP40				mA
		XC2VP50				mA
		XC2VP70				mA
		XC2VP100				mA
		XC2VP125				mA

Notes:
1. With no output current loads, no active input pull-up resistors, all I/O pins are 3-state and floating.
2. If DCI or differential signaling is used, more accurate quiescent current estimates can be obtained by using the Power Estimator or XPOWER™.

Power-On Power Supply Requirements

Xilinx FPGAs require a certain amount of supply current during power-on to insure proper device operation. The actual current consumed depends on the power-on ramp rate of the power supply.

The V_{CCINT} power supply must ramp on no faster than 200 µs and no slower than 50 ms. Ramp-on is defined as: 0 V_{DC} to minimum supply voltages (see Table 2).

V_{CCAUX} and V_{CCO} can power on at any ramp rate. Power supplies can be turned on in any sequence, though V_{CCAUX} must power on before or with V_{CCO} for the specifications shown in Table 5 to apply.

Table 5 shows the minimum current required by Virtex-II Pro devices for proper power-on and configuration.

If the current minimums shown in Table 5 are met, the device powers on properly after all three supplies have passed through their power-on reset threshold voltages.

Once initialized and configured, use the power calculator to estimate current drain on these supplies.

For more information on V_{CCAUX}, V_{CCO}, and configuration mode, refer to Chapter 3 in the *Virtex-II Pro Platform FPGA User Guide*.

Table 5: **Power-On Current for Virtex-II Pro Devices**

Symbol	Device										Units
	XC2VP2	XC2VP4	XC2VP7	XC2VP20	XC2VP30	XC2VP40	XC2VP50	XC2VP70	XC2VP100	XC2VP125	
$I_{CCINTMIN}$	500	500	500	500	TBD	TBD	TBD	TBD	TBD	TBD	mA
$I_{CCAUXMIN}$	250	250	250	250	250	250	250	250	250	250	mA
I_{CCOMIN}	100	100	100	100	100	100	100	100	100	100	mA

General Power Supply Requirements

Proper decoupling of all FPGA power supplies is essential. Consult Xilinx **Application Note 623** for detailed information on power distribution system design.

V_{CCAUX} powers critical resources in the FPGA. Therefore, this supply voltage is especially susceptible to power supply noise. V_{CCAUX} can share a power plane with V_{CCO}, but only if V_{CCO} does not have excessive noise. Staying within simultaneously switching output (SSO) limits is essential for keeping power supply noise to a minimum. More information on SSO is available at **support.xilinx.com** in Xilinx Answer Record 11713.

Changes in V_{CCAUX} voltage beyond 200 mV peak-to-peak should take place at a rate no faster than 10 mV per millisecond.

Recommended practices that can help reduce jitter and period distortion are described in Xilinx Answer Record 13756.

SelectIO-Ultra DC Input and Output Levels

Values for V_{IL} and V_{IH} are recommended input voltages. Values for I_{OL} and I_{OH} are guaranteed over the recommended operating conditions at the V_{OL} and V_{OH} test points. Only selected standards are tested. These are chosen to ensure that all standards meet their specifications. The selected standards are tested at minimum V_{CCO} with the respective V_{OL} and V_{OH} voltage levels shown. Other standards are sample tested.

Table 6: **DC Input and Output Levels**

Input/Output Standard	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}
	V, min	V, max	V, min	V, max	V, Max	V, Min	mA	mA
LVTTL	–0.3	0.8	2.0	3.6	0.4	2.4	24	–24
LVCMOS33	–0.3	0.8	2.0	3.6	0.4	V_{CCO} – 0.4	24	–24
LVCMOS25	–0.5	0.7	1.7	V_{CCO} + 0.4	0.4	V_{CCO} – 0.4	24	–24
LVCMOS18	–0.5	20% V_{CCO}	70% V_{CCO}	V_{CCO} + 0.4	0.4	V_{CCO} – 0.45	16	–16
LVCMOS15	–0.5	20% V_{CCO}	70% V_{CCO}	V_{CCO} + 0.4	0.4	V_{CCO} – 0.45	16	–16
PCI33_3	–0.3	30% V_{CCO}	50% V_{CCO}	3.6	10% V_{CCO}	90% V_{CCO}		
PCI66_3	–0.3	30% V_{CCO}	50% V_{CCO}	3.6	10% V_{CCO}	90% V_{CCO}		
PCI-X	–0.3	Note (1)	Note (1)	Note (1)	Note (1)	Note (1)	Note (1)	Note (1)
GTLP	–0.5	V_{REF} – 0.1	V_{REF} + 0.1	V_{CCO} + 0.4	0.6	n/a	36	n/a
GTL	–0.5	V_{REF} – 0.05	V_{REF} + 0.05	V_{CCO} + 0.4	0.4	n/a	40	n/a
HSTL I	–0.5	V_{REF} – 0.1	V_{REF} + 0.1	V_{CCO} + 0.4	0.4(2)	V_{CCO} – 0.4	8(2)	–8(2)
HSTL II	–0.5	V_{REF} – 0.1	V_{REF} + 0.1	V_{CCO} + 0.4	0.4(2)	V_{CCO} – 0.4	16(2)	–16(2)
HSTL III	–0.5	V_{REF} – 0.1	V_{REF} + 0.1	V_{CCO} + 0.4	0.4(2)	V_{CCO} – 0.4	24(2)	–8(2)
HSTL IV	–0.5	V_{REF} – 0.1	V_{REF} + 0.1	V_{CCO} + 0.4	0.4(2)	V_{CCO} – 0.4	48(2)	–8(2)
SSTL2 I	–0.3	V_{REF} – 0.15	V_{REF} + 0.15	V_{CCO} + 0.3	V_{TT} – 0.61	V_{TT} + 0.61	8.1	–8.1
SSTL2 II	–0.3	V_{REF} – 0.15	V_{REF} + 0.15	V_{CCO} + 0.3	V_{TT} – 0.81	V_{TT} + 0.81	16.2	–16.2
SSTL18 I	–0.3	V_{REF} – 0.125	V_{REF} + 0.125	V_{CCO} + 0.3	V_{TT} – 0.61	V_{TT} + 0.61	6.7	–6.7
SSTL18 II	–0.3	V_{REF} – 0.125	V_{REF} + 0.125	V_{CCO} + 0.3	V_{TT} – 0.61	V_{TT} + 0.61	13.4	–13.4

Notes:
1. Tested according to relevant specifications.
2. This applies to 1.5V and 1.8V HSTL.

LDT DC Specifications (LDT_25)

Table 7: **LDT DC Specifications**

DC Parameter	Symbol	Conditions	Min	Typ	Max	Units
Supply Voltage	V_{CCO}		2.38	2.5	2.63	V
Differential Output Voltage	V_{OD}	R_T = 100 ohm across Q and $\overline{Q}$ signals	495	600	715	mV
Change in V_{OD} Magnitude	ΔV_{OD}		–15		15	mV
Output Common Mode Voltage	V_{OCM}	R_T = 100 ohm across Q and $\overline{Q}$ signals	495	600	715	mV
Change in V_{OS} Magnitude	ΔV_{OCM}		–15		15	mV
Input Differential Voltage	V_{ID}		200	600	1000	mV

Table 7: **LDT DC Specifications *(Continued)***

DC Parameter	Symbol	Conditions	Min	Typ	Max	Units
Change in V_{ID} Magnitude	ΔV_{ID}		–15		15	mV
Input Common Mode Voltage	V_{ICM}		440	600	780	mV
Change in V_{ICM} Magnitude	ΔV_{ICM}		–15		15	mV

LVDS DC Specifications (LVDS_25)

Table 8: **LVDS DC Specifications**

DC Parameter	Symbol	Conditions	Min	Typ	Max	Units
Supply Voltage	V_{CCO}		2.38	2.5	2.63	V
Output High Voltage for Q and $\overline{Q}$	V_{OH}	R_T = 100 Ω across Q and $\overline{Q}$ signals			1.602	V
Output Low Voltage for Q and $\overline{Q}$	V_{OL}	R_T = 100 Ω across Q and $\overline{Q}$ signals	0.898			V
Differential Output Voltage (Q – $\overline{Q}$), Q = High ($\overline{Q}$ – Q), $\overline{Q}$ = High	V_{ODIFF}	R_T = 100 Ω across Q and $\overline{Q}$ signals	247	350	454	mV
Output Common-Mode Voltage	V_{OCM}	R_T = 100 Ω across Q and $\overline{Q}$ signals	1.125	1.2	1.375	V
Differential Input Voltage (Q – $\overline{Q}$), Q = High ($\overline{Q}$ – Q), $\overline{Q}$ = High	V_{IDIFF}	Common-mode input voltage = 1.25V	100	350	600	mV
Input Common-Mode Voltage	V_{ICM}	Differential input voltage = ±350 mV	0.3	1.2	2.2	V

Extended LVDS DC Specifications (LVDSEXT_25)

Table 9: **Extended LVDS DC Specifications**

DC Parameter	Symbol	Conditions	Min	Typ	Max	Units
Supply Voltage	V_{CCO}		2.38	2.5	2.63	V
Output High Voltage for Q and $\overline{Q}$	V_{OH}	R_T = 100 Ω across Q and $\overline{Q}$ signals			1.785	V
Output Low Voltage for Q and $\overline{Q}$	V_{OL}	R_T = 100 Ω across Q and $\overline{Q}$ signals	0.715			V
Differential Output Voltage (Q – $\overline{Q}$), Q = High ($\overline{Q}$ – Q), $\overline{Q}$ = High	V_{ODIFF}	R_T = 100 Ω across Q and $\overline{Q}$ signals	440		820	mV
Output Common-Mode Voltage	V_{OCM}	R_T = 100 Ω across Q and $\overline{Q}$ signals	1.125	1.250	1.375	V
Differential Input Voltage (Q – $\overline{Q}$), Q = High ($\overline{Q}$ – Q), $\overline{Q}$ = High	V_{IDIFF}	Common-mode input voltage = 1.25V	100		1000	mV
Input Common-Mode Voltage	V_{ICM}	Differential input voltage = ±350 mV	0.3	1.2	2.2	V

LVPECL DC Specifications (LVPECL_25)

Table 10: **LVPECL DC Specifications**

DC Parameter	V_{CCO} = 2.375V		V_{CCO} = 2.5V		V_{CCO} = 2.825V		Units
	Min	Max	Min	Max	Min	Max	
V_{OH}	1.35	1.495	1.475	1.62	1.6	1.745	V
V_{OL}	0.565	0.755	0.69	0.88	0.815	1.005	V
V_{IH}	1.34	1.495	1.465	1.62	1.59	1.745	V
V_{IL}	0.565	0.765	0.69	0.89	0.815	1.015	V
Differential Input Voltage	0.345	-	0.345	-	0.345	-	V

RocketIO DC Input and Output Levels

Table 11: **RocketIO DC Specifications**

DC Parameter	Symbol	Conditions	Min	Typ	Max	Units
Peak-to-Peak Differential Input Voltage	DV_{IN}		175		2000	mV
Single-Ended Output Voltage Swing(1,2)	DV_{OUT}			400		mV
				500		mV
				600		mV
				700		mV
				800		mV
Peak-to-Peak Differential Output Voltage(1,2)	DV_{PPOUT}			800		mV
				1000		mV
				1200		mV
				1400		mV
				1600		mV

Notes:
1. Output swing levels are selectable using TX_DIFF_CTRL attribute. Refer to the *RocketIO Transceiver User Guide* for details.
2. Output preemphasis levels are selectable at 10% (default), 20%, 25%, and 33% using the TX_PREEMPHASIS attribute. Refer to the *RocketIO Transceiver User Guide* or Chapter 2 in the *Virtex-II Pro Platform FPGA User Guide* for details.

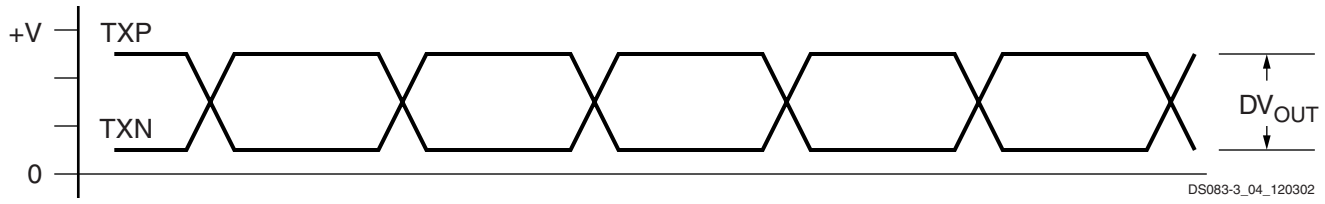

Figure 1: **Single-Ended Output Voltage Swing**

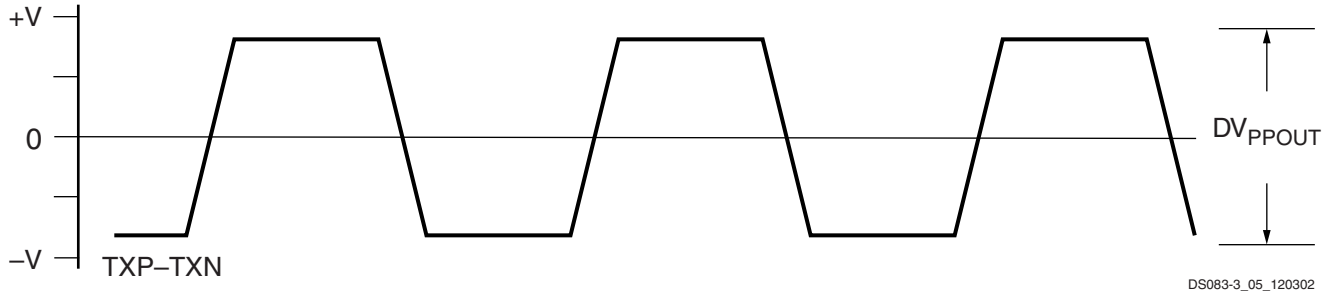

Figure 2: **Peak-to-Peak Differential Output Voltage**

Virtex-II Pro Performance Characteristics

This section provides the performance characteristics of some common functions and designs implemented in Virtex-II Pro devices. The numbers reported here are fully characterized worst-case values. Note that these values are subject to the same guidelines as Virtex-II Pro Switching Characteristics (speed files).

Table 12 provides pin-to-pin values (in nanoseconds) including IOB delays; that is, delay through the device from input pin to output pin. In the case of multiple inputs and outputs, the worst delay is reported.

Table 12: **Pin-to-Pin Performance**

Description	Pin-to-Pin (w/ I/O delays)	Units	Device Used & Speed Grade
Basic Functions:			
16-bit Address Decoder		ns	XC2VP7FF672-6
32-bit Address Decoder		ns	XC2VP7FF672-6
64-bit Address Decoder		ns	XC2VP7FF672-6
4:1 MUX		ns	XC2VP7FF672-6
8:1 MUX		ns	XC2VP7FF672-6
16:1 MUX		ns	XC2VP7FF672-6
32:1 MUX		ns	XC2VP7FF672-6
Combinatorial (pad to LUT to pad)		ns	XC2VP7FF672-6
Memory:			
Block RAM			
Pad to setup		ns	XC2VP7FF672-6
Clock to Pad		ns	XC2VP7FF672-6
Distributed RAM			
Pad to setup		ns	XC2VP7FF672-6
Clock to Pad		ns	XC2VP7FF672-6

Table 13 shows internal (register-to-register) performance. Values are reported in MHz.

Table 13: **Register-to-Register Performance**

Description	Register-to-Register Performance	Units	Device Used & Speed Grade
Basic Functions:			
16-bit Address Decoder		MHz	XC2VP7FF672-6
32-bit Address Decoder		MHz	XC2VP7FF672-6
64-bit Address Decoder		MHz	XC2VP7FF672-6
4:1 MUX		MHz	XC2VP7FF672-6
8:1 MUX		MHz	XC2VP7FF672-6
16:1 MUX		MHz	XC2VP7FF672-6
32:1 MUX		MHz	XC2VP7FF672-6
Register to LUT to Register		MHz	XC2VP7FF672-6
8-bit Adder		MHz	XC2VP7FF672-6
16-bit Adder		MHz	XC2VP7FF672-6
64-bit Adder		MHz	XC2VP7FF672-6
64-bit Counter		MHz	XC2VP7FF672-6
64-bit Accumulator		MHz	XC2VP7FF672-6

Table 13: **Register-to-Register Performance *(Continued)***

Description	Register-to-Register Performance	Units	Device Used & Speed Grade
Multiplier 18x18 (with Block RAM inputs)		MHz	XC2VP7FF672-6
Multiplier 18x18 (with Register inputs)		MHz	XC2VP7FF672-6
Memory:			
Block RAM			
Single-Port 4096 x 4 bits		MHz	XC2VP7FF672-6
Single-Port 2048 x 9 bits		MHz	XC2VP7FF672-6
Single-Port 1024 x 18 bits		MHz	XC2VP7FF672-6
Single-Port 512 x 36 bits		MHz	XC2VP7FF672-6
Dual-Port A:4096 x 4 bits & B:1024 x 18 bits		MHz	XC2VP7FF672-6
Dual-Port A:1024 x 18 bits & B:1024 x 18 bits		MHz	XC2VP7FF672-6
Dual-Port A:2048 x 9 bits & B: 512 x 36 bits		MHz	XC2VP7FF672-6
Distributed RAM			
Single-Port 32 x 8-bit		MHz	XC2VP7FF672-6
Single-Port 64 x 8-bit		MHz	XC2VP7FF672-6
Single-Port 128 x 8-bit		MHz	XC2VP7FF672-6
Dual-Port 16 x 8		MHz	XC2VP7FF672-6
Dual-Port 32 x 8		MHz	XC2VP7FF672-6
Dual-Port 64 x 8		MHz	XC2VP7FF672-6
Dual-Port 128 x 8		MHz	XC2VP7FF672-6
Shift Registers			
128-bit SRL		MHz	XC2VP7FF672-6
256-bit SRL		MHz	XC2VP7FF672-6
FIFOs (Async. in Block RAM)			
1024 x 18-bit		MHz	XC2VP7FF672-6
1024 x 18-bit		MHz	XC2VP7FF672-6
FIFOs (Sync. in SRL)			
128 x 8-bit		MHz	XC2VP7FF672-6
128 x 16-bit		MHz	XC2VP7FF672-6
CAMs in Block RAM			
32 x 9-bit		MHz	XC2VP7FF672-6
64 x 9-bit		MHz	XC2VP7FF672-6
128 x 9-bit		MHz	XC2VP7FF672-6
256 x 9-bit		MHz	XC2VP7FF672-6
CAMs in SRL			
32 x 16-bit		MHz	XC2VP7FF672-6
64 x 32-bit		MHz	XC2VP7FF672-6
128 x 40-bit		MHz	XC2VP7FF672-6
256 x 48-bit		MHz	XC2VP7FF672-6
1024 x 16-bit		MHz	XC2VP7FF672-6
1024 x 72-bit		MHz	XC2VP7FF672-6

Virtex-II Pro Switching Characteristics

Switching characteristics are specified on a per-speed-grade basis and can be designated as Advance, Preliminary, or Production. Note that Virtex-II Pro Performance Characteristics are subject to these guidelines, as well. Each designation is defined as follows:

Advance: These speed files are based on simulations only and are typically available soon after device design specifications are frozen. Although speed grades with this designation are considered relatively stable and conservative, some under-reporting might still occur.

Preliminary: These speed files are based on complete ES (engineering sample) silicon characterization. Devices and speed grades with this designation are intended to give a better indication of the expected performance of production silicon. The probability of under-reporting delays is greatly reduced as compared to Advance data.

Production: These speed files are released once enough production silicon of a particular device family member has been characterized to provide full correlation between speed files and devices over numerous production lots. There is no under-reporting of delays, and customers receive formal notification of any subsequent changes. Typically, the slowest speed grades transition to Production before faster speed grades.

Since individual family members are produced at different times, the migration from one category to another depends completely on the status of the fabrication process for each device. Table 14 correlates the current status of each Virtex-II Pro device with a corresponding speed file designation.

All specifications are always representative of worst-case supply voltage and junction temperature conditions.

Table 14: **Virtex-II Pro Device Speed Grade Designations**

Device	Speed Grade Designations		
	Advance	Preliminary	Production
XC2VP2	-7, -6, -5		
XC2VP4	-7, -6, -5		
XC2VP7	-7, -6, -5		
XC2VP20	-7, -6, -5		
XC2VP30			
XC2VP40			
XC2VP50	-7, -6, -5		
XC2VP70			
XC2VP100			
XC2VP125			

Testing of Switching Characteristics

All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotate to the simulation net list. Unless otherwise noted, values apply to all Virtex-II Pro devices.

PowerPC Switching Characteristics

Table 15: **Processor Clocks Absolute AC Characteristics**

Description	Speed Grade						Units
	-7		-6		-5		
	Min	Max	Min	Max	Min	Max	
CPMC405CLOCK frequency	0	400	0	350	0	300	MHz
JTAGC405TCK frequency(1)	0	200	0	175	0	150	MHz
PLBCLK(2)	0	400	0	350	0	300	MHz
BRAMDSOCMCLK(2)	0	‘400	0	350	0	300	MHz
BRAMISOCMCLK(2)	0	400	0	350	0	300	MHz

Notes:
1. The theoretical maximum frequency of this clock is one-half the CPMC405CLOCK. However, the achievable maximum is dependent on the system, and will be much less.
2. The theoretical maximum frequency of these clocks is equal to the CPMC405CLOCK. However, the achievable maximum is dependent on the system. Please see ***PPC405 Processor Block Manual*** and **XAPP640** for more information.

Table 16: **Processor Block Switching Characteristics**

Description	Symbol	Speed Grade			Units
		-7	-6	-5	
Setup and Hold Relative to Clock (CPMC405CLOCK)					
Device Control Register Bus control inputs	$T_{PCCK\_}DCR/T_{PCKC\_}DCR$		0.56/ –0.23	0.61/–0.25	ns, min
Device Control Register Bus data inputs	$T_{PDCK\_}DCR/T_{PCKD\_}DCR$		0.82/ –0.02	0.91/–0.02	ns, min
Clock and Power Management control inputs	$T_{PCCK\_}CPM/T_{PCKC\_}CPM$		0.20/ 0.03	0.22/ 0.04	ns, min
Reset control inputs	$T_{PCCK\_}RST/T_{PCKC\_}RST$		0.20/0.03	0.22/ 0.04	ns, min
Debug control inputs	$T_{PCCK\_}DBG/T_{PCKC\_}DBG$		0.34/0.38	0.38/ 0.42	ns, min
Trace control inputs	$T_{PCCK\_}TRC/T_{PCKC\_}TRC$		1.73/–0.52	1.90/–0.58	ns, min
External Interrupt Controller control inputs	$T_{PCCK\_}EIC/T_{PCKC\_}EIC$		0.72/–0.27	0.79/–0.30	ns, min
Clock to Out					
Device Control Register Bus control outputs	$T_{PCKCO\_}DCR$		1.67	1.84	ns, max
Device Control Register Bus address outputs	$T_{PCKAO\_}DCR$		2.17	2.39	ns, max
Device Control Register Bus data outputs	$T_{PCKDO\_}DCR$		2.22	2.44	ns, max
Clock and Power Management control outputs	$T_{PCKCO\_}CPM$		1.59	1.75	ns, max
Reset control outputs	$T_{PCKCO\_}RST$		1.66	1.83	ns, max
Debug control outputs	$T_{PCKCO\_}DBG$		2.44	2.69	ns, max
Trace control outputs	$T_{PCKCO\_}TRC$		1.71	1.88	ns, max
Clock					
CPMC405CLOCK minimum pulse width, high	T_{CPWH}				ns, min
CPMC405CLOCK minimum pulse width, low	T_{CPWL}				ns, min

Table 17: **Processor Block PLB Switching Characteristics**

Description	Symbol	Speed Grade			Units
		-7	-6	-5	
Setup and Hold Relative to Clock (PLBCLK)					
Processor Local Bus(ICU/DCU) control inputs	$T_{PCCK\_}PLB/T_{PCKC\_}PLB$		1.23/0.23	1.35/ 0.25	ns, min
Processor Local Bus (ICU/DCU) data inputs	$T_{PDCK\_}PLB/T_{PCKD\_}PLB$		0.78/0.20	0.86/ 0.22	ns, min
Clock to Out					
Processor Local Bus(ICU/DCU) control outputs	$T_{PCKCO\_}PLB$		1.69	1.86	ns, max
Processor Local Bus(ICU/DCU) address bus outputs	$T_{PCKAO\_}PLB$		1.47	1.61	ns, max
Processor Local Bus(ICU/DCU) data bus outputs	$T_{PCKDO\_}PLB$		1.81	1.99	ns, max

Table 18: **Processor Block JTAG Switching Characteristics**

		Speed Grade			
Description	**Symbol**	**-7**	**-6**	**-5**	**Units**
Setup and Hold Relative to Clock (JTAGC405TCK)					
JTAG control inputs	$T_{PCCK_}$JTAG/$T_{PCKC_}$JTAG		0.80/0.70	0.88/ 0.77	ns, min
JTAG reset input	$T_{PCCK_}$JTAGRST/ $T_{PCKC_}$JTAGRST		0.80/0.70	0.88/ 0.77	ns, min
Clock to Out					
JTAG control outputs	$T_{PCKCO_}$JTAG		1.69	1.86	ns, max

Table 19: **PowerPC 405 Data-Side On-Chip Memory Switching Characteristics**

		Speed Grade			
Description	**Symbol**	**-7**	**-6**	**-5**	**Units**
Setup and Hold Relative to Clock (BRAMDSOCMCLK)					
Data-Side On-Chip Memory data bus inputs	$T_{PDCK_}$DSOCM/ $T_{PCKD_}$DSOCM		0.92/1.05	1.02/ 1.15	ns, min
Clock to Out					
Data-Side On-Chip Memory control outputs	$T_{PCKCO_}$DSOCM		2.63	2.90	ns, max
Data-Side On-Chip Memory address bus outputs	$T_{PCKAO_}$DSOCM		3.20	3.52	ns, max
Data-Side On-Chip Memory data bus outputs	$T_{PCKDO_}$DSOCM		1.13	1.25	ns, max

Table 20: **PowerPC 405 Instruction-Side On-Chip Memory Switching Characteristics**

		Speed Grade			
Description	**Symbol**	**-7**	**-6**	**-5**	**Units**
Setup and Hold Relative to Clock (BRAMISOCMCLK)					
Instruction-Side On-Chip Memory data bus inputs	$T_{PDCK_}$ISOCM/ $T_{PCKD_}$ISOCM		1.02/0.86	1.12/ 0.95	ns, min
Clock to Out					
Instruction-Side On-Chip Memory control outputs	$T_{PCKCO_}$ISOCM		1.68	1.85	ns, max
Instruction-Side On-Chip Memory address bus outputs	$T_{PCKAO_}$ISOCM		2.05	2.25	ns, max
Instruction-Side On-Chip Memory data bus outputs	$T_{PCKDO_}$ISOCM		1.20	1.32	ns, max

RocketIO Switching Characteristics

Table 21: **RocketIO Reference Clock Switching Characteristics**

			All Speed Grades			
Description	**Symbol**	**Conditions**	**Min**	**Typ**	**Max**	**Units**
Reference Clock frequency range(1)	F_{GCLK}	Full rate operation	40		156.25	MHz
		Half rate operation	62.2		100	MHz
Reference Clock frequency tolerance	F_{GTOL}				±100	ppm
Reference Clock rise time	T_{RCLK}	20% – 80%		600	1000	ps
Reference Clock fall time	T_{FCLK}	20% – 80%		600	1000	ps
Reference Clock duty cycle	T_{DCREF}		45	50	55	%
Reference Clock total jitter(2)	T_{GJTT}	peak-to-peak			40	ps
Clock recovery frequency acquisition time	T_{LOCK}			10		µs
Clock recovery phase acquisition time	T_{PHASE}			960		bits

Notes:
1. BREFCLK/BREFCLK2 can be used for all serial bit rates up to the maximum shown. REFCLK/REFCLK2 can be used for serial bit rates up to 2.5 Gb/s (REFCLK = 125 MHz). All other parameters apply equally to REFCLK, REFCLK2, BREFCLK, and BREFCLK2 except as noted.
2. Measured at the package pin. For reference clock frequencies equal to or above 125 MHz, BREFCLK/BREFCLK2 must be used.

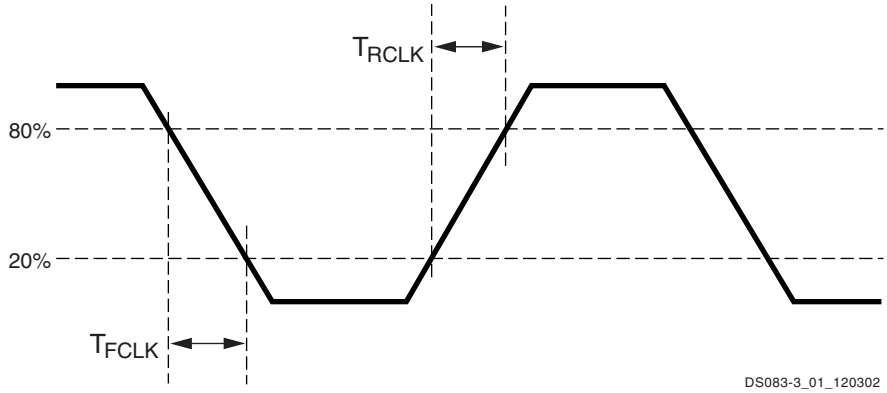

Figure 3: **Reference Clock Timing Parameters**

Table 22: **RocketIO Receiver Switching Characteristics**

Description	Symbol	Conditions	Min	Typ	Max	Units
Receive total jitter tolerance	T_{JTOL}				0.65	UI(1)
Receive deterministic jitter tolerance	T_{DJTOL}				0.41	UI
Receive latency(2)	T_{RXLAT}			25	42	RXUSRCLK cycles
RXUSRCLK duty cycle	T_{RXDC}		45	50	55	%
RXUSRCLK2 duty cycle	T_{RX2DC}		45	50	55	%
Bit error rate	BER				10^{-12}	

Notes:
1. UI = Unit Interval
2. Receive latency delay RXP/RXN to RXDATA. Refer to ***RocketIO Transceiver User Guide*** for more information on calculating latency.

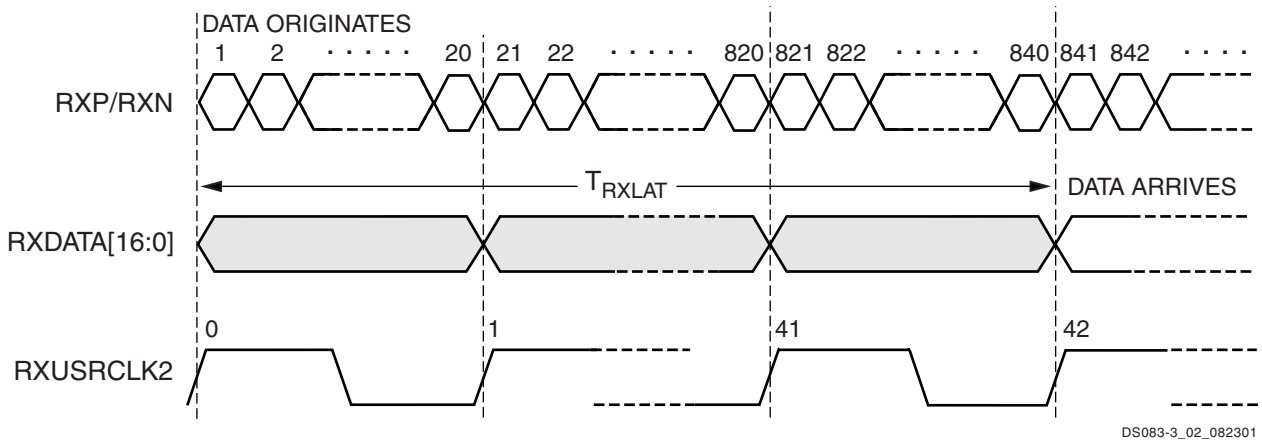

Figure 4: **Receive Latency (Maximum)**

Table 23: **RocketIO Transmitter Switching Characteristics**

Description	Symbol	Conditions	Min	Typ	Max	Units
Serial data rate, full-speed clock	F_{GTX}	Flipchip packages	0.800		3.125(1)	Gb/s
		Wirebond packages	0.800		2.5(1)	Gb/s
Serial data rate, half-speed clock		Flipchip packages	0.622		1.0	Gb/s
		Wirebond packages	0.622		1.0	Gb/s
Serial data output deterministic jitter	T_{DJ}				0.18	UI(2)
Serial data output random jitter	T_{RJ}				0.17	UI
TX rise time	T_{RTX}	20% – 80%		120		ps
TX fall time	T_{FTX}			120		ps
Transmit latency(3)	T_{TXLAT}	Including CRC		14	17	TXUSR CLK cycles
		Excluding CRC		8	11	
TXUSRCLK duty cycle	T_{TXDC}		45	50	55	%
TXUSRCLK2 duty cycle	T_{TX2DC}		45	50	55	%

Notes:
1. Serial data rate in the -5 speed grade is limited to 2.0 Gb/s in both wirebond and flipchip packages.
2. UI = Unit Interval
3. Transmit latency delay TXDATA to TXP/TXN. Refer to ***RocketIO Transceiver User Guide*** for more information on calculating latency.

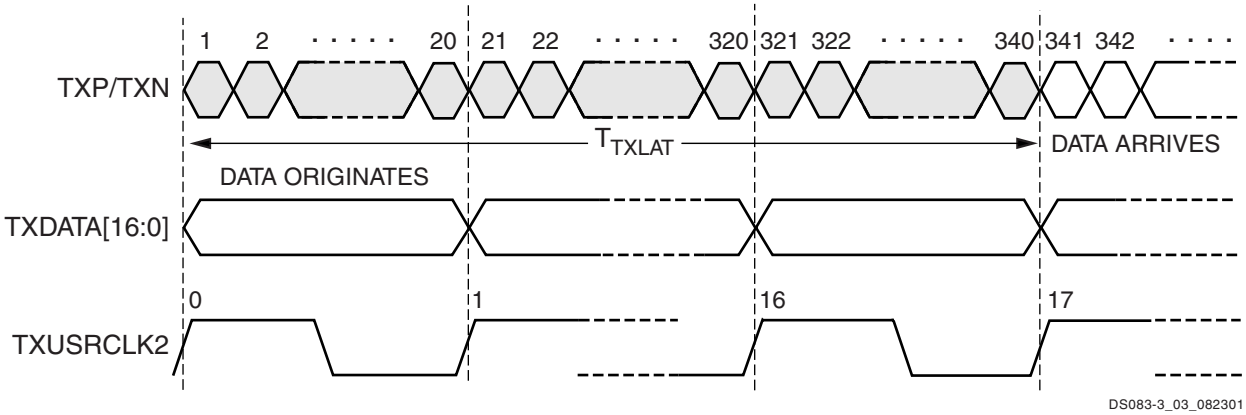

Figure 5: **Transmit Latency (Maximum, Including CRC)**

Table 24: **RocketIO RXUSRCLK Switching Characteristics**

		Speed Grade			
Description	**Symbol**	**-7**	**-6**	**-5**	**Units**
Setup and Hold Relative to Clock (RXUSRCLK)					
CHBONDI control inputs	$T_{GCCK\_}CHBI/T_{GCKC\_}CHBI$	0.00/0.12	0.00/0.12	0.00/ 0.14	ns, min
Clock to Out					
CHBONDO control outputs	$T_{GCKCO\_}CHBO$	0.50	0.50	0.55	ns, max
Clock					
RXUSRCLK minimum pulse width, High	$T_{GPWH\_}RX$	0.80	0.80	0.88	ns, min
RXUSRCLK minimum pulse width, Low	$T_{GPWL\_}RX$	0.40	0.40	0.44	ns, min

Table 25: **RocketIO RXUSRCLK2 Switching Characteristics**

		Speed Grade			
Description	**Symbol**	**-7**	**-6**	**-5**	**Units**
Setup and Hold Relative to Clock (RXUSRCLK2)					
RXRESET control input	$T_{GCCK\_}RRST/T_{GCKC\_}RRST$	0.02/0.00	0.02/0.00	0.02/0.00	ns, min
RXPOLARITY control input	$T_{GCCK\_}RPOL/T_{GCKC\_}RPOL$	0.02/0.00	0.02/0.00	0.02/0.00	ns, min
ENCHANSYNC control input	$T_{GCCK\_}ECSY/T_{GCKC\_}ECSY$	0.02/0.00	0.02/0.00	0.02/0.00	ns, min
Clock to Out					
RXNOTINTABLE status outputs	$T_{GCKST\_}RNIT$	0.50	0.50	0.55	ns, max
RXDISPERR status outputs	$T_{GCKST\_}RDERR$	0.50	0.50	0.55	ns, max
RXCHARISCOMMA status outputs	$T_{GCKST\_}RCMCH$	0.50	0.50	0.55	ns, max
RXREALIGN status output	$T_{GCKST\_}ALIGN$	0.41	0.41	0.46	ns, max
RXCOMMADET status output	$T_{GCKST\_}CMDT$	0.41	0.41	0.46	ns, max
RXLOSSOFSYNC status outputs	$T_{GCKST\_}RLOS$	0.50	0.50	0.55	ns, max
RXCLKCORCNT status outputs	$T_{GCKST\_}RCCCNT$	0.41	0.41	0.46	ns, max
RXBUFSTATUS status outputs	$T_{GCKST\_}RBSTA$	0.45	0.45	0.50	ns, max
RXCHECKINGCRC status output	$T_{GCKST\_}RCCRC$	0.36	0.40	0.44	ns, max
RXCRCERR status output	$T_{GCKST\_}RCRCE$	0.36	0.40	0.44	ns, max
CHBONDDONE status output	$T_{GCKST\_}CHBD$	0.50	0.50	0.55	ns, max
RXCHARISK status outputs	$T_{GCKST\_}RKCH$	0.50	0.50	0.55	ns, max
RXRUNDISP status outputs	$T_{GCKST\_}RRDIS$	0.50	0.50	0.55	ns, max
RXDATA data outputs	$T_{GCKDO\_}RDAT$	0.50	0.50	0.55	ns, max
Clock					
RXUSRCLK2 minimum pulse width, High	$T_{GPWH\_}RX2$	0.40	0.40	0.44	ns, min
RXUSRCLK2 minimum pulse width, Low	$T_{GPWL\_}RX2$	0.20	0.20	0.22	ns, min

Table 26: **RocketIO TXUSRCLK Switching Characteristics**

		Speed Grade			
Description	**Symbol**	**-7**	**-6**	**-5**	**Units**
Setup and Hold Relative to Clock (TXUSRCLK2)					
CONFIGENABLE control input	$T_{GCCK\_}CFGEN/T_{GCKC\_}CFGEN$	0.35/0.10	0.35/0.10	0.39/ 0.11	ns, min
TXBYPASS8B10B control inputs	$T_{GCCK\_}TBYP/T_{GCKC\_}TBYP$	0.02/0.00	0.02/0.00	0.02/ 0.00	ns, min
TXFORCECRCERR control input	$T_{GCCK\_}TCRCE/T_{GCKC\_}TCRCE$	0.39/0.12	0.44/0.14	0.49/ 0.15	ns, min
TXPOLARITY control input	$T_{GCCK\_}TPOL/T_{GCKC\_}TPOL$	0.02/0.00	0.02/0.00	0.02/ 0.00	ns, min
TXINHIBIT control inputs	$T_{GCCK\_}TINH/T_{GCKC\_}TINH$	0.02/0.00	0.02/0.00	0.02/ 0.00	ns, min
LOOPBACK control inputs	$T_{GCCK\_}LBK/T_{GCKC\_}LBK$	0.02/0.00	0.02/0.00	0.02/ 0.00	ns, min
TXRESET control input	$T_{GCCK\_}TRST/T_{GCKC\_}TRST$	0.02/0.10	0.02/0.10	0.02/ 0.11	ns, min
TXCHARISK control inputs	$T_{GCCK\_}TKCH/T_{GCKC\_}TKCH$	0.02/0.00	0.02/0.00	0.02/ 0.00	ns, min
TXCHARDISPMODE control inputs	$T_{GCCK\_}TCDM/T_{GCKC\_}TCDM$	0.02/0.00	0.02/0.00	0.02/ 0.00	ns, min
TXCHARDISPVAL control inputs	$T_{GCCK\_}TCDV/T_{GCKC\_}TCDV$	0.02/0.00	0.02/0.00	0.02/ 0.00	ns, min
CONFIGIN data input	$T_{GDCK\_}CFGIN/T_{GCKD\_}CFGIN$	0.35/0.10	0.35/0.10	0.39/ 0.11	ns, min
TXDATA data inputs	$T_{GDCK\_}TDAT/T_{GCKD\_}TDAT$	0.02/0.00	0.02/0.00	0.02/ 0.00	ns, min
Clock to Out					
TXBUFERR status output	$T_{GCKST\_}TBERR$	0.54	0.54	0.60	ns, max
TXKERR status outputs	$T_{GCKST\_}TKERR$	0.41	0.41	0.46	ns, max
TXRUNDISP status outputs	$T_{GCKST\_}TRDIS$	0.41	0.41	0.46	ns, max
CONFIGOUT data output	$T_{GCKDO\_}CFGOUT$	0.25	0.25	0.28	ns, max
Clock					
TXUSRCLK minimum pulse width, High	$T_{GPWH\_}TX$	0.80	0.80	0.88	ns, min
TXUSRCLK minimum pulse width, Low	$T_{GPWL\_}TX$	0.40	0.40	0.44	ns, min
TXUSRCLK2 minimum pulse width, High	$T_{GPWH\_}TX2$	0.40	0.40	0.44	ns, min
TXUSRCLK2 minimum pulse width, Low	$T_{GPWL\_}TX2$	0.20	0.20	0.22	ns, min

IOB Input Switching Characteristics

Input delays associated with the pad are specified for LVCMOS 2.5V levels. For other standards, adjust the delays with the values shown in IOB Input Switching Characteristics Standard Adjustments.

Table 27: **IOB Input Switching Characteristics**

			Speed Grade			
Description	**Symbol**	**Device**	**-7**	**-6**	**-5**	**Units**
Propagation Delays						
Pad to I output, no delay	T_{IOPI}	All			0.75	ns, max
Pad to I output, with delay	T_{IOPID}	XC2VP2			1.99	ns, max
		XC2VP4			1.99	ns, max
		XC2VP7			1.99	ns, max
		XC2VP20			2.40	ns, max
		XC2VP30				ns, max
		XC2VP40				ns, max
		XC2VP50			3.04	ns, max
		XC2VP70				ns, max
		XC2VP100				ns, max
		XC2VP125				ns, max
Propagation Delays						
Pad to output IQ via transparent latch, no delay	T_{IOPLI}	All			0.96	ns, max
Pad to output IQ via transparent latch, with delay	T_{IOPLID}	XC2VP2			3.76	ns, max
		XC2VP4			3.76	ns, max
		XC2VP7			3.76	ns, max
		XC2VP20			4.21	ns, max
		XC2VP30				
		XC2VP40				
		XC2VP50			5.17	ns, max
		XC2VP70				
		XC2VP100				
		XC2VP125				
Clock CLK to output IQ	T_{IOCKIQ}	All			0.71	ns, max
Setup and Hold Times With Respect to Clock at IOB Input Register						
Pad, no delay	T_{IOPICK}/T_{IOICKP}	All			0.74/–0.40	ns, min

Table 27: **IOB Input Switching Characteristics *(Continued)***

			Speed Grade			
Description	**Symbol**	**Device**	**-7**	**-6**	**-5**	**Units**
Pad, with delay	$T_{IOPICKD}/T_{IOICKPD}$	XC2VP2			4.07/–2.73	ns, max
		XC2VP4			4.07/–2.73	ns, max
		XC2VP7			4.07/–2.73	ns, max
		XC2VP20			4.47/–3.01	ns, max
		XC2VP30				
		XC2VP40				
		XC2VP50			5.12/–3.46	ns, max
		XC2VP70				
		XC2VP100				
		XC2VP125				
ICE input	$T_{IOICECK}/T_{IOCKICE}$	All			0.39/ 0.01	ns, min
SR input (IFF, synchronous)	$T_{IOSRCKI}$	All			0.77	ns, min
Set/Reset Delays						
SR input to IQ (asynchronous)	T_{IOSRIQ}	All			1.58	ns, max
GSR to output IQ	T_{GSRQ}	All			10.00	ns, max

Notes:
1. Input timing for LVCMOS25 is measured at 1.25V. For other I/O standards, see Table 31.

IOB Input Switching Characteristics Standard Adjustments

Table 28: **IOB Input Switching Characteristics Standard Adjustments**

			Speed Grade			
Description	**Symbol**	**Standard**	**-7**	**-6**	**-5**	**Units**
Data Input Delay Adjustments						
Standard-specific data input delay adjustments	T_{ILVTTL}	LVTTL				ns
	$T_{ILVCMOS33}$	LVCMOS				ns
	$T_{ILVCMOS25}$	LVCMOS25			0.00	ns
	$T_{ILVCMOS18}$	LVCMOS18			0.26	ns
	$T_{ILVCMOS15}$	LVCMOS15			0.43	ns
	T_{ILVDS_25}	LVDS_25			0.35	ns
	T_{IPCI33_3}	PCI, 33 MHz, 3.3V			0.15	ns
	T_{IPCI66_3}	PCI, 66 MHz, 3.3V			0.15	ns
	T_{IPCIX}	PCI-X				ns
	T_{IGTL}	GTL			0.68	ns
	T_{IGTLP}	GTLP			0.66	ns
	T_{IHSTL_I}	HSTL_I			0.72	ns
	T_{IHSTL_II}	HSTL_II			0.69	ns
	T_{IHSTL_III}	HSTL_III			0.70	ns
	T_{IHSTL_IV}	HSTL_IV			0.71	ns
	$T_{IHSTL\_I\_18}$	HSTL_I_18			0.72	ns
	$T_{IHSTL\_II\_18}$	HSTL_II_18			0.69	ns
	$T_{IHSTL\_III\_18}$	HSTL_III_18			0.70	ns
	$T_{IHSTL\_IV\_18}$	HSTL_IV_18			0.71	ns
	T_{ISSTL2_I}	SSTL2_I			0.56	ns
	T_{ISSTL2_II}	SSTL2_II			0.65	ns
	$T_{ILVDCI33}$	LVDCI_33			-0.05	ns
	$T_{ILVDCI25}$	LVDCI_25			0.00	ns
	$T_{ILVDCI18}$	LVDCI_18			0.08	ns
	$T_{ILVDCI15}$	LVDCI_15			0.15	ns
	$T_{ILVDCI\_DV2\_25}$	LVDCI_DV2_25			0.00	ns
	$T_{ILVDCI\_DV2\_18}$	LVDCI_DV2_18			0.08	ns
	$T_{ILVDCI\_DV2\_15}$	LVDCI_DV2_15			0.15	ns
	T_{IGTL_DCI}	GTL_DCI			0.54	ns
	T_{IGTLP_DCI}	GTLP_DCI			0.30	ns
	$T_{IHSTL\_I\_DCI}$	HSTL_I_DCI			0.30	ns
	$T_{IHSTL\_II\_DCI}$	HSTL_II_DCI			0.30	ns
	$T_{IHSTL\_III\_DCI}$	HSTL_III_DCI			0.30	ns
	$T_{IHSTL\_IV\_DCI}$	HSTL_IV_DCI			0.30	ns
	$T_{IHSTL\_I\_DCI\_18}$	HSTL_I_DCI_18			0.30	ns

Table 28: **IOB Input Switching Characteristics Standard Adjustments *(Continued)***

			Speed Grade			
Description	**Symbol**	**Standard**	**-7**	**-6**	**-5**	**Units**
Standard-specific data input delay adjustments *(continued)*	$T_{IHSTL\_II\_DCI\_18}$	HSTL_II_DCI_18			0.30	ns
	$T_{IHSTL\_III\_DCI\_18}$	HSTL_III_DCI_18			0.30	ns
	$T_{IHSTL\_IV\_DCI\_18}$	HSTL_IV_DCI_18			0.30	ns
	$T_{ISSTL2\_I\_DCI}$	SSTL2_I_DCI			0.19	ns
	$T_{ISSTL2\_II\_DCI}$	SSTL2_II_DCI			0.19	ns
	$T_{ILVDSEXT\_25}$	LVDSEXT_25			0.35	ns
	T_{ILDT_25}	LDT_25			0.34	ns
	T_{IBLVDS_25}	BLVDS_25			0.00	ns
	T_{IULVDS_25}	ULVDS_25			0.34	ns
	$T_{ILVDS\_25\_DCI}$	LVDS_25_DCI			0.19	ns
	$T_{ILVDSEXT\_25\_DCI}$	LVDSEXT_25_DCI			0.35	ns
	$T_{ILVPECL\_25}$	LVPECL_25			0.76	ns
	$T_{ISSTL18\_I}$	SSTL18_I			0.56	ns
	$T_{ISSTL18\_II}$	SSTL18_II			0.65	ns
	$T_{ISSTL18\_I\_DCI}$	SSTL18_I_DCI			0.56	ns
	$T_{ISSTL18\_II\_DCI}$	SSTL18_II_DCI			0.65	ns

IOB Output Switching Characteristics

Output delays terminating at a pad are specified for LVCMOS25 with 12 mA drive and fast slew rate. For other standards, adjust the delays with the values shown in IOB Output Switching Characteristics Standard Adjustments.

Table 29: **IOB Output Switching Characteristics**

		Speed Grade			
Description	**Symbol**	**-7**	**-6**	**-5**	**Units**
Propagation Delays					
O input to Pad	T_{IOOP}			3.42	ns, max
O input to Pad via transparent latch	T_{IOOLP}			3.55	ns, max
3-State Delays					
T input to Pad high-impedance(2)	T_{IOTHZ}			0.88	ns, max
T input to valid data on Pad	T_{IOTP}			3.45	ns, max
T input to Pad high-impedance via transparent latch(2)	$T_{IOTLPHZ}$			0.90	ns, max
T input to valid data on Pad via transparent latch	$T_{IOTLPON}$			3.49	ns, max
GTS to Pad high-impedance(2)	T_{GTS}			7.78	ns, max
Sequential Delays					
Clock CLK to Pad	T_{IOCKP}			3.59	ns, max
Clock CLK to Pad high-impedance (synchronous)(2)	T_{IOCKHZ}			1.28	ns, max
Clock CLK to valid data on Pad (synchronous)	T_{IOCKON}			3.85	ns, max
Setup and Hold Times Before/After Clock CLK					
O input	T_{IOOCK}/T_{IOCKO}			0.18/ 0.12	ns, min
OCE input	$T_{IOOCECK}/T_{IOCKOCE}$			0.39/ 0.01	ns, min
SR input (OFF)	$T_{IOSRCKO}/T_{IOCKOSR}$			0.77/ 0.00	ns, min
3–State Setup Times, T input	T_{IOTCK}/T_{IOCKT}			0.18/ 0.12	ns, min
3-State Setup Times, TCE input	$T_{IOTCECK}/T_{IOCKTCE}$			0.39/ 0.01	ns, min
3-State Setup Times, SR input (TFF)	$T_{IOSRCKT}/T_{IOCKTSR}$			0.77/ 0.00	ns, min
Set/Reset Delays					
SR input to Pad (asynchronous)	T_{IOSRP}			4.57	ns, max
SR input to Pad high-impedance (asynchronous)(2)	T_{IOSRHZ}			1.93	ns, max
SR input to valid data on Pad (asynchronous)	T_{IOSRON}			4.51	ns, max
GSR to Pad	T_{IOGSRQ}			7.43	ns, max

Notes:
1. A Zero “0” Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed “best-case”, but if a “0” is listed, there is no positive hold time.
2. The 3-state turn-off delays should not be adjusted.

IOB Output Switching Characteristics Standard Adjustments

Output delays terminating at a pad are specified for LVCMOS25 with 12 mA drive and fast slew rate. For other standards, adjust the delays by the values shown.

Table 30: **IOB Output Switching Characteristics Standard Adjustments**

Output Delay Adjustments			Speed Grade			
Description	**Symbol**	**Standard**	**-7**	**-6**	**-5**	**Units**
Standard-specific adjustments for output delays terminating at pads (based on standard capacitive load, Csl)	T_{OLVDS_25}	LVDS			–0.77	ns
	$T_{OLVDSEXT\_25}$	LVDSEXT			–0.64	ns
	T_{OLDT_25}	LDT			–0.63	ns
	T_{OBLVDS_25}	BLVDS			0.00	ns
	T_{OULVDS_25}	ULVDS			–0.63	ns
	T_{OPCI33_3}	PCI, 33 MHz, 3.3V			0.28	ns
	T_{OPCI66_3}	PCI, 66 MHz, 3.3V			0.31	ns
	T_{OPCIX}	PCI-X				ns
	T_{OGTL}	GTL			1.01	ns
	T_{OGTLP}	GTLP			3.38	ns
	T_{OHSTL_I}	HSTL_I			0.01	ns
	T_{OHSTL_II}	HSTL_II			–0.36	ns
	T_{OHSTL_IIII}	HSTL_III			–0.33	ns
	T_{OHSTL_IV}	HSTL_IV			0.89	ns
	$T_{OHSTL\_I\_18}$	HSTL_I_18			–0.09	ns
	$T_{OHSTL\_II\_18}$	HSTL_II_18			–0.47	ns
	$T_{OHSTL\_IIII\_18}$	HSTL_III_18			–0.36	ns
	$T_{OHSTL\_IV\_18}$	HSTL_IV_18			0.86	ns
	T_{OSSTL2_I}	SSTL2_I			0.05	ns
	T_{OSSTL2_II}	SSTL2_II			–0.66	ns
	T_{OLVTTL}	LVTTL				
	$T_{OLVCMOS33\_S2}$	LVCMOS33, Slow, 2 mA				
	$T_{OLVCMOS33\_S4}$	4 mA				
	$T_{OLVCMOS33\_S6}$	6 mA				
	$T_{OLVCMOS33\_S8}$	8 mA				
	$T_{OLVCMOS33\_S12}$	12 mA				
	$T_{OLVCMOS33\_S16}$	16 mA				
	$T_{OLVCMOS33\_S24}$	24 mA				
	$T_{OLVCMOS33\_F2}$	LVCMOS33, Fast, 2 mA				
	$T_{OLVCMOS33\_F4}$	4 mA				
	$T_{OLVCMOS33\_F6}$	6 mA				
	$T_{OLVCMOS33\_F8}$	8 mA				
	$T_{OLVCMOS33\_F12}$	12 mA				
	$T_{OLVCMOS33\_F16}$	16 mA				
	$T_{OLVCMOS33\_F24}$	24 mA				

Table 30: **IOB Output Switching Characteristics Standard Adjustments *(Continued)***

Output Delay Adjustments			Speed Grade			
Description	**Symbol**	**Standard**	**-7**	**-6**	**-5**	**Units**
Standard-specific adjustments for output delays terminating at pads (based on standard capacitive load, Csl)	$T_{OLVCMOS25\_S2}$	LVCMOS25, Slow, 2 mA			12.96	ns
	$T_{OLVCMOS25\_S4}$	4 mA			6.42	ns
	$T_{OLVCMOS25\_S6}$	6 mA			4.17	ns
	$T_{OLVCMOS25\_S8}$	8 mA			2.61	ns
	$T_{OLVCMOS25\_S12}$	12 mA			1.42	ns
	$T_{OLVCMOS25\_S16}$	16 mA			0.83	ns
	$T_{OLVCMOS25\_S24}$	24 mA			0.19	ns
	$T_{OLVCMOS25\_F2}$	LVCMOS25, Fast, 2 mA			11.84	ns
	$T_{OLVCMOS25\_F4}$	4 mA			4.74	ns
	$T_{OLVCMOS25\_F6}$	6 mA			2.85	ns
	$T_{OLVCMOS25\_F8}$	8 mA			1.22	ns
	$T_{OLVCMOS25\_F12}$	12 mA			0.00	ns
	$T_{OLVCMOS25\_F16}$	16 mA			–0.17	ns
	$T_{OLVCMOS25\_F24}$	24 mA			–0.44	ns
	$T_{OLVCMOS18\_S2}$	LVCMOS18, Slow, 2 mA			10.06	ns
	$T_{OLVCMOS18\_S4}$	4 mA			6.26	ns
	$T_{OLVCMOS18\_S6}$	6 mA			3.85	ns
	$T_{OLVCMOS18\_S8}$	8 mA			3.94	ns
	$T_{OLVCMOS18\_S12}$	12 mA			3.16	ns
	$T_{OLVCMOS18\_S16}$	16 mA			1.21	ns
	$T_{OLVCMOS18\_F2}$	LVCMOS18, Fast, 2 mA			8.83	ns
	$T_{OLVCMOS18\_F4}$	4 mA			3.46	ns
	$T_{OLVCMOS18\_F6}$	6 mA			1.69	ns
	$T_{OLVCMOS18\_F8}$	8 mA			1.24	ns
	$T_{OLVCMOS18\_F12}$	12 mA			0.49	ns
	$T_{OLVCMOS18\_F16}$	16 mA			–0.03	ns
	$T_{OLVCMOS15\_S2}$	LVCMOS15, Slow, 2 mA			12.76	ns
	$T_{OLVCMOS15\_S4}$	4 mA			8.73	ns
	$T_{OLVCMOS15\_S6}$	6 mA			5.66	ns
	$T_{OLVCMOS15\_S8}$	8 mA			4.85	ns
	$T_{OLVCMOS15\_S12}$	12 mA			2.14	ns
	$T_{OLVCMOS15\_S16}$	16 mA			1.99	ns
	$T_{OLVCMOS15\_F2}$	LVCMOS15, Fast, 2 mA			7.84	ns
	$T_{OLVCMOS15\_F4}$	4 mA			4.10	ns
	$T_{OLVCMOS15\_F6}$	6 mA			1.34	ns
	$T_{OLVCMOS15\_F8}$	8 mA			2.32	ns
	$T_{OLVCMOS15\_F12}$	12 mA			0.12	ns
	$T_{OLVCMOS15\_F16}$	16 mA			0.18	ns

Table 30: **IOB Output Switching Characteristics Standard Adjustments *(Continued)***

Output Delay Adjustments			Speed Grade			
Description	**Symbol**	**Standard**	**-7**	**-6**	**-5**	**Units**
Standard-specific adjustments for output delays terminating at pads (based on standard capacitive load, Csl)	$T_{OLVDCI33}$	LVDCI_33			1.89	ns
	$T_{OLVDCI25}$	LVDCI_25			1.72	ns
	$T_{OLVDCI18}$	LVDCI_18			2.61	ns
	$T_{OLVDCI15}$	LVDCI_15			3.58	ns
	$T_{OLVDCI\_DV2\_25}$	LVDCI_DV2_25			–0.02	ns
	$T_{OLVDCI\_DV2\_18}$	LVDCI_DV2_18			0.43	ns
	$T_{OLVDCI\_DV2\_15}$	LVDCI_DV2_15			1.00	ns
	T_{OGTL_DCI}	GTL_DCI			1.10	ns
	T_{OGTLP_DCI}	GTLP_DCI			3.23	ns
	$T_{OHSTL\_I\_DCI}$	HSTL_I_DCI			0.00	ns
	$T_{OHSTL\_II\_DCI}$	HSTL_II_DCI			–0.22	ns
	$T_{OHSTL\_III\_DCI}$	HSTL_III_DCI			–0.32	ns
	$T_{OHSTL\_IV\_DCI}$	HSTL_IV_DCI			1.93	ns
	$T_{OHSTL\_I\_DCI\_18}$	HSTL_I_DCI_18			–0.13	ns
	$T_{OHSTL\_II\_DCI\_18}$	HSTL_II_DCI_18			–0.35	ns
	$T_{OHSTL\_III\_DCI\_18}$	HSTL_III_DCI_18			–0.40	ns
	$T_{OHSTL\_IV\_DCI\_18}$	HSTL_IV_DCI_18			1.30	ns
	$T_{OSSTL2\_I\_DCI}$	SSTL2_I_DCI			–0.15	ns
	$T_{OSSTL2\_II\_DCI}$	SSTL2_II_DCI			–0.38	ns
	$T_{OLVPECL\_25}$	LVPECL_25			0.21	ns
	$T_{OSSTL18\_I}$	SSTL18_I			0.04	ns
	$T_{OSSTL18\_II}$	SSTL18_II			–0.66	ns
	$T_{OSSTL18\_I\_DCI}$	SSTL18_I_DCI			–0.15	ns
	$T_{OSSTL18\_II\_DCI}$	SSTL18_II_DCI			–0.39	ns

Table 31: **Delay Measurement Methodology**

Standard	V_L (1)	V_H (1)	Meas. Point	V_{REF} (Typ) (2)
LVTTL	0	3.3	1.65	–
LVCMOS33	0	3.3	1.65	–
LVCMOS25	0	2.5	1.25	–
LVCMOS18	0	1.8	0.9	–
LVCMOS15	0	1.5	0.75	–
PCI33_3	Per PCI Specification			–
PCI66_3	Per PCI Specification			–
PCI-X	Per PCI-X Specification			–
GTL	V_{REF} – 0.2	V_{REF} + 0.2	V_{REF}	0.80
GTLP	V_{REF} – 0.2	V_{REF} + 0.2	V_{REF}	1.0
HSTL Class I	V_{REF} – 0.5	V_{REF} + 0.5	V_{REF}	0.75
HSTL Class II	V_{REF} – 0.5	V_{REF} + 0.5	V_{REF}	0.75
HSTL Class III	V_{REF} – 0.5	V_{REF} + 0.5	V_{REF}	0.90
HSTL Class IV	V_{REF} – 0.5	V_{REF} + 0.5	V_{REF}	0.90
HSTL Class I (1.8V)	V_{REF} – 0.5	V_{REF} + 0.5	V_{REF}	1.08
HSTL Class II (1.8V)	V_{REF} – 0.5	V_{REF} + 0.5	V_{REF}	1.08
HSTL Class III (1.8V)	V_{REF} – 0.5	V_{REF} + 0.5	V_{REF}	1.08
HSTL Class IV (1.8V)	V_{REF} – 0.5	V_{REF} + 0.5	V_{REF}	1.08
SSTL2 I & II	V_{REF} – 0.75	V_{REF} + 0.75	V_{REF}	1.25
SSTL18 I & II	V_{REF} – 0.5	V_{REF} + 0.5	V_{REF}	0.9
LVDS_25	1.2 – 0.125	1.2 + 0.125	1.2	
LVDSEXT_25	1.2 – 0.125	1.2 + 0.125	1.2	
ULVDS_25	0.6 – 0.125	0.6 + 0.125	0.6	
LDT_25	0.6 – 0.125	0.6 + 0.125	0.6	

Notes:
1. Input waveform switches between V_L and V_H.
2. Measurements are made at V_{REF} (Typ), Maximum, and Minimum. Worst-case values are reported.

Table 32: **Standard Capacitive Loads**

Standard	Csl (pF)
LVTTL	0
LVCMOS33	0
LVCMOS25	0
LVCMOS18	0
LVCMOS15	0
PCI 33MHZ 3.3V	10
PCI 66 MHz 3.3V	10
PCI-X	10
GTL	0
GTLP	0
HSTL Class I (1.5V and 1.8V)	0
HSTL Class II (1.5V and 1.8V	0
HSTL Class III (1.5V and 1.8V)	0
HSTL Class IV (1.5V and 1.8V)	0
SSTL2 Class I	0
SSTL2 Class II	0
SSTL18 Class I	0
SSTL18 Class II	0

Notes:

1. I/O parameter measurements are made with the capacitance values shown above.
2. I/O standard measurements are reflected in the IBIS model information except where the IBIS format precludes it.
3. Use of IBIS models results in a more accurate prediction of the propagation delay:
   a. Model the output in an IBIS simulation into the standard capacitive load.
   b. Record the relative time to the V_{OH} or V_{OL} transition of interest.
   c. Remove the capacitance, and model the actual PCB traces (transmission lines) and actual loads from the appropriate IBIS models for driven devices.
   d. Record the results from the new simulation.
   e. Compare with the capacitance simulation. The increase or decrease in delay from the capacitive load delay simulation should be added or subtracted from the value above to predict the actual delay.

CLB Switching Characteristics

Delays originating at F/G inputs vary slightly according to the input used (see Figure 24 in **Data Sheet Module 2**). The values listed below are worst-case. Precise values are provided by the timing analyzer.

Table 33: **CLB Switching Characteristics**

		Speed Grade			
Description	**Symbol**	**-7**	**-6**	**-5**	**Units**
Combinatorial Delays					
4-input function: F/G inputs to X/Y outputs	T_{ILO}	0.29	0.33	0.37	ns, max
5-input function: F/G inputs to F5 output	T_{IF5}	0.62	0.70	0.77	ns, max
5-input function: F/G inputs to X output	T_{IF5X}	0.59	0.67	0.74	ns, max
FXINA or FXINB inputs to Y output via MUXFX	T_{IFXY}	0.30	0.34	0.38	ns, max
FXINA input to FX output via MUXFX	T_{INAFX}	0.29	0.33	0.36	ns, max
FXINB input to FX output via MUXFX	T_{INBFX}	0.29	0.33	0.36	ns, max
SOPIN input to SOPOUT output via ORCY	T_{SOPSOP}	0.22	0.25	0.27	ns, max
Incremental delay routing through transparent latch to XQ/YQ outputs	T_{IFNCTL}	0.28	0.32	0.35	ns, max
Sequential Delays					
FF Clock CLK to XQ/YQ outputs	T_{CKO}	0.32	0.36	0.40	ns, max
Latch Clock CLK to XQ/YQ outputs	T_{CKLO}	0.58	0.66	0.73	ns, max
Setup and Hold Times Before/After Clock CLK					
BX/BY inputs	T_{DICK}/T_{CKDI}	0.23/–0.06	0.26/–0.07	0.29/–0.08	ns, min
DY inputs	T_{DYCK}/T_{CKDY}	0.01/0.09	0.01/0.11	0.01/ 0.12	ns, min
DX inputs	T_{DXCK}/T_{CKDX}	0.01/0.09	0.01/0.11	0.01/ 0.12	ns, min
CE input	T_{CECK}/T_{CKCE}	0.31/0.01	0.35/0.01	0.39/ 0.01	ns, min
SR/BY inputs (synchronous)	T_{RCK}/T_{CKR}	0.69/–0.01	0.79/–0.01	0.87/–0.01	ns, min
Clock CLK					
Minimum Pulse Width, High	T_{CH}	0.37	0.42	0.46	ns, min
Minimum Pulse Width, Low	T_{CL}	0.37	0.42	0.46	ns, min
Set/Reset					
Minimum Pulse Width, SR/BY inputs	TRPW	0.37	0.42	0.46	ns, min
Delay from SR/BY inputs to XQ/YQ outputs (asynchronous)	TRQ	1.16	1.32	1.45	ns, max
Toggle Frequency (MHz) (for export control)	FTOG	1350	1200	1050	MHz

Notes:
1. A Zero “0” Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed “best-case”, but if a “0” is listed, there is no positive hold time.

CLB Distributed RAM Switching Characteristics

Table 34: **CLB Distributed RAM Switching Characteristics**

Description	Symbol	Speed Grade			Units
		-7	-6	-5	
Sequential Delays					
Clock CLK to X/Y outputs (WE active) in 16 x 1 mode	$T_{SHCKO16}$	1.30	1.48	1.63	ns, max
Clock CLK to X/Y outputs (WE active) in 32 x 1 mode	$T_{SHCKO32}$	1.56	1.78	1.96	ns, max
Clock CLK to F5 output	$T_{SHCKOF5}$	1.56	1.78	1.96	ns, max
Setup and Hold Times Before/After Clock CLK					
BX/BY data inputs (DIN)	T_{DS}/T_{DH}	0.35/–0.03	0.39/–0.04	0.43/–0.04	ns, min
F/G address inputs	T_{AS}/T_{AH}	0.42/0.00	0.47/0.00	0.52/ 0.00	ns, min
CE input (WE)	T_{WES}/T_{WEH}	0.21/0.04	0.24/0.05	0.26/ 0.05	ns, min
Clock CLK					
Minimum Pulse Width, High	T_{WPH}	0.63	0.72	0.79	ns, min
Minimum Pulse Width, Low	T_{WPL}	0.63	0.72	0.79	ns, min
Minimum clock period to meet address write cycle time	T_{WC}	1.25	1.44	1.58	ns, min

Notes:
1. A Zero “0” Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed “best-case”, but if a “0” is listed, there is no positive hold time.

CLB Shift Register Switching Characteristics

Table 35: **CLB Shift Register Switching Characteristics**

Description	Symbol	Speed Grade			Units
		-7	-6	-5	
Sequential Delays					
Clock CLK to X/Y outputs	T_{REG}	2.61	2.97	3.27	ns, max
Clock CLK to X/Y outputs	T_{REG32}	2.87	3.27	3.59	ns, max
Clock CLK to XB output via MC15 LUT output	T_{REGXB}	2.62	2.99	3.29	ns, max
Clock CLK to YB output via MC15 LUT output	T_{REGYB}	2.60	2.97	3.26	ns, max
Clock CLK to Shiftout	T_{CKSH}	2.53	2.88	3.17	ns, max
Clock CLK to F5 output	T_{REGF5}	2.86	3.27	3.59	ns, max
Setup and Hold Times Before/After Clock CLK					
BX/BY data inputs (DIN)	T_{SRLDS}/T_{SRLDH}	0.84/–0.15	0.96/–0.17	1.06/–0.19	ns, min
CE input (WS)	T_{WSS}/T_{WSH}	0.31/0.01	0.35/0.01	0.39/ 0.01	ns, min
Clock CLK					
Minimum Pulse Width, High	T_{SRPH}	0.63	0.72	0.79	ns, min
Minimum Pulse Width, Low	T_{SRPL}	0.63	0.72	0.79	ns, min

Notes:
1. A Zero “0” Hold Time listing indicates no hold time or a negative hold time. Negative values cannot be guaranteed “best-case”, but if a “0” is listed, there is no positive hold time.

Multiplier Switching Characteristics

Table 36: **Multiplier Switching Characteristics**

Description	Symbol	Speed Grade			Units
		-7	-6	-5	
Propagation Delay to Output Pin					
Input to Pin35	T_{MULT_P35}	4.04	4.66	5.14	ns, max
Input to Pin34	T_{MULT_P34}	3.96	4.57	5.03	ns, max
Input to Pin33	T_{MULT_P33}	3.88	4.47	4.93	ns, max
Input to Pin32	T_{MULT_P32}	3.79	4.37	4.82	ns, max
Input to Pin31	T_{MULT_P31}	3.71	4.28	4.71	ns, max
Input to Pin30	T_{MULT_P30}	3.62	4.18	4.61	ns, max
Input to Pin29	T_{MULT_P29}	3.54	4.08	4.50	ns, max
Input to Pin28	T_{MULT_P28}	3.46	3.99	4.39	ns, max
Input to Pin27	T_{MULT_P27}	3.37	3.89	4.28	ns, max
Input to Pin26	T_{MULT_P26}	3.29	3.79	4.18	ns, max
Input to Pin25	T_{MULT_P25}	3.20	3.69	4.07	ns, max
Input to Pin24	T_{MULT_P24}	3.12	3.60	3.96	ns, max
Input to Pin23	T_{MULT_P23}	3.04	3.50	3.86	ns, max
Input to Pin22	T_{MULT_P22}	2.95	3.40	3.75	ns, max
Input to Pin21	T_{MULT_P21}	2.87	3.31	3.64	ns, max
Input to Pin20	T_{MULT_P20}	2.78	3.21	3.54	ns, max
Input to Pin19	T_{MULT_P19}	2.70	3.11	3.43	ns, max
Input to Pin18	T_{MULT_P18}	2.62	3.02	3.32	ns, max
Input to Pin17	T_{MULT_P17}	2.53	2.92	3.21	ns, max
Input to Pin16	T_{MULT_P16}	2.45	2.82	3.11	ns, max
Input to Pin15	T_{MULT_P15}	2.36	2.72	3.00	ns, max
Input to Pin14	T_{MULT_P14}	2.28	2.63	2.89	ns, max
Input to Pin13	T_{MULT_P13}	2.20	2.53	2.79	ns, max
Input to Pin12	T_{MULT_P12}	2.11	2.43	2.68	ns, max
Input to Pin11	T_{MULT_P11}	2.03	2.34	2.57	ns, max
Input to Pin10	T_{MULT_P10}	1.94	2.24	2.47	ns, max
Input to Pin9	T_{MULT_P9}	1.86	2.14	2.36	ns, max
Input to Pin8	T_{MULT_P8}	1.78	2.05	2.25	ns, max
Input to Pin7	T_{MULT_P7}	1.69	1.95	2.14	ns, max
Input to Pin6	T_{MULT_P6}	1.61	1.85	2.04	ns, max
Input to Pin5	T_{MULT_P5}	1.52	1.75	1.93	ns, max
Input to Pin4	T_{MULT_P4}	1.44	1.66	1.82	ns, max
Input to Pin3	T_{MULT_P3}	1.36	1.56	1.72	ns, max
Input to Pin2	T_{MULT_P2}	1.27	1.46	1.61	ns, max
Input to Pin1	T_{MULT_P1}	1.19	1.37	1.50	ns, max
Input to Pin0	T_{MULT_P0}	1.10	1.27	1.40	ns, max

Table 37: **Pipelined Multiplier Switching Characteristics**

Description	Symbol	Speed Grade			Units
		-7	-6	-5	
Setup and Hold Times Before/After Clock					
Data Inputs	$T_{MULIDCK}/T_{MULCKID}$	2.61/0.00	3.00/0.00	3.45/ 0.00	ns, max
Clock Enable	$T_{MULIDCK\_CE}/T_{MULCKID\_CE}$	0.63/0.00	0.72/0.00	0.80/ 0.00	ns, max
Reset	$T_{MULIDCK\_RST}/T_{MULCKID\_RST}$	0.63/0.00	0.72/0.00	0.80/ 0.00	ns, max
Clock to Output Pin					
Clock to Pin35	T_{MULTCK_P35}	2.64	3.05	3.36	ns, max
Clock to Pin34	T_{MULTCK_P34}	2.56	2.95	3.25	ns, max
Clock to Pin33	T_{MULTCK_P33}	2.48	2.85	3.14	ns, max
Clock to Pin32	T_{MULTCK_P32}	2.39	2.76	3.04	ns, max
Clock to Pin31	T_{MULTCK_P31}	2.31	2.66	2.93	ns, max
Clock to Pin30	T_{MULTCK_P30}	2.22	2.56	2.82	ns, max
Clock to Pin29	T_{MULTCK_P29}	2.14	2.47	2.72	ns, max
Clock to Pin28	T_{MULTCK_P28}	2.06	2.37	2.61	ns, max
Clock to Pin27	T_{MULTCK_P27}	1.97	2.27	2.50	ns, max
Clock to Pin26	T_{MULTCK_P26}	1.89	2.17	2.40	ns, max
Clock to Pin25	T_{MULTCK_P25}	1.80	2.08	2.29	ns, max
Clock to Pin24	T_{MULTCK_P24}	1.72	1.98	2.18	ns, max
Clock to Pin23	T_{MULTCK_P23}	1.64	1.88	2.07	ns, max
Clock to Pin22	T_{MULTCK_P22}	1.55	1.79	1.97	ns, max
Clock to Pin21	T_{MULTCK_P21}	1.47	1.69	1.86	ns, max
Clock to Pin20	T_{MULTCK_P20}	1.38	1.59	1.75	ns, max
Clock to Pin19	T_{MULTCK_P19}	1.30	1.50	1.65	ns, max
Clock to Pin18	T_{MULTCK_P18}	1.22	1.40	1.54	ns, max
Clock to Pin17	T_{MULTCK_P17}	1.13	1.30	1.43	ns, max
Clock to Pin16	T_{MULTCK_P16}	1.05	1.20	1.33	ns, max
Clock to Pin15	T_{MULTCK_P15}	0.96	1.11	1.22	ns, max
Clock to Pin14	T_{MULTCK_P14}	0.88	1.01	1.11	ns, max
Clock to Pin13	T_{MULTCK_P13}	0.80	0.91	1.00	ns, max
Clock to Pin12	T_{MULTCK_P12}	0.80	0.91	1.00	ns, max
Clock to Pin11	T_{MULTCK_P11}	0.80	0.91	1.00	ns, max
Clock to Pin10	T_{MULTCK_P10}	0.80	0.91	1.00	ns, max
Clock to Pin9	T_{MULTCK_P9}	0.80	0.91	1.00	ns, max
Clock to Pin8	T_{MULTCK_P8}	0.80	0.91	1.00	ns, max
Clock to Pin7	T_{MULTCK_P7}	0.80	0.91	1.00	ns, max
Clock to Pin6	T_{MULTCK_P6}	0.80	0.91	1.00	ns, max
Clock to Pin5	T_{MULTCK_P5}	0.80	0.91	1.00	ns, max
Clock to Pin4	T_{MULTCK_P4}	0.80	0.91	1.00	ns, max
Clock to Pin3	T_{MULTCK_P3}	0.80	0.91	1.00	ns, max
Clock to Pin2	T_{MULTCK_P2}	0.80	0.91	1.00	ns, max
Clock to Pin1	T_{MULTCK_P1}	0.80	0.91	1.00	ns, max
Clock to Pin0	T_{MULTCK_P0}	0.80	0.91	1.00	ns, max

Block SelectRAM+ Switching Characteristics

Table 38: **Block SelectRAM+ Switching Characteristics**

Description	Symbol	Speed Grade			Units
		-7	-6	-5	
Sequential Delays					
Clock CLK to DOUT output	T_{BCKO}	1.80	2.06	2.26	ns, max
Setup and Hold Times Before Clock CLK					
ADDR inputs	T_{BACK}/T_{BCKA}	0.28/0.00	0.32/0.00	0.35/ 0.00	ns, min
DIN inputs	T_{BDCK}/T_{BCKD}	0.28/0.00	0.32/0.00	0.35/ 0.00	ns, min
EN input	T_{BECK}/T_{BCKE}	0.91/–0.44	1.04/–0.50	1.15/–0.56	ns, min
RST input	T_{BRCK}/T_{BCKR}	1.25/–0.68	1.44/–0.78	1.58/–0.86	ns, min
WEN input	T_{BWCK}/T_{BCKW}	0.55/–0.18	0.63/–0.21	0.69/–0.24	ns, min
Clock CLK					
Minimum Pulse Width, High	T_{BPWH}	1.04	1.19	1.30	ns, min
Minimum Pulse Width, Low	T_{BPWL}	1.04	1.19	1.30	ns, min

Notes:
1. A Zero “0” Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed “best-case”, but if a “0” is listed, there is no positive hold time.

TBUF Switching Characteristics

Table 39: **TBUF Switching Characteristics**

Description	Symbol	Speed Grade			Units
		-7	-6	-5	
Combinatorial Delays					
IN input to OUT output	T_{IO}	1.09	1.24	1.37	ns, max
TRI input to OUT output high-impedance	T_{OFF}	0.47	0.54	0.60	ns, max
TRI input to valid data on OUT output	T_{ON}	0.47	0.54	0.60	ns, max

Configuration Timing

Configuration Memory Clearing Parameters

Power-up timing of configuration signals is shown in Figure 6; corresponding timing characteristics are listed in Table 40.

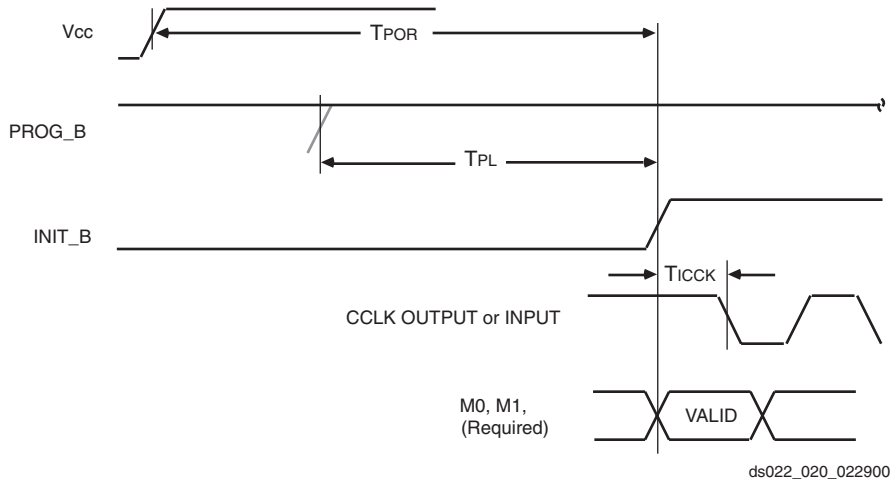

Figure 6: **Power-Up Timing Configuration Signals**

Table 40: **Power-Up Timing Characteristics**

Description	Symbol	Value	Units
Program Latency	T_{PL}		4 µs per frame max
Power-on-Reset	T_{POR}		ms, max
CCLK (output) Delay	T_{ICCK}		µs, min
			µs, max
Program Pulse Width	$T_{PROGRAM}$		ns, min

Master/Slave Serial Mode Parameters

For Slave configurations, a free running CCLK can be used, as shown in Figure 7.

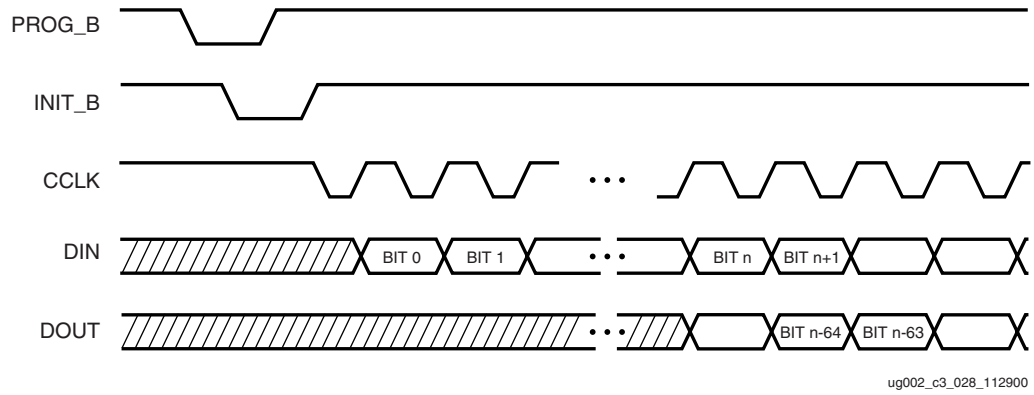

Figure 7: **Serial Configuration Clocking Sequence**

Table 41: **Master/Slave Serial Mode Programming Switching**

	Description	Symbol	Values	Units
CCLK	DIN setup/hold, slave mode	T_{DCC}/T_{CCD}	5.0/0.0	ns, min
	DIN setup/hold, master mode	T_{DSCK}/T_{SCKD}	5.0/0.0	ns, min
	DOUT	T_{CCO}	12.0	ns, max
	High time	T_{CCH}	5.0	ns, min
	Low time	T_{CCL}	5.0	ns, min
	Maximum Frequency	F_{CC_SERIAL}	66	MHz, max
	Frequency Tolerance, master mode with respect to nominal		+45% -30%	

Master/Slave SelectMAP Parameters

Figure 8 is a generic diagram for data loading using SelectMAP. For other data loading diagrams, refer to the *Virtex-II Pro Platform FPGA User Guide*.

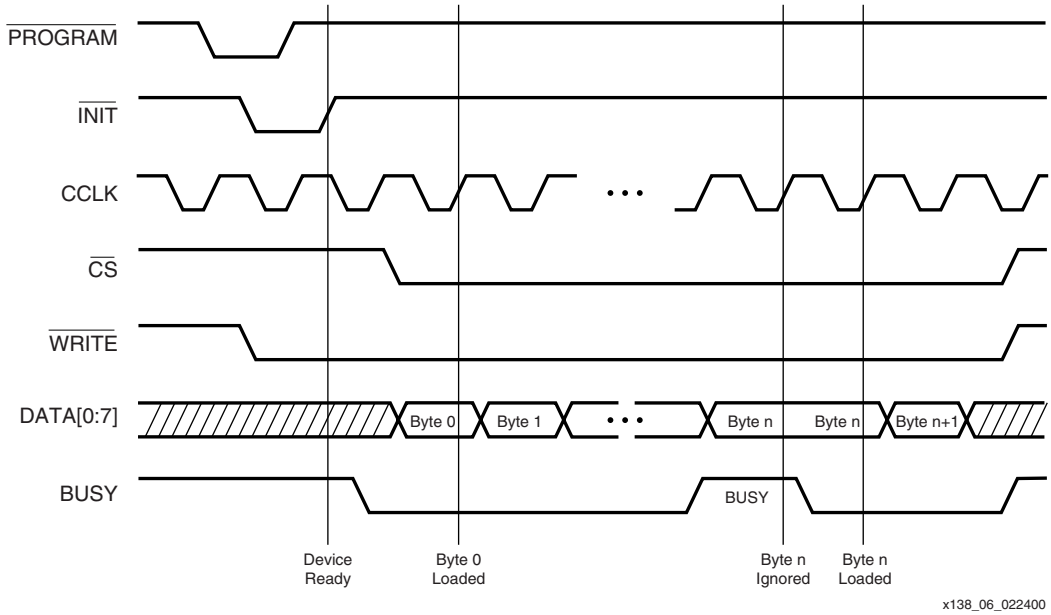

Figure 8: **Data Loading in SelectMAP**

Table 42: **SelectMAP Write Timing Characteristics**

	Description	Symbol	Value	Units
CCLK	D_{0-7} Setup/Hold	T_{SMDCC}/T_{SMCCD}	5.0/0.0	ns, min
	CS_B Setup/Hold	T_{SMCSCC}/T_{SMCCCS}	7.0/0.0	ns, min
	RDWR_B Setup/Hold	T_{SMCCW}/T_{SMWCC}	7.0/0.0	ns, min
	BUSY Propagation Delay	T_{SMCKBY}	12.0	ns, max
	Maximum Frequency	$F_{CC_}$SelectMAP	50	MHz, max
	Maximum Frequency with No Handshake	F_{CCNH}	50	MHz, max

JTAG Test Access Port Switching Characteristics

Characterization data for some of the most commonly requested timing parameters shown in Figure 9 is listed in Table 43.

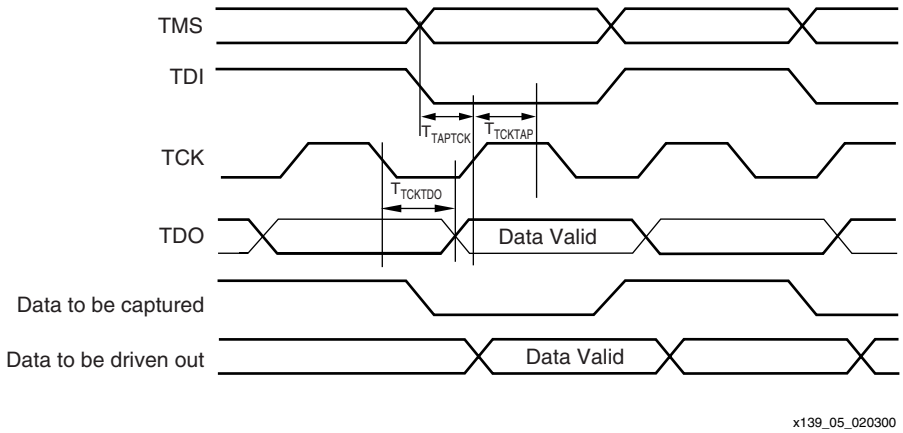

Figure 9: **Virtex-II Pro Boundary Scan Port Timing Waveforms**

Table 43: **Boundary-Scan Port Timing Specifications**

Symbol	Parameter	Value	Units
T_{TAPTCK}	TMS and TDI setup time before TCK	4.0	ns, min
T_{TCKTAP}	TMS and TDI hold times after TCK	2.0	ns, min
T_{TCKTDO}	TCK falling edge to TDO output valid	11.0	ns, min
F_{TCK}	Maximum TCK clock frequency	33.0	MHz, max

Virtex-II Pro Pin-to-Pin Output Parameter Guidelines

All devices are 100% functionally tested. Listed below are representative values for typical pin locations and normal clock loading. Values are expressed in nanoseconds unless otherwise noted.

Global Clock Input to Output Delay for LVCMOS25, 12 mA, Fast Slew Rate, *With* DCM

Table 44: **Global Clock Input to Output Delay for LVCMOS25, 12 mA, Fast Slew Rate, *With* DCM**

			Speed Grade			
Description	**Symbol**	**Device**	**-7**	**-6**	**-5**	**Units**
LVCMOS25 Global Clock Input to Output Delay using Output Flip-flop, 12 mA, Fast Slew Rate, *with* DCM. For data *output* with different standards, adjust the delays with the values shown in **IOB Output Switching Characteristics Standard Adjustments**, page 23.						
Global Clock and OFF with DCM	$T_{ICKOFDCM}$	XC2VP2				ns
		XC2VP4				ns
		XC2VP7				ns
		XC2VP20				ns
		XC2VP30				ns
		XC2VP40				ns
		XC2VP50				ns
		XC2VP70				ns
		XC2VP100				ns
		XC2VP125				ns

Notes:
1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. Output timing is measured at 50% V_{CC} threshold with 35 pF external capacitive load. For other I/O standards and different loads, see Table 31.
3. DCM output jitter is already included in the timing calculation.

Global Clock Input to Output Delay for LVCMOS25, 12 mA, Fast Slew Rate, *Without* DCM

Table 45: **Global Clock Input to Output Delay for LVCMOS25, 12 mA, Fast Slew Rate, *Without* DCM**

			Speed Grade			
Description	**Symbol**	**Device**	**-7**	**-6**	**-5**	**Units**
LVCMOS25 Global Clock Input to Output Delay using Output Flip-flop, 12 mA, Fast Slew Rate, *without* DCM. For data *output* with different standards, adjust the delays with the values shown in **IOB Output Switching Characteristics Standard Adjustments**, page 23.						
Global Clock and OFF without DCM	T_{ICKOF}	XC2VP2				ns
		XC2VP4				ns
		XC2VP7				ns
		XC2VP20				ns
		XC2VP30				ns
		XC2VP40				ns
		XC2VP50				ns
		XC2VP70				ns
		XC2VP100				ns
		XC2VP125				ns

Notes:
1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. Output timing is measured at 50% V_{CC} threshold with 35 pF external capacitive load. For other I/O standards and different loads, see Table 31.
3. DCM output jitter is already included in the timing calculation.

Virtex-II Pro Pin-to-Pin Input Parameter Guidelines

All devices are 100% functionally tested. Listed below are representative values for typical pin locations and normal clock loading. Values are expressed in nanoseconds unless otherwise noted

Global Clock Set-Up and Hold for LVCMOS25 Standard, *With* DCM

Table 46: **Global Clock Set-Up and Hold for LVCMOS25 Standard, *With* DCM**

			Speed Grade			
Description	**Symbol**	**Device**	**-7**	**-6**	**-5**	**Units**
Input Setup and Hold Time Relative to Global Clock Input Signal for LVCMOS25 Standard. For data input with different standards, adjust the setup time delay by the values shown in **IOB Input Switching Characteristics Standard Adjustments**, page 20.						
No Delay Global Clock and IFF with DCM	T_{PSDCM}/T_{PHDCM}	XC2VP2				ns
		XC2VP4				ns
		XC2VP7				ns
		XC2VP20				ns
		XC2VP30				ns
		XC2VP40				ns
		XC2VP50				ns
		XC2VP70				ns
		XC2VP100				ns
		XC2VP125				ns

Notes:
1. IFF = Input Flip-Flop or Latch
2. Setup time is measured relative to the Global Clock input signal with the fastest route and the lightest load. Hold time is measured relative to the Global Clock input signal with the slowest route and heaviest load.
3. DCM output jitter is already included in the timing calculation.

Global Clock Set-Up and Hold for LVCMOS25 Standard, *Without* DCM

Table 47: **Global Clock Set-Up and Hold for LVCMOS25 Standard, *Without* DCM**

			Speed Grade			
Description	**Symbol**	**Device**	**-7**	**-6**	**-5**	**Units**
Input Setup and Hold Time Relative to Global Clock Input Signal for LVCMOS25 Standard. For data input with different standards, adjust the setup time delay by the values shown in **IOB Input Switching Characteristics Standard Adjustments**, page 20.						
Full Delay Global Clock and IFF without DCM	T_{PSFD}/T_{PHFD}	XC2VP2				ns
		XC2VP4				ns
		XC2VP7				ns
		XC2VP20				ns
		XC2VP30				ns
		XC2VP40				ns
		XC2VP50				ns
		XC2VP70				ns
		XC2VP100				ns
		XC2VP125				ns

Notes:
1. IFF = Input Flip-Flop or Latch
2. Setup time is measured relative to the Global Clock input signal with the fastest route and the lightest load. Hold time is measured relative to the Global Clock input signal with the slowest route and heaviest load.
3. A Zero “0” Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed “best-case”, but if a “0” is listed, there is no positive hold time.

DCM Timing Parameters

All devices are 100% functionally tested. Because of the difficulty in directly measuring many internal timing parameters, those parameters are derived from benchmark timing patterns. The following guidelines reflect worst-case values across the recommended operating conditions. All output jitter and phase specifications are determined through statistical measurement at the package pins.

Operating Frequency Ranges

Table 48: **Operating Frequency Ranges**

			Speed Grade			
Description	**Symbol**	**Constraints**	**-7**	**-6**	**-5**	**Units**
Output Clocks (Low Frequency Mode)						
CLK0, CLK90, CLK180, CLK270	CLKOUT_FREQ_1X_LF_MIN			24.00	24.00	MHz
	CLKOUT_FREQ_1X_LF_MAX			210.00	180.00	MHz
CLK2X, CLK2X180	CLKOUT_FREQ_2X_LF_MIN			48.00	48.00	MHz
	CLKOUT_FREQ_2X_LF_MAX			420.00	360.00	MHz
CLKDV	CLKOUT_FREQ_DV_LF_MIN			1.50	1.50	MHz
	CLKOUT_FREQ_DV_LF_MAX			140.00	120.00	MHz
CLKFX, CLKFX180	CLKOUT_FREQ_FX_LF_MIN			24.00	24.00	MHz
	CLKOUT_FREQ_FX_LF_MAX			240.00	210.00	MHz
Input Clocks (Low Frequency Mode)						
CLKIN (using DLL outputs)(1)	CLKIN_FREQ_DLL_LF_MIN			24.00	24.00	MHz
	CLKIN_FREQ_DLL_LF_MAX			210.00	180.00	MHz
CLKIN (using CLKFX outputs)(2)	CLKIN_FREQ_FX_LF_MIN			1.00	1.00	MHz
	CLKIN_FREQ_FX_LF_MAX			240.00	210.00	MHz
PSCLK	PSCLK_FREQ_LF_MIN			0.01	0.01	MHz
	PSCLK_FREQ_LF_MAX			420.00	360.00	MHz
Output Clocks (High Frequency Mode)						
CLK0, CLK180	CLKOUT_FREQ_1X_HF_MIN			48.00	48.00	MHz
	CLKOUT_FREQ_1X_HF_MAX			420.00	360.00	MHz
CLKDV	CLKOUT_FREQ_DV_HF_MIN			3.00	3.00	MHz
	CLKOUT_FREQ_DV_HF_MAX			280.00	240.00	MHz
CLKFX, CLKFX180	CLKOUT_FREQ_FX_HF_MIN			210.00	210.00	MHz
	CLKOUT_FREQ_FX_HF_MAX			320.00	270.00	MHz
Input Clocks (High Frequency Mode)						
CLKIN (using DLL outputs)(1)	CLKIN_FREQ_DLL_HF_MIN			48.00	48.00	MHz
	CLKIN_FREQ_DLL_HF_MAX			420.00	360.00	MHz
CLKIN (using CLKFX outputs)(2)	CLKIN_FREQ_FX_HF_MIN			50.00	50.00	MHz
	CLKIN_FREQ_FX_HF_MAX			320.00	270.00	MHz
PSCLK	PSCLK_FREQ_HF_MIN			0.01	0.01	MHz
	PSCLK_FREQ_HF_MAX			420.00	360.00	MHz

Notes:
1. "DLL outputs" is used here to describe the outputs: CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, and CLKDV.
2. If both DLL and CLKFX outputs are used, follow the more restrictive specification.

Input Clock Tolerances

Table 49: **Input Clock Tolerances**

Description	Symbol	Constraints F_{CLKIN}	Speed Grade						Units
			–7		–6		–5		
			Min	Max	Min	Max	Min	Max	
Input Clock Low/high Pulse Width									
PSCLK	PSCLK_PULSE	< 1MHz			25.00		25.00		ns
PSCLK and CLKIN(2)	PSCLK_PULSE and CLKIN_PULSE	1 – 10 MHz			25.00		25.00		ns
		10 – 25 MHz			10.00		10.00		ns
		25 – 50 MHz			5.00		5.00		ns
		50 – 100 MHz			3.00		3.00		ns
		100 – 150 MHz			2.40		2.40		ns
		150 – 200 MHz			2.00		2.00		ns
		200 – 250 MHz			1.80		1.80		ns
		250 – 300 MHz			1.50		1.50		ns
		300 – 350 MHz			1.30		1.30		ns
		350 – 400 MHz			1.15		1.15		ns
		> 400 MHz			1.05		1.05		ns
Input Clock Cycle-Cycle Jitter (Low Frequency Mode)									
CLKIN (using DLL outputs)(1)	CLKIN_CYC_JITT_DLL_LF					±300		±300	ps
CLKIN (using CLKFX outputs)(2)	CLKIN_CYC_JITT_FX_LF					±300		±300	ps
Input Clock Cycle-Cycle Jitter (High Frequency Mode)									
CLKIN (using DLL outputs)(1)	CLKIN_CYC_JITT_DLL_HF					±150		±150	ps
CLKIN (using CLKFX outputs)(2)	CLKIN_CYC_JITT_FX_HF					±150		±150	ps
Input Clock Period Jitter (Low Frequency Mode)									
CLKIN (using DLL outputs)(1)	CLKIN_PER_JITT_DLL_LF					±1		±1	ns
CLKIN (using CLKFX outputs)(2)	CLKIN_PER_JITT_FX_LF					±1		±1	ns
Input Clock Period Jitter (High Frequency Mode)									
CLKIN (using DLL outputs)(1)	CLKIN_PER_JITT_DLL_HF					±1		±1	ns
CLKIN (using CLKFX outputs)(2)	CLKIN_PER_JITT_FX_HF					±1		±1	ns
Feedback Clock Path Delay Variation									
CLKFB off-chip feedback	CLKFB_DELAY_VAR_EXT					±1		±1	ns

Notes:
1. “”DLL outputs” is used here to describe the outputs: CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, and CLKDV.
2. If both DLL and CLKFX outputs are used, follow the more restrictive specification.

Output Clock Jitter

Table 50: **Output Clock Jitter**

Description	Symbol	Constraints	Speed Grade			Units
			–7	–6	–5	
Clock Synthesis Period Jitter						
CLK0	CLKOUT_PER_JITT_0			±100	±100	ps
CLK90	CLKOUT_PER_JITT_90			±150	±150	ps
CLK180	CLKOUT_PER_JITT_180			±150	±150	ps
CLK270	CLKOUT_PER_JITT_270			±150	±150	ps
CLK2X, CLK2X180	CLKOUT_PER_JITT_2X			±200	±200	ps
CLKDV (integer division)	CLKOUT_PER_JITT_DV1			±150	±150	ps
CLKDV (non-integer division)	CLKOUT_PER_JITT_DV2			±300	±300	ps
CLKFX, CLKFX180	CLKOUT_PER_JITT_FX			Note 1	Note 1	ps

Notes:
1. Values for this parameter are available on the Xilinx Support website in **Answer Record 13645**.

Output Clock Phase Alignment

Table 51: **Output Clock Phase Alignment**

Description	Symbol	Constraints	Speed Grade			Units
			–7	–6	–5	
Phase Offset Between CLKIN and CLKFB						
CLKIN/CLKFB	CLKIN_CLKFB_PHASE			±50	±50	ps
Phase Offset Between Any DCM Outputs						
All CLK* outputs	CLKOUT_PHASE			±140	±140	ps
Duty Cycle Precision						
DLL outputs(1)	CLKOUT_DUTY_CYCLE_DLL(2)			±150	±150	ps
CLKFX outputs	CLKOUT_DUTY_CYCLE_FX			±100	±100	ps

Notes:
1. “”DLL outputs” is used here to describe the outputs: CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, and CLKDV.
2. CLKOUT_DUTY_CYCLE_DLL applies to the 1X clock outputs (CLK0, CLK90, CLK180, and CLK270) only if DUTY_CYCLE_CORRECTION = TRUE.
3. Specification also applies to PSCLK.

Miscellaneous Timing Parameters

Table 52: **Miscellaneous Timing Parameters**

			Speed Grade			
Description	**Symbol**	**Constraints F_{CLKIN}**	**-7**	**-6**	**-5**	**Units**
Time Required to Achieve LOCK						
Using DLL outputs(1)	LOCK_DLL:					
	LOCK_DLL_60	> 60MHz		20.00	20.00	us
	LOCK_DLL_50_60	50 - 60 MHz		25.00	25.00	us
	LOCK_DLL_40_50	40 - 50 MHz		50.00	50.00	us
	LOCK_DLL_30_40	30 - 40 MHz		90.00	90.00	us
	LOCK_DLL_24_30	24 - 30 MHz		120.00	120.00	us
Using CLKFX outputs	LOCK_FX_MIN			10.00	10.00	ms
	LOCK_FX_MAX			10.00	10.00	ms
Additional lock time with fine phase shifting	LOCK_DLL_FINE_SHIFT			50.00	50.00	us
Fine Phase Shifting						
Absolute shifting range	FINE_SHIFT_RANGE			10.00	10.00	ns
Delay Lines						
Tap delay resolution	DCM_TAP_MIN			30.00	30.00	ps
	DCM_TAP_MAX			50.00	50.00	ps

Notes:
1. “”DLL outputs” is used here to describe the outputs: CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, and CLKDV.

Frequency Synthesis

Table 53: **Frequency Synthesis**

Attribute	Min	Max
CLKFX_MULTIPLY	2	32
CLKFX_DIVIDE	1	32

Parameter Cross-Reference

Table 54: **Parameter Cross-Reference**

Libraries Guide	Data Sheet
DLL_CLKOUT_{MIN|MAX}_LF	CLKOUT_FREQ_{1X|2X|DV}_LF
DFS_CLKOUT_{MIN|MAX}_LF	CLKOUT_FREQ_FX_LF
DLL_CLKIN_{MIN|MAX}_LF	CLKIN_FREQ_DLL_LF
DFS_CLKIN_{MIN|MAX}_LF	CLKIN_FREQ_FX_LF
DLL_CLKOUT_{MIN|MAX}_HF	CLKOUT_FREQ_{1X|DV}_HF
DFS_CLKOUT_{MIN|MAX}_HF	CLKOUT_FREQ_FX_HF
DLL_CLKIN_{MIN|MAX}_HF	CLKIN_FREQ_DLL_HF
DFS_CLKIN_{MIN|MAX}_HF	CLKIN_FREQ_FX_HF

Source-Synchronous Switching Characteristics

The parameters in this section provide the necessary values for calculating timing budgets for Virtex-II Pro source-synchronous transmitter and receiver data-valid windows.

Table 55: **Duty Cycle Distortion and Clock-Tree Skew**

Description	Symbol	Device	Speed Grade			Units
			–7	–6	–5	
Duty Cycle Distortion(1)	T_{DCD_CLK0}	All				ps
	T_{DCD_CLK180}	All				ps
Clock Tree Skew(2)	T_{CKSKEW}	XC2VP2				ps
		XC2VP4				ps
		XC2VP7				ps
		XC2VP20				ps
		XC2VP30				ps
		XC2VP40				ps
		XC2VP50				ps
		XC2VP70				ps
		XC2VP100				ps
		XC2VP125				ps

Notes:

1. These parameters represent the worst-case duty cycle distortion observable at the pins of the device using LVDS output buffers. For cases where other I/O standards are used, IBIS can be used to calculate any additional duty cycle distortion that might be caused by asymmetrical rise/fall times.
   T_{DCD_CLK0} applies to cases where local (IOB) inversion is used to provide the negative-edge clock to the DDR element in the I/O.
   T_{DCD_CLK180} applies to cases where the CLK180 output of the DCM is used to provide the negative-edge clock to the DDR element in the I/O.
2. This value represents the worst-case clock-tree skew observable between sequential I/O elements. Significantly less clock-tree skew exists for I/O registers that are close to each other and fed by the same or adjacent clock-tree branches. Use the Xilinx FPGA_Editor and Timing Analyzer tools to evaluate clock skew specific to your application.

Table 56: **Package Skew**

Description	Symbol	Device/Package	Value	Units
Package Skew(1)	$T_{PKGSKEW}$			ps
				ps
				ps
				ps
				ps
				ps
				ps
				ps
				ps

Notes:

1. These values represent the worst-case skew between any two balls of the package: shortest flight time to longest flight time from Pad to Ball (7.1ps per mm).
2. Package trace length information is available for these device/package combinations. This information can be used to deskew the package.

Table 57: **Sample Window**

Description	Symbol	Device	Speed Grade			Units
			–7	–6	–5	
Sampling Error at Receiver Pins(1)	T_{SAMP}	XC2VP2				ps
		XC2VP4				ps
		XC2VP7				ps
		XC2VP20				ps
		XC2VP30				ps
		XC2VP40				ps
		XC2VP50				ps
		XC2VP70				ps
		XC2VP100				ps
		XC2VP125				ps

Notes:
1. This parameter indicates the total sampling error of Virtex-II Pro DDR input registers across voltage, temperature, and process. The characterization methodology uses the DCM to capture the DDR input registers' edges of operation. These measurements include:
   - CLK0 and CLK180 DCM jitter
   - Worst-case Duty-Cycle Distortion - T_{DCD_CLK180}
   - DCM accuracy (phase offset)
   - DCM phase shift resolution.

   These measurements do not include package or clock tree skew.

Table 58: **Pin-to-Pin Setup/Hold: Source-Synchronous Configuration**

Description	Symbol	Device	Speed Grade			Units
			–7	–6	–5	
Data Input Set-Up and Hold Times Relative to a Forwarded Clock Input Pin, Using DCM and Global Clock Buffer. For situations where clock and data inputs conform to different standards, adjust the setup and hold values accordingly using the values shown in **IOB Input Switching Characteristics Standard Adjustments**, page 20.						
No Delay Global Clock and IFF with DCM	T_{XXX}	XC2VP2				ns
		XC2VP4				ns
		XC2VP7				ns
		XC2VP20				ns
		XC2VP30				ns
		XC2VP40				ns
		XC2VP50				ns
		XC2VP70				ns
		XC2VP100				ns
		XC2VP125				ns

Notes:
1. IFF = Input Flip-Flop
2. The timing values were measured using the fine-phase adjustment feature of the DCM.
3. The worst-case duty-cycle distortion and DCM jitter on CLK0 and CLK180 is included in these measurements.

Source Synchronous Timing Budgets

This section describes how to use the parameters provided in the Source-Synchronous Switching Characteristics section to develop system-specific timing budgets. The following analysis provides information necessary for determining Virtex-II Pro contributions to an overall system timing analysis; no assumptions are made about the effects of Inter-Symbol Interference or PCB skew.

Virtex-II Pro Transmitter Data-Valid Window (T_X)

T_X is the minimum aggregate valid data period for a source-synchronous data bus at the pins of the device and is calculated as follows:

$$T_X = \text{Data Period} - [\text{Jitter}^{(1)} + \text{Duty Cycle Distortion}^{(2)} + \text{TCKSKEW}^{(3)} + \text{TPKGSKEW}^{(4)}]$$

Notes:

1. Jitter values and accumulation methodology to be provided in a future release of this document. The absolute period jitter values found in the DCM Timing Parameters section of the particular DCM output clock used to clock the IOB FF can be used for a best case analysis.
2. This value depends on the clocking methodology used. See Note1 for Table 55.
3. This value represents the worst-case clock-tree skew observable between sequential I/O elements. Significantly less clock-tree skew exists for I/O registers that are close to each other and fed by the same or adjacent clock-tree branches. Use the Xilinx FPGA_Editor and Timing Analyzer tools to evaluate clock skew specific to your application.
4. These values represent the worst-case skew between any two balls of the package: shortest flight time to longest flight time from Pad to Ball.

Virtex-II Pro Receiver Data-Valid Window (R_X)

R_X is the required minimum aggregate valid data period for a source-synchronous data bus at the pins of the device and is calculated as follows:

$$R_X = [\text{TSAMP}^{(1)} + \text{TCKSKEW}^{(2)} + \text{TPKGSKEW}^{(3)}]$$

Notes:

1. This parameter indicates the total sampling error of Virtex-II Pro DDR input registers across voltage, temperature, and process. The characterization methodology uses the DCM to capture the DDR input registers' edges of operation. These measurements include:
   - CLK0 and CLK180 DCM jitter in a quiet system
   - Worst-case duty-cycle distortion
   - DCM accuracy (phase offset)
   - DCM phase shift resolution.

   These measurements do not include package or clock tree skew.
2. This value represents the worst-case clock-tree skew observable between sequential I/O elements. Significantly less clock-tree skew exists for I/O registers that are close to each other and fed by the same or adjacent clock-tree branches. Use the Xilinx FPGA_Editor and Timing Analyzer tools to evaluate clock skew specific to your application.
3. These values represent the worst-case skew between any two balls of the package: shortest flight time to longest flight time from Pad to Ball.

Revision History

This section records the change history for this module of the data sheet.

Date	Version	Revision
01/31/02	1.0	Initial Xilinx release.
06/17/02	2.0	• Added new Virtex-II Pro family members. • Added timing parameters from speedsfile **v1.62**. • Added Table 37, Pipelined Multiplier Switching Characteristics. • Added 3.3V-vs-2.5V table entries for some parameters.
09/03/02	2.1	• Added Source-Synchronous Switching Characteristics section. • Added absolute max ratings for 3.3V-vs-2.5V parameters in Table 1. • Added recommended operating conditions for V_{IN} and RocketIO footnote to Table 2. • Updated SSTL2 values in Table 6. Added SSTL18 values: Table 6, Table 31, Table 32. • Added Table 10, which contains LVPECL DC specifications.
09/27/02	2.2	Added section General Power Supply Requirements.

Date	Version	Revision
11/20/02	2.3	Updated parametric information in: • Table 1: Increase Absolute Max Rating for V_{CCO}, V_{REF}, V_{IN}, and V_{TS} from 3.6V to 3.75V. Delete cautionary footnotes related to voltage overshoot/undershoot. • Table 2: Delete V_{CCO} specifications for 2.5V and below operation. Delete footnote referencing special information for 3.3V operation. Add footnote for PCI/PCI-X. • Table 3: Add I_{BATT}. Delete I_L specifications for 2.5V and below operation. • Table 4: Add Typical Quiescent Supply Currents for XC2VP4 and XC2VP7 only • Table 6: Correct I_{OL} and I_{OH} for SSTL2 I. Add rows for LVTTL, LVCMOS33, and PCI-X. Correct max V_{IH} from V_{CCO} to 3.6V. • Table 7: Correct Min/Max V_{OD}, V_{OCM}, and V_{ICM} • Table 10: Reformat LVPECL DC Specifications to match Virtex-II data sheet format • Table 11: Correct parameter name from Differential Output Voltage to Single-Ended Output Voltage Swing. • Table 15: Add CPMC405CLOCK max frequencies • Table 23: Add footnote regarding serial data rate limitation in -5 part. • Table 31: Add rows for LVTTL, LVCMOS33, and PCI-X. • Table 32: Add LVTTL, LVCMOS33, and PCI-X. Correct all capacitive load values (except PCI/PCI-X) to 0 pF. • Table 42: Correct CCLK max frequencies
11/25/02	2.4	Table 1: Correct lower limit of voltage range of V_{IN} and V_{TS} from –0.3V to –0.5V for 3.3V.
12/03/02	2.5	Updated parametric information in: • Table 1: Correct lower limit of voltage range of V_{IN} and V_{TS} from –0.5V to –0.3V for 3.3V. • Table 2: Add footnote (2) regarding V_{CCAUX} voltage droop. Renumbered other notes. • Table 11: Add waveform diagrams (Figure 1 and Figure 2) illustrating DV_{OUT} (single-ended) and DV_{PPOUT} (differential). • Table 21: Indicate REFCLK upper frequency limitation; relate REFCLK parameters to REFCLK2, BREFCLK, and BREFCLK2; correct T_{RCLK} and T_{FCLK} values and unit of measurement. • Table 51: Add qualifying footnote to CLKOUT_DUTY_CYCLE_DLL.
01/20/03	2.6	Updated parametric information in: • Table 11: Correct DV_{IN} Min (200 mV to 175 mV) and DV_{IN} Max (1000 mV to 2000 mV). • Table 21: Correct T_{RCLK} / T_{FCLK} Typ (400 ps to 600 ps) and Max (600 ps to 1000 ps). Add footnote (2) to qualify Max T_{GJTT} parameter. • Table 50: Correct hyperlink in footnote (1) to point directly to Answer Record 13645. • Move clock parameters from Table 17, Table 18, Table 19, and Table 20 to Table 15.

Virtex-II Pro Data Sheet

The Virtex-II Pro Data Sheet contains the following modules:

- **Virtex-II Pro™ Platform FPGAs: Introduction and Overview (Module 1)**
- **Virtex-II Pro™ Platform FPGAs: Detailed Description (Module 2)**
- **Virtex-II Pro™ Platform FPGAs: DC and Switching Characteristics (Module 3)**
- **Virtex-II Pro™ Platform FPGAs: Pinout Information (Module 4)**