CoolRunner-II CPLD Family

DS090 (v1.3) September 24, 2002 **Advance Product Specification**

Features

- Optimized for 1.8V systems
  - Industry's fastest low power CPLD
  - Static Icc of less than 100 microamps at all times
  - Densities from 32 to 512 macrocells
- Industry's best 0.18 micron CMOS CPLD
  - Optimized architecture for effective logic synthesis
  - Multi-voltage I/O operation — 1.5V to 3.3V
- Advanced system features
  - Fastest in system programming
    - 1.8V ISP using IEEE 1532 (JTAG) interface
  - On-The-Fly (OTF) Programming
  - IEEE1149.1 JTAG Boundary Scan Test
  - Optional Schmitt trigger input (per pin)
  - Unsurpassed low power management
  - FZP 100% CMOS product term generation
  - DataGATE external signal control
  - Flexible clocking modes
    - Optional DualEDGE triggered registers
    - Clock divider (÷ 2,4,6,8,10,12,14,16)
    - CoolCLOCK
  - Global signal options with macrocell control
    - Multiple global clocks with phase selection per macrocell
    - Multiple global output enables
    - Global set/reset
  - Abundant product term clocks, output enables and set/resets
  - Efficient control term clocks, output enables and set/resets for each macrocell and shared across function blocks
  - Advanced design security
  - Open-drain output option for Wired-OR and LED drive
  - Optional bus-hold or weak pullup on selected I/O pins
  - Optional configurable grounds on unused I/Os
  - Mixed I/O voltages compatible with 1.5V, 1.8V, 2.5V, and 3.3V logic levels on all parts
    - SSTL2-1,SSTL3-1, and HSTL-1 on 128 macrocell and denser devices
  - PLA architecture
    - Superior pinout retention
    - 100% product term routability across function block
  - Hot pluggable
  - Wide package availability including fine pitch:
    - Chip Scale Package (CSP) BGA, Fine Line BGA, TQFP, PQFP, VQFP, and PLCC packages
  - Design entry/verification using Xilinx and industry standard CAE tools
  - Free software support for all densities using Xilinx WebPACK™ or WebFITTER™ tools
  - Industry leading nonvolatile 0.18 micron CMOS process
  - Guaranteed 1,000 program/erase cycles
  - Guaranteed 20 year data retention

Family Overview

Xilinx CoolRunner™-II CPLDs deliver the high speed and ease of use associated with the XC9500/XL/XV CPLD family with the extremely low power versatility of the XPLA3™ family in a single CPLD. This means that the exact same parts can be used for high-speed data communications/computing systems and leading edge portable products, with the added benefit of In System Programming. Low power consumption and high-speed operation are combined into a single family that is easy to use and cost effective. Xilinx patented Fast Zero Power™ (FZP) architecture inherently delivers very low power performance without the need for any special design measures. Clocking techniques and other power saving features extend the users' power budget. The design features are supported starting with Xilinx ISE 4.1i, WebFITTER, and ISE WebPACK.

Table 1 shows the macrocell capacity and key timing parameters for the CoolRunner-II CPLD family.

Table 1: **CoolRunner-II CPLD Family Parameters**

	XC2C32	XC2C64	XC2C128	XC2C256	XC2C384	XC2C512
Macrocells	32	64	128	256	384	512
Max I/O	33	64	100	184	240	270
T_{PD} (ns)	3.5	4.0	4.5	5.0	5.5	6.0
T_{SU} (ns)	1.7	2.0	2.1	2.2	2.3	2.4
T_{CO} (ns)	2.8	3.0	3.4	3.8	4.2	4.6
$F_{SYSTEM1}$ (MHz)	333	270	263	238	217	217

Table 2 shows the CoolRunner-II CPLD package offering with corresponding I/O count. All packages are surface mount, with over half of them being ball-grid technologies. The ultra tiny packages permit maximum functional capacity in the smallest possible area. The CMOS technology used in CoolRunner-II CPLDs generates minimal heat, allowing the use of tiny packages during high-speed operation.

There are at least two densities present in each package with three in the VQ100 (100-pin 1.0mm QFP) and TQ144 (144-pin 1.4mm QFP), and in the FT256 (256-ball 1.0mm spacing FLBGA). The FT256 is particularly important for slim dimensioned portable products with mid- to high-density logic requirements.

Table 2: **CoolRunner-II CPLD Family Packages and I/O Count**

	XC2C32	XC2C64	XC2C128	XC2C256	XC2C384	XC2C512
PC44	33	33	-	-	-	-
VQ44	33	33	-	-	-	-
CP56	33	45	-	-	-	-
VQ100	-	64	80	80	-	-
CP132	-	-	100	106	-	-
TQ144	-	-	100	118	118	-
PQ208	-	-	-	173	173	173
FT256	-	-	-	184	212	212
FG324	-	-	-	-	240	270

Table 3 details the distribution of advanced features across the CoolRunner-II CPLD family. The family has uniform basic features with advanced features included in densities where they are most useful. For example, it is very unlikely that four I/O banks are needed on 32 and 64 macrocell parts, but very likely they are for 384 and 512 macrocell parts. The I/O banks are groupings of I/O pins using any one of a subset of compatible voltage standards that share the same V_{CCIO} level. (See Table 4 for a summary of CoolRunner-II I/O standards.) The clock division capability is less efficient on small parts, but more useful and likely to be used on larger ones. DataGATE, an ability to block and latch inputs to save power, is valuable in larger parts, but brings marginal benefit to small parts.

Table 3: **CoolRunner-II CPLD Family Features**

	XC2C32	XC2C64	XC2C128	XC2C256	XC2C384	XC2C512
IEEE 1532	✓	✓	✓	✓	✓	✓
I/O banks	1	1	2	2	4	4
Clock division	-	-	✓	✓	✓	✓
Clock doubling	✓	✓	✓	✓	✓	✓
DataGATE	-	-	✓	✓	✓	✓
LVTTL	✓	✓	✓	✓	✓	✓
LVCMOS33, 25, 18, and 1.5V I/O	✓	✓	✓	✓	✓	✓
SSTL2-1	-	-	✓	✓	✓	✓
SSTL3-1	-	-	✓	✓	✓	✓
HSTL-1	-	-	✓	✓	✓	✓
Configurable ground	✓	✓	✓	✓	✓	✓
Quadruple data security	✓	✓	✓	✓	✓	✓
Open drain outputs	✓	✓	✓	✓	✓	✓
Hot plugging	✓	✓	✓	✓	✓	✓

Architecture Description

CoolRunner-II CPLD is a highly uniform family of fast, low power CPLDs. The underlying architecture is a traditional CPLD architecture combining macrocells into Function Blocks (FBs) interconnected with a global routing matrix, the Xilinx Advanced Interconnect Matrix (AIM). The Function Blocks use a Programmable Logic Array (PLA) configuration which allows all product tems to be routed and shared among any of the macrocells of the FB. Design software can efficiently synthesize and optimize logic that is subsequently fit to the FBs and connected with the ability to utilize a very high percentage of device resources. Design changes are easily and automatically managed by the software, which exploits the 100% routability of the Programmable Logic Array within each FB. This extremely robust building block delivers the industry's highest pinout retention, under very broad design conditions. The architecture will be explained by expanding the detail as we discuss the underlying Function Blocks, logic and interconnect.

The design software automatically manages these device resources so that users can express their designs using completely generic constructs without knowledge of these architectural details. More advanced users can take advantage of these details to more thoroughly understand the software's choices and direct its results.

Figure 1 shows the high-level architecture whereby Function Blocks attach to pins and interconnect to each other within the internal interconnect matrix. Each FB contains 16 macrocells. The BSC path is the JTAG Boundary Scan Control path. The BSC and ISP block has the JTAG controller and In-System Programming Circuits.

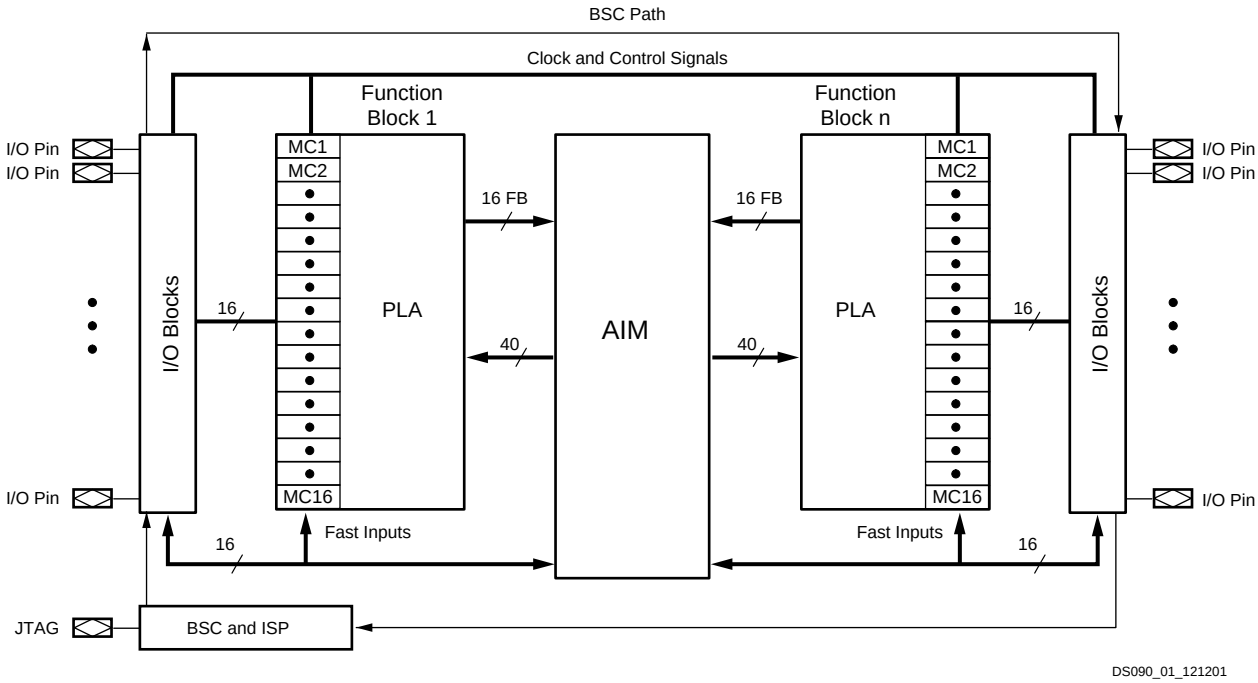

Figure 1: **CoolRunner-II CPLD Architecture**

Function Block

The CoolRunner-II CPLD Function Blocks contain 16 macrocells, with 40 entry sites for signals to arrive for logic creation and connection. The internal logic engine is a 56 product term PLA. All Function Blocks, regardless of the number contained in the device, are identical. For a high-level view of the Function Block, see Figure 2.

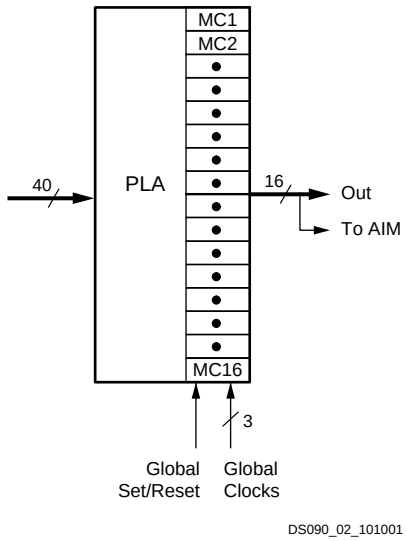

Figure 2: **CoolRunner-II CPLD Function Block**

At the high level, it is seen that the product terms (p-terms) reside in a programmable logic array (PLA). This structure is extremely flexible, and very robust when compared to fixed or cascaded product term function blocks.

Classic CPLDs typically have a few product terms available for a high-speed path to a given macrocell. They rely on capturing unused p-terms from neighboring macrocells to expand their product term tally, when needed. The result of this architecture is a variable timing model and the possibility of stranding unusable logic within the FB.

The PLA is different — and better. First, any product term can be attached to any OR gate inside the FB macrocell(s). Second, any logic function can have as many p-terms as needed attached to it within the FB, to an upper limit of 56. Third, product terms can be re-used at multiple macrocell OR functions so that within a FB, a particular logical product need only be created once, but can be re-used up to 16 times within the FB. Naturally, this plays well with the fitting software, which identifies product terms that can be shared.

The software places as many of those functions as it can into FBs, so it happens for free. There is no need to force macrocell functions to be adjacent or any other restriction save residing in the same FB, which is handled by the software. Functions need not share a common clock, common set/reset or common output enable to take full advantage of the PLA. Also, every product term arrives with the same time delay incurred. There are no cascade time adders for putting more product terms in the FB. When the FB product term budget is reached, there is a small interconnect timing penalty to route signals to another FB to continue creating logic. Xilinx design software handles all this automatically.

Macrocell

The CoolRunner-II CPLD macrocell is extremely efficient and streamlined for logic creation. Users can develop sum of product (SOP) logic expressions that comprise up to 40 inputs and span 56 product terms within a single function block. The macrocell can further combine the SOP expression into an XOR gate with another single p-term expression. The resulting logic expression's polarity is also selectable. As well, the logic function can be pure combinatorial or registered, with the storage element operating selectably as a D or T flip-flop, or transparent latch. Available at each macrocell are independent selections of global, function block level or local p-term derived clocks, sets, resets, and output enables. Each macrocell flip-flop is configurable for either single edge or DualEDGE clocking, providing either double data rate capability or the ability to distribute a slower clock (thereby saving power). For single edge clocking or latching, either clock polarity may be selected per macrocell. CoolRunner-II macrocell details are shown in Figure 3. Note that in Figure 3, standard logic symbols are used except the trapezoidal multiplexers have input selection from statically programmed configuration select lines (not shown). Xilinx application note XAPP376 gives a detailed explanation of how logic is created in the CoolRunner-II CPLD family.

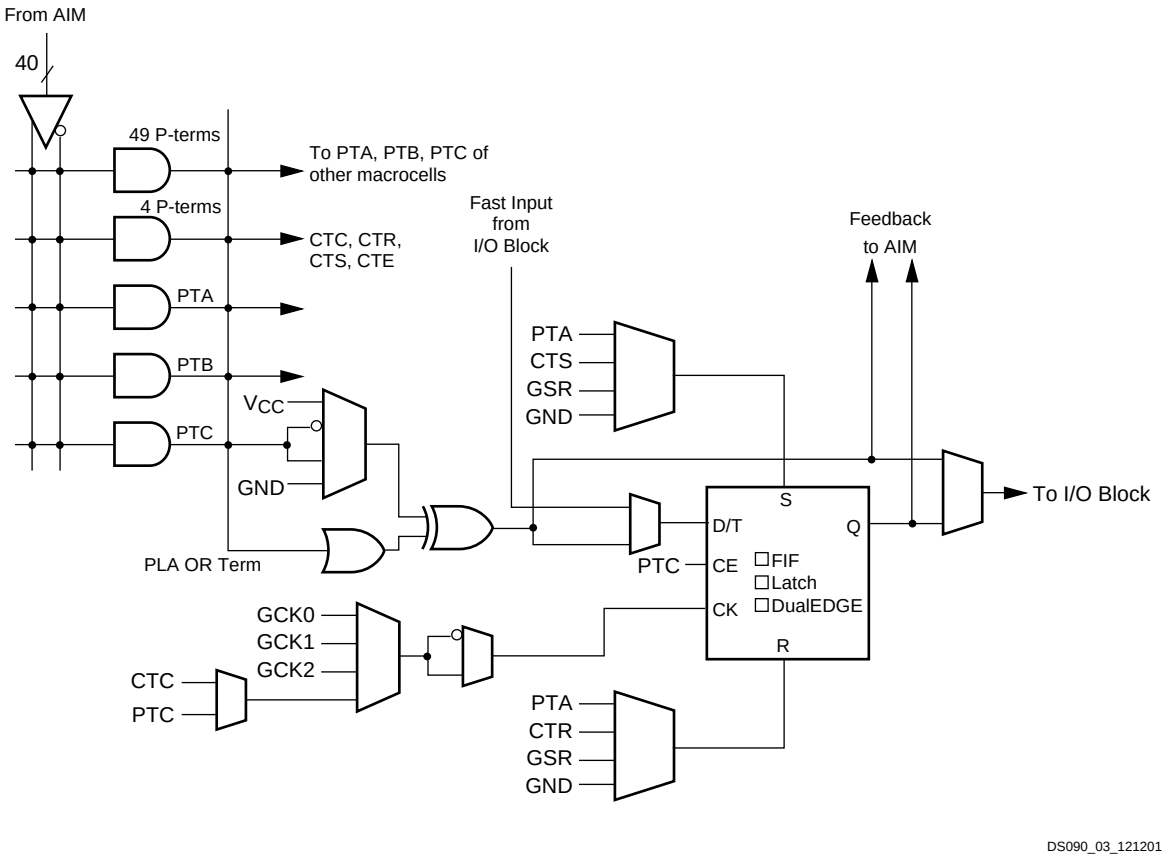

Figure 3: **CoolRunner-II CPLD Macrocell**

When configured as a D-type flip-flop, each macrocell has an optional clock enable signal permitting state hold while a clock runs freely. Note that Control Terms (CT) are available to be shared for key functions within the FB, and are generally used whenever the exact same logic function would be repeatedly created at multiple macrocells. The CT product terms are available for FB clocking (CTC), FB asynchronous set (CTS), FB asynchronous reset (CTR), and FB output enable (CTE).

Any macrocell flip-flop can be configured as an input register or latch, which takes in the signal from the macrocell's I/O pin, and directly drives the AIM. The macrocell combinational functionality is retained for use as a buried logic node if needed.

Advanced Interconnect Matrix (AIM)

The Advanced Interconnect Matrix is a highly connected low power rapid switch. The AIM is directed by the software to deliver up to a set of 40 signals to each FB for the creation of logic. Results from all FB macrocells, as well as, all pin inputs circulate back through the AIM for additional connection available to all other FBs as dictated by the design software. The AIM minimizes both propagation delay and power as it makes attachments to the various FBs.

I/O Block

I/O blocks are primarily transceivers. However, each I/O is either automatically compliant with standard voltage ranges or can be programmed to become so.

In addition to voltage levels, each input can selectively arrive through Schmitt-trigger inputs. This adds a small time delay, but substantially reduces noise on that input pin. Hysteresis also allows easy generation of external clock circuits. The Schmitt-trigger path is best seen in Figure 4.

Outputs can be directly driven, 3-stated or open-drain configured. A choice of slow or fast slew rate output signal is also available. Table 4 summarizes various supported voltage standards associated with specific part capacities. All inputs and disabled outputs are voltage tolerant up to 3.3V.

Figure 4 details the I/O pin, where it is noted that the inputs requiring comparison to an external reference voltage (SSTL2-1, SSTL3-1, HSTL-1) are available on the 128 macrocell and denser parts.

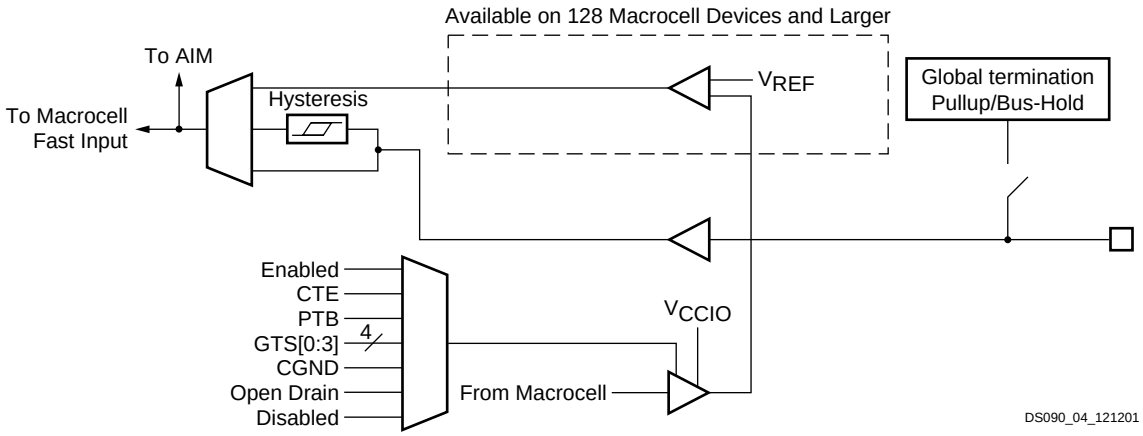

Figure 4: **CoolRunner-II CPLD I/O Block Diagram**

Table 4 summarizes the single ended I/O standard support and shows which standards require V_{REF} values and board termination. V_{REF} detail is given in specific data sheets.

Table 4: **CoolRunner-II CPLD I/O Standard Summary**

I/O Standard	V_{CCIO}	Input V_{REF}	Board Termination Voltage (V_{TT})
LVTTL	3.3	N/A	N/A
LVCMOS33	3.3	N/A	N/A
LVCMOS25	2.5	N/A	N/A
LVCMOS18	1.8	N/A	N/A
1.5V I/O	1.5	N/A	N/A
HSTL-1	1.5	0.75	0.75
SSTL2-1	2.5	1.25	1.25
SSTL3-1	3.3	1.5	1.5

Output Banking

CPLDs are widely used as voltage interface translators. To that end, the output pins are grouped in large banks. The smallest parts are not banked, so all signals will have the same output swing for 32 and 64 macrocell parts. The medium parts (128 and 256 macrocell) support two output banks. With two, the outputs will switch to one of two selected output voltage levels, unless both banks are set to the same voltage. The larger parts (384 and 512 macrocell) support four output banks split evenly. They can support groupings of one, two, three or four separate output voltage levels. This kind of flexibility permits easy interfacing to 3.3V, 2.5V, 1.8V, and 1.5V in a single part.

DataGATE

Low power is the hallmark of CMOS technology. Other CPLD families use a sense amplifier approach to creating product terms, which always has a residual current component being drawn. This residual current can be several hundred milliamps, making them unusable in portable systems. CoolRunner-II CPLDs use standard CMOS methods to create the CPLD architecture and deliver the corresponding low current consumption, without doing any special tricks. However, sometimes designers would like to reduce their system current even more by selectively disabling circuitry not being used.

The patented DataGATE technology was developed to permit a straightforward approach to additional power reduction. Each I/O pin has a series switch that can block the arrival of free running signals that are not of interest. Signals that serve no use may increase power consumption, and can be disabled. Users are free to do their design, then choose sections to participate in the DataGATE function. DataGATE is a logic function that drives an assertion rail threaded through the medium and high-density CoolRunner-II CPLD parts. Designers can select inputs to be blocked under the control of the DataGATE function, effectively blocking controlled switching signals so they do not drive internal chip capacitances. Output signals that do not switch, are held by the bus hold feature. Any set of input pins can be chosen to participate in the DataGATE function. Figure 5 shows the familiar CMOS I_{CC} versus switching frequency graph. With DataGATE, designers can approach zero power, should they choose to, in their designs

Figure 6 shows how DataGATE basically works. One I/O pin drives the DataGATE Assertion Rail. It can have any desired logic function on it. It can be as simple as mapping an input pin to the DataGATE function or as complex as a counter or state machine output driving the DataGATE I/O pin through a macrocell. When the DataGATE rail is asserted low, any pass transistor switch attached to it is blocked. Note that each pin has the ability to attach to the AIM through a DataGATE pass transistor, and thus be blocked. A latch automatically captures the state of the pin when it becomes blocked. The DataGATE Assertion Rail threads throughout all possible I/Os, so each can participate if chosen. Note that one macrocell is singled out to drive the rail, and that macrocell is exposed to the outside

world through a pin, for inspection. If DataGATE is not needed, this pin is an ordinary I/O.

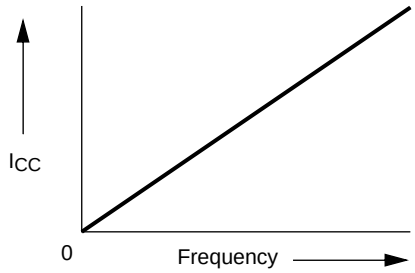

Figure 5: **CMOS I_{CC} vs. Switching Frequency Curve**

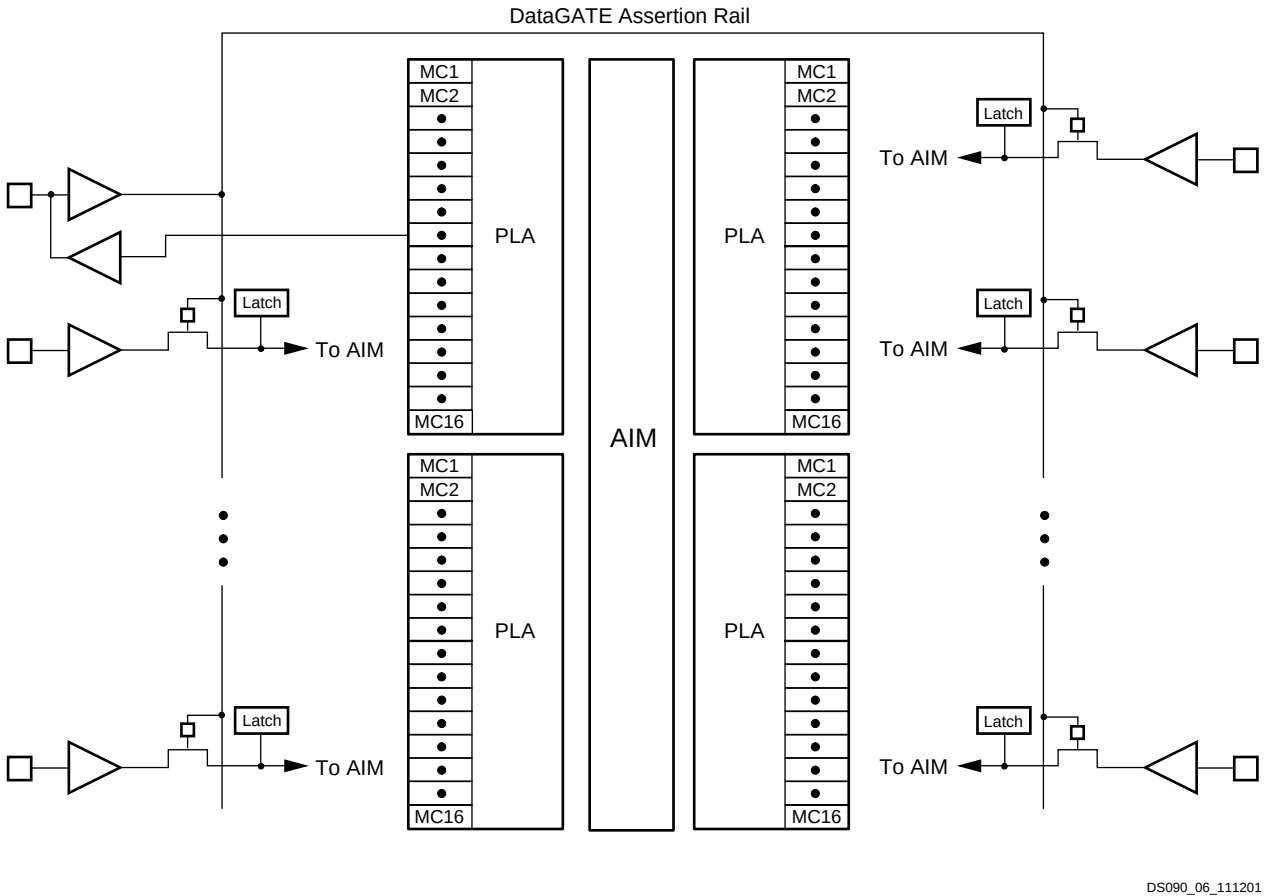

Figure 6: **DataGATE Architecture (output drivers not shown)**

Global Signals

Global signals, clocks (GCK), sets/resets (GSR) and output enables (GTS), are designed to strongly resemble each other. This approach enables design software to make the best utilization of their capabilities. Each global capability is supplemented by a corresponding product term version. Figure 7 shows the common structure of the global signal trees. The pin input is buffered, then drives multiple internal global signal traces to deliver low skew and reduce loading delays. The DataGATE assertion rail is also a global signal.

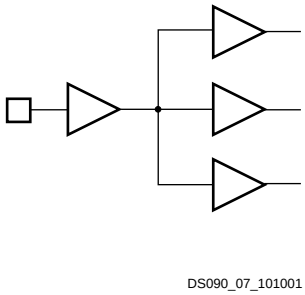

Figure 7: **Global Clocks (GCK), Sets/Resets (GSR) and Output Enables (GTS)**

Additional Clock Options: Division, DualEDGE, and CoolCLOCK

Division

Circuitry has been included in the CoolRunner-II CPLD architecture to divide one externally supplied global clock by standard values. Division by 2,4,6,8,10, 12, 14 and 16 are the options (see Figure 8). This capability is supplied on the GCK2 pin. The resulting clock produced will be 50% duty cycle for all possible divisions. Note that a Synchronous Reset (CDRST) is included to guarantee no runt clocks can get through to the global clock nets. Note that again, the signal is buffered and driven to multiple traces with minimal loading and skew.

DualEDGE

Each macrocell has the ability to double its input clock switching frequency. Figure 9 shows the macrocell flip-flop with the DualEDGE option (doubled clock) at each macrocell. The source to double can be a control term clock, a product term clock or one of the available global clocks. The ability to switch on both clock edges is vital for a number of synchronous memory interface applications as well as certain double data rate I/O applications.

CoolCLOCK

In addition to the DualEDGE flip-flop, additional power savings can be had by combining the clock division circuitry with the DualEDGE circuitry. This capability is called CoolCLOCK and is designed to reduce clocking power within the CPLD. Because the clock net can be an appreciable power drain, the clock power can be reduced by driving the net at half frequency, then doubling the clock rate using DualEDGE triggering at the macrocells. Figure 10 shows how CoolCLOCK is created by internal clock cascading with the divider and DualEDGE flip-flop working together.

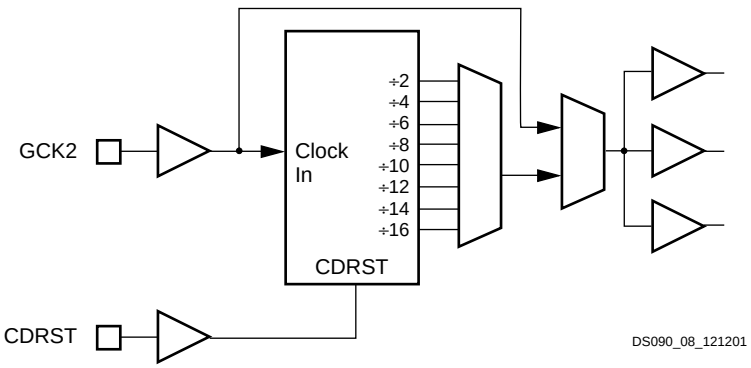

Figure 8: **Clock Division Circuitry for GCK2**

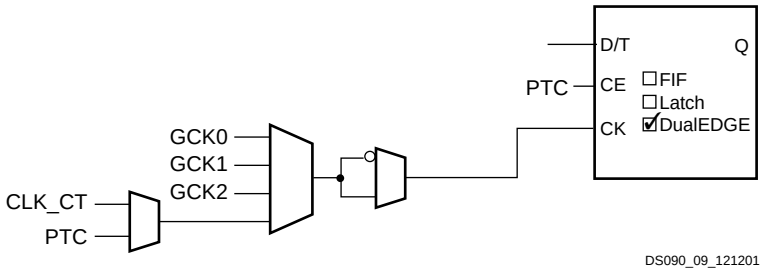

Figure 9: **Macrocell Clock Chain with DualEDGE Option Shown**

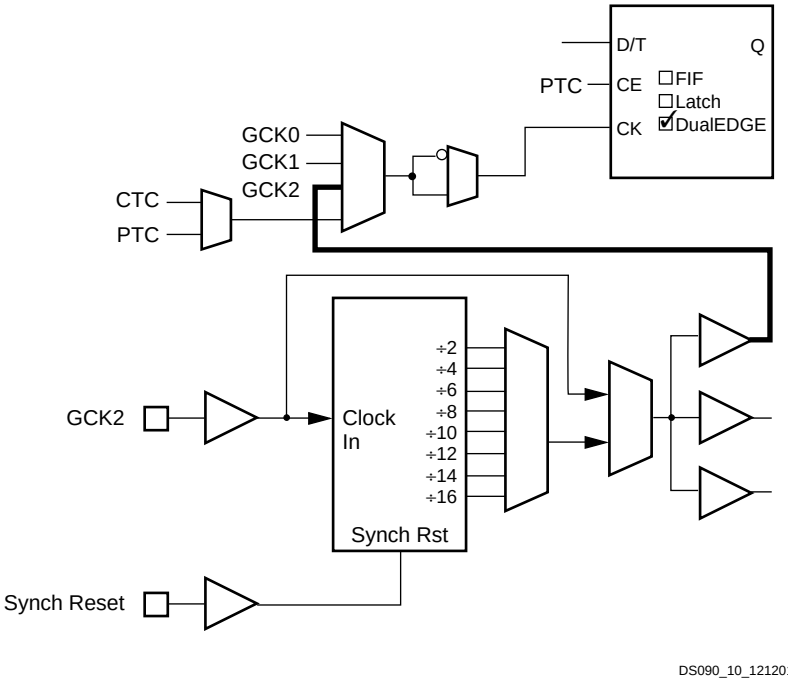

Figure 10: **CoolCLOCK Created by Cascading Clock Divider and DualEDGE Option**

Design Security

Designs can be secured during programming to prevent either accidental overwriting or pattern theft via readback. Four independent levels of security are provided on-chip, eliminating any electrical or visual detection of configuration patterns. These security bits can be reset only by erasing the entire device. Additional detail is omitted intentionally.

Timing Model

Figure 11 shows the CoolRunner-II CPLD timing model. It represents one aspect of the overall architecture from a timing viewpoint. Each little block is a time delay that a signal will incur if the signal passes through such a resource. Timing reports are created by tallying the incremental signal delays as signals progress within the CPLD. Software creates the timing reports after a design has been mapped onto the specific part, and knows the specific delay values for a given speed grade. Equations for the higher level timing values (i.e., T_{PD} and F_{SYSTEM}) are available. Table 5 summarizes the individual parameters and provides a brief definition of their associated functions. Xilinx application note XAPP375 details the CoolRunner-II CPLD family timing with several examples.

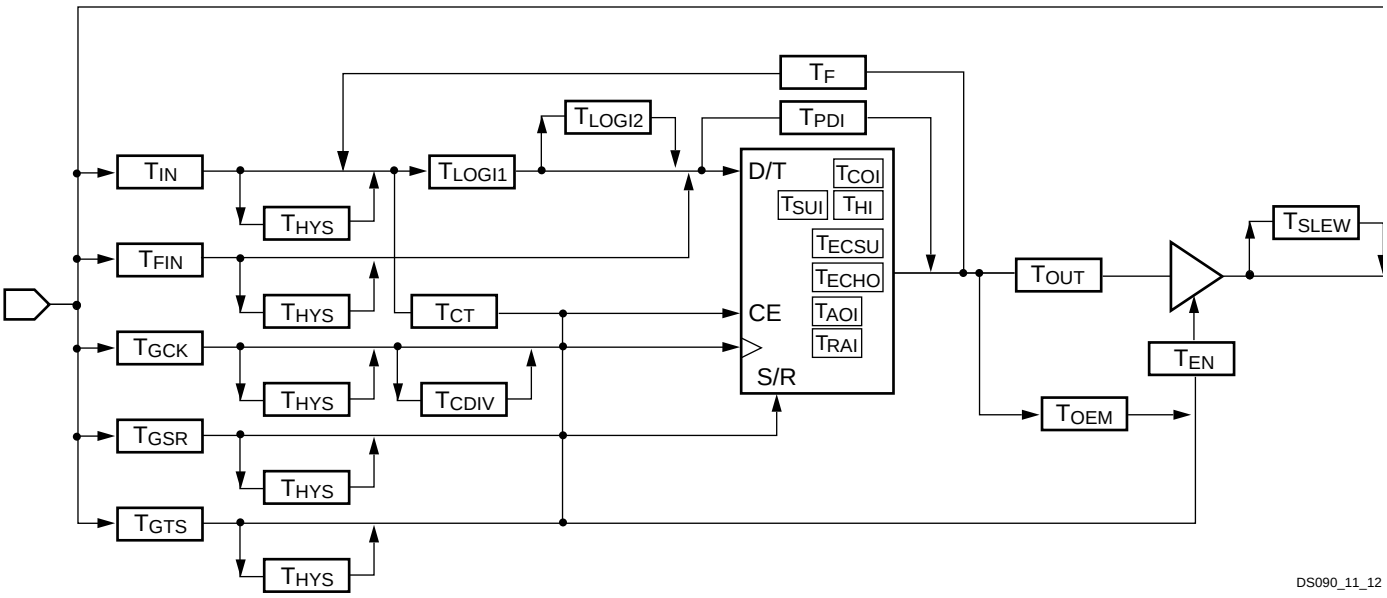

Figure 11: **CoolRunner-II CPLD Timing Model**

Table 5: **Timing Parameter Definitions**

Symbol	Parameter
Buffer Delays	
T_{IN}	Input Buffer Delay
T_{FIN}	Fast data register input delay
T_{GCK}	Global clock (GCK) buffer delay
T_{GSR}	Global set/reset (GSR) buffer delay
T_{GTS}	Global output enable (GTS) buffer delay
T_{OUT}	Output buffer delay
T_{EN}	Output buffer enable/disable delay
T_{SLEW}	Output buffer slew rate control delay
P-term Delays	
T_{CT}	Control Term delay (single PT or FB-CT)
T_{LOGI1}	Single P-term logic delay
T_{LOGI2}	Multiple P-term logic delay adder

Table 5: **Timing Parameter Definitions *(Continued)***

Symbol	Parameter
Macrocell Delays	
T_{PDI}	Macro cell input to output valid
T_{SUI}	Macro register setup before clock
T_{HI}	Macro register hold after clock
T_{ECSU}	Macro register enable clock setup time
T_{ECHO}	Macro register enable clock hold time
T_{COI}	Macro register clock to output valid
T_{RAI}	Macro register set/reset recovery before clock
T_{AOI}	Macro register set/reset to output valid
T_{CDIV}	Clock divider delay adder
T_{HYS}	Hysteresis selection delay adder
Feedback Delays	
T_F	Feedback delay
T_{OEM}	Macrocell to Global OE delay

In System Programming

All CoolRunner-II CPLD parts are 1.8V in system programmable. This means they derive their programming voltage and currents from the 1.8V V_{CC} (internal supply voltage) pins on the part. The V_{CCIO} pins do not participate in this operation, as they may assume another voltage ranging as high as 3.3V down to 1.5V. A 1.8V V_{CC} is required to properly operate the internal state machines and charge pumps that reside within the CPLD to do the nonvolatile programming operations. Xilinx software is provided to deliver the bit-stream to the CPLD and drive the appropriate IEEE 1532 protocol. To that end, there is a set of IEEE 1532 commands that are supported in the CoolRunner-II CPLD parts. Programming times are less than one second for 32 to 256 macrocell parts. Programming times are less than four seconds for 384 and 512 macrocell parts.

On-The-Fly Programming

Xilinx ISE 5.1 supports OTF programming for CoolRunner-II CPLDs. This permits programming a new nonvolatile pattern into the part while another pattern is currently in use.

JTAG Instructions

Table 6 shows the commands available to users. These same commands may be used by third party ATE products, as well. The internal controllers can operate as fast as 66 MHz.

The JTAG interface buffers are powered by a dedicated power pin, V_{CCAUX}, which is independent of all other supply pins.

Table 6: **JTAG Instructions**

Code	Instruction	Description
00000000	EXTEST	Force boundary scan data onto outputs
00000011	PRELOAD	Latch macrocell data into boundary scan cells
11111111	BYPASS	Insert bypass register between TDI and TDO
00000010	INTEST	Force boundary scan data onto inputs and feedbacks
00000001	IDCODE	Read IDCODE
11111101	USERCODE	Read USERCODE
11111100	HIGHZ	Force output into high impedance state
11111010	CLAMP	Latch present output state

Power-Up Characteristics

CoolRunner-II CPLD parts must operate under the demands of both the high-speed and the portable market places, therefore, they must support hot plugging for the high-speed world and tolerate most any power sequence to its various voltage pins. They must also not draw excessive current during power-up initialization. To those ends, the general behavior is summarized as follows:

1. I/O pins are disabled until the end of power-up.
2. As supply rises, configuration bits transfer from nonvolatile memory to SRAM cells.
3. As power up completes, the outputs become as configured (input, output, or I/O).
4. The process takes less than 5 ms and draws less than 5 mA of current.

CoolRunner-II CPLD I/O pins are well behaved under all operating conditions. During power-up, CoolRunner-II devices employ internal circuitry which keeps the devices in the quiescent state until the V_{CCINT} supply voltage is at a safe level (approximately 1.3V). In the quiescent state, JTAG pins are disabled, and all device outputs are disabled with the pins weakly pulled high, as shown in Table 7. When the supply voltage reaches a safe level, all user registers become initialized, and the device is immediately available for operation, as shown in Figure 12.

If the device is in the erased state (before any user pattern is programmed), the device outputs remain disabled with a weak pull-up. The JTAG pins are enabled to allow the device to be programmed at any time. All devices are shipped in the erased state from the factory.

If the device is programmed, the device inputs and outputs take on their configured states for normal operation. The JTAG pins are enabled to allow device erasure or boundary-scan tests at any time.

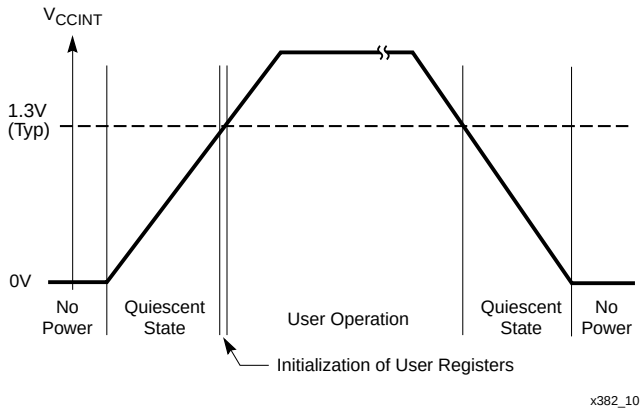

Figure 12: **Device Behavior During Power Up**

Table 7: **I/O Power-Up Characteristics**

Device Circuitry	Quiescent State	Erased Device Operation	Valid User Operation
IOB Bus-Hold	Pull-up	Pull-up	Bus-Hold
Device Outputs	Disabled	Disabled	As Configured
Device Inputs and Clocks	Disabled	Disabled	As Configured
Function Block	Disabled	Disabled	As Configured
JTAG Controller	Disabled	Enabled	Enabled

I/O Banking

CoolRunner-II CPLD 32 and 64 macrocell parts support a single V_{CCIO} rail that can range from 3.3V down to 1.5V operation. Two V_{CCIO} rails are supported on the 128 and 256 macrocell parts where outputs on each rail can independently range from 3.3V down to 1.5V operation. Four V_{CCIO} rails are supported on the 384 and 512 macrocell parts with each rail independently supporting any voltage between 3.3V and 1.5V. The V_{CC} (internal supply voltage) for a CoolRunner-II CPLD must be maintained within 1.8V ±5% for correct speed operation and proper in system programming.

Mixed Voltage, Power Sequencing, and Hot Plugging

As mentioned in I/O Banking, CoolRunner-II CPLD parts support mixed voltage I/O signals where signals within the same bank can range from 3.3V down to 1.5V. The power applied to the V_{CCIO} and V_{CC} pins can occur in any order and the CoolRunner-II CPLD will not be damaged. CoolRunner-II CPLDs can reside on boards where the board is inserted into a “live” connector (hot plugged) and the parts will be well-behaved as if powering up in a standard way.

Development System Support

Xilinx CoolRunner-II CPLDs are supported by all configurations of Xilinx standard release development software as well as the freely available WebFITTER and ISE WebPACK software available from **www.xilinx.com**. Third party development tools include synthesis tools from Cadence, Exemplar, Mentor Graphics, Synplicity, and Synopsys.

ATE Support

Third party ATE development support is available for both programming and board/chip level testing. Vendors providing this support include Hewlett-Packard, GenRad, and Teradyne. Other third party providers are expected to deliver solutions in the future.

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply voltage(2) relative to GND	–0.5	2.0	V
V_I	Input voltage(3) relative to GND	–0.5	4.0	V
TJ	Maximum junction temperature	–40	125	°C
T_{STR}	Storage temperature	–65	150	°C

Notes:

1. Stresses above those listed may cause malfunction or permanent damage to the device. This is a stress rating only. Functional operation at these or any other condition above those indicated in the operational and programming specification is not implied.
2. The chip supply voltage should rise monotonically.
3. Maximum DC undershoot below GND must be limited to either 0.5V or 10 mA, whichever is easier to achieve. During transitions, the device pins may undershoot to –2.0V or overshoot to 3.5 V, provided this over- or undershoot lasts less than 10 ns and with the forcing current being limited to 200 mA. The I/O voltage may never exceed 4.0V.

Quality and Reliability Parameters

Symbol	Parameter	Min	Max	Units
T_{DR}	Data retention	20	-	Years
N_{PE}	Program/erase cycles (Endurance)	1,000	-	Cycles
V_{ESD}	Electrostatic discharge	2,000	-	Volts

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
01/03/02	1.0	Initial Xilinx release.
07/04/02	1.1	Revisions and updates
07/24/02	1.2	Revisions and updates
09/24/02	1.3	Additions to "Power Characteristics" section