XC2C128 CoolRunner-II CPLD

DS093 (v1.0) September 1, 2002 **Advance Product Specification**

Features

- Optimized for 1.8V systems
  - As fast as 4.5 ns pin-to-pin delays
  - As low as 20 µA quiescent current
- Industry's best 0.18 micron CMOS CPLD
  - Optimized architecture for effective logic synthesis
  - Multi-voltage I/O operation — 1.5V to 3.3V
- Available in multiple package options
  - 100-pin VQFP with 80 user I/O
  - 144-pin TQFP with 100 user I/O
  - 132-ball CP (0.5mm) BGA with 100 user I/O
- Advanced system features
  - Fastest in system programming
    - 1.8V ISP using IEEE 1532 (JTAG) interface
  - IEEE1149.1 JTAG Boundary Scan Test
  - Optional Schmitt-trigger input (per pin)
  - Unsurpassed low power management
  - Two seperate output banks
  - Fast Zero Power™ (FZP) 100% CMOS product term generation
  - DataGATE enable (DGE) signal control
  - Flexible clocking modes
    - Optional DualEDGE triggered registers
    - Clock divider (divide by 2,4,6,8,10,12,14,16)
    - CoolCLOCK
  - Global signal options with macrocell control
    - Multiple global clocks with phase selection per macrocell
    - Multiple global output enables
    - Global set/reset
  - Advanced design security
  - Open-drain output option for Wired-OR and LED drive
  - Optional bus-hold, 3-state or weak pullup on selected I/O pins
  - Optional configurable grounds on unused I/Os
  - Mixed I/O voltages compatible with 1.5V, 1.8V, 2.5V, and 3.3V logic levels
    - SSTL2-1, SSTL3-1, and HSTL-1 I/O compatibility
  - Hot pluggable

Refer to the CoolRunner™-II family data sheet for architecture description.

Description

The CoolRunner-II 128-macrocell device is designed for both high performance and low power applications. This lends power savings to high-end communication equipment and high speed to battery operated devices. Low power stand-by and dynamic operation improves overall system reliability.

This device consists of eight Function Blocks inter-connected by a low power Advanced Interconnect Matrix (AIM). The AIM feeds 40 true and complement inputs to each Function Block. The Function Blocks consist of a 40 by 56 P-term PLA and 16 macrocells which contain numerous configuration bits that allow for combinational or registered modes of operation.

Additionally, these registers can be globally reset or preset and configured as D or T flip-flops or as D latches. There are also multiple clock signals, both global and local product term types, configured on a per-macrocell basis. Output pin configurations include slew rate limit, bus hold, pull-up, open drain and programmable grounds. A Schmitt-trigger input is available on a per-input pin basis. In addition to storing macrocell output states, the macrocell registers may be configured as direct input registers to store signals directly from input pins.

Clocking is available on a global or Function Block basis. Three global clocks are available for all Function Blocks as a synchronous clock source. Macrocell registers can be individually configured to power up to the zero or one state. A global set/reset control line is also available to asynchronously set or reset selected registers during operation. Additional local clock, synchronous clock-enable, asynchonous set/reset and output enable signals can be formed using product terms on a per-macrocell or per-Function Block basis.

A DualEDGE flip-flop feature is also available on a per-macrocell basis. This feature allows high performance synchronous operation based on lower frequency clocking to help reduce the total power consumption of the device.

Special circuitry divides one externally supplied global clock (GCK2) by eight different selections. This yields divide by even and odd clock frequencies.

The use of the clock divide (division by 2) and DualEDGE flip-flop gives the resultant CoolCLOCK feature.

DataGATE is a method to selectively disable inputs of the CPLD that are not of interest during certain points in time.

Mapping a signal to the DataGATE function reduces signal switching and thus achieves lower power.

Another feature that eases voltage translation is output banking. Two output banks are available on the CoolRunner-II 128-macrocell device that permit easy interfacing to 3.3V, 2.5V, 1.8V, and 1.5V devices.

The CoolRunner-II 128-macrocell CPLD is I/O compatible with various JEDEC I/O standards (see Table 1). This device is also 1.5V I/O compatible with the use of Schmitt-trigger inputs.

Fast Zero Power Design Technology

Xilinx CoolRunner-II CPLDs are fabricated on a 0.18 micron process technology which is derived from leading edge FPGA product development. CoolRunner-II CPLDs employ Fast Zero Power™ (FZP), a design technique that makes use of CMOS technology in both the fabrication and design methodology. FZP design technology employs a cascade of CMOS gates to implement sum of products instead of traditional sense amplifier methodology. Due to this technology, Xilinx CoolRunner-II CPLDs achieve both high-performance and low power operation.

Supported I/O Standards

The CoolRunner-II 128-macrocell features LVCMOS, LVTTL, SSTL and HSTL I/O implementations. See Table 1 for I/O standard voltages. The LVTTL I/O standard is a general purpose EIA/JEDEC standard for 3.3V applications that use an LVTTL input buffer and Push-Pull output buffer. The LVCMOS standard is used in 3.3V, 2.5V, 1.8V applications. Both HSTL and SSTL make use of a V_{REF} pin for JEDEC compliance. CoolRunner-II CPLDs are also 1.5V I/O compatible with the use of Schmitt-trigger inputs.

Table 1: **I/O Standards for XC2C128**

I/O Types	Output V_{CCIO}	Input V_{CCIO}	Input V_{REF}	Board Termination Voltage V_{TT}
LVTTL	3.3	3.3	N/A	N/A
LVCMOS33	3.3	3.3	N/A	N/A
LVCMOS25	2.5	2.5	N/A	N/A
LVCMOS18	1.8	1.8	N/A	N/A
1.5V I/O	1.5	1.5	N/A	N/A
HSTL-1	1.5	1.5	0.75	0.75
SSTL2-1	2.5	2.5	1.25	1.25
SSTL3-1	3.3	3.3	1.5	1.5

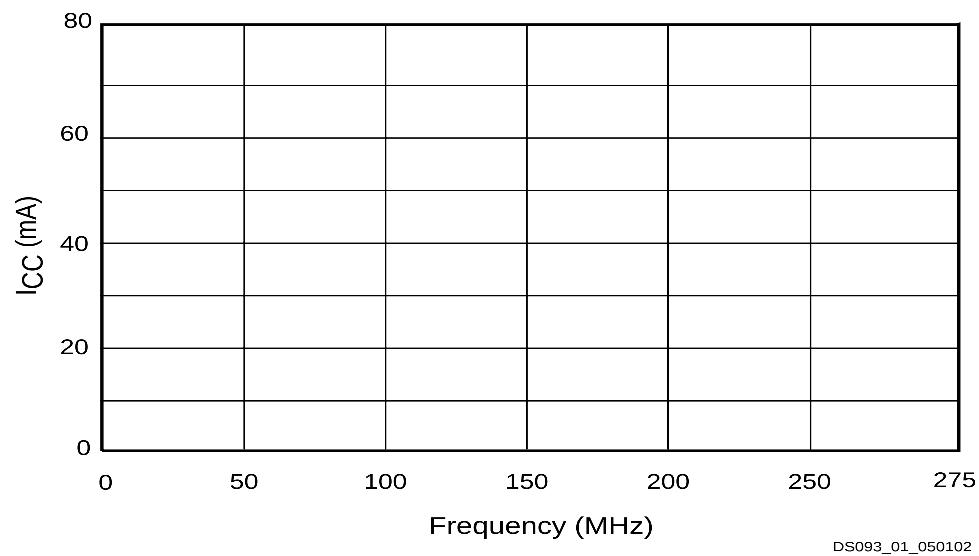


Figure 1: **I_{CC} vs Frequency**

Table 2: **I_{CC} vs Frequency (LVCMOS 1.8V T_A = 25°C)(1)**

	Frequency (MHz)									
	0	25	50	75	100	150	175	200	225	260
Typical -6, -7 I_{CC} (mA)										
Typical -4 I_{CC} (mA)										

Notes:
1. 16-bit up/down, resettable binary counter (one counter per function block).

Absolute Maximum Ratings

Symbol	Description	Value	Units
V_{CC}	Supply voltage relative to ground	–0.5 to 2.0	V
V_{CCIO}	Supply voltage for output drivers	–0.5 to 4.0	V
V_{JTAG}	JTAG input voltage limits	–0.5 to 4.0	V
V_{AUX}	JTAG input supply voltage	–0.5 to 4.0	V
V_{IN}	Input voltage relative to ground(1)	–0.5 to 4.0	V
V_{TS}	Voltage applied to 3-state output(1)	–0.5 to 4.0	V
T_{STG}	Storage Temperature (ambient)	–65 to +150	°C
T_J	Junction Temperature	+ 150	°C

Notes:
1. Maximum DC undershoot below GND must be limited to either 0.5V or 10 mA, whichever is easiest to achieve. During transitions, the device pins may undershoot to –2.0V or overshoot to +4.5V, provided this over or undershoot lasts less than 10 ns and with the forcing current being limited to 200 mA.

Recommended Operating Conditions

Symbol	Parameter		Min	Max	Units
V_{CC}	Supply voltage for internal logic and input buffers	Commercial T_A = 0°C to +70°C	1.7	1.9	V
		Industrial T_A = –40°C to +85°C	1.7	1.9	V
V_{CCIO}	Supply voltage for output drivers @ 3.3V operation		3.0	3.6	V
	Supply voltage for output drivers @ 2.5V operation		2.3	2.7	V
	Supply voltage for output drivers @ 1.8V operation		1.7	1.9	V
	Supply voltage for output drivers @ 1.5V operation		1.4	1.6	V
V_{AUX}	JTAG programming		1.7	3.6	V

DC Electrical Characteristics (Over recommended operating conditions)

Symbol	Parameter	Test Conditions	Min.	Max.	Units
I_{CCSB}	Standby current (-6, -7)	V_{CC} = 1.9V, V_{CCIO} = 3.6V	-	100	µA
I_{CCSB}	Standby current (-4)	V_{CC} = 1.9V, V_{CCIO} = 3.6V			mA
I_{CC} (1)	Dynamic current (-6, -7)	f = 1 MHz			mA
		f = 50 MHz			mA
I_{CC} (1)	Dynamic current (-4)	f = 1 MHz			mA
		f = 50 MHz			mA
C_{JTAG}	JTAG input capacitance	f = 1 MHz	-	10	pF
C_{CLK}	Global clock input capacitance	f = 1 MHz	-	12	pF
C_{IO}	I/O capacitance	f = 1 MHz	-	10	pF

Notes:
1. 16-bit up/down, resettable binary counter (one counter per function block).

LVCMOS and LVTTL 3.3V DC Voltage Specifications

Symbol	Parameter	Test Conditions	Min.	Max.	Units
V_{CCIO}	Input source voltage		3.0	3.6	V
V_{IH}	High level input voltage		2.0	3.9	V
V_{IL}	Low level input voltage		–0.3	0.8	V
V_{OH}	High level output voltage	I_{OH} = –8 mA, V_{CCIO} = 3V	2.4	-	V
		I_{OH} = –0.1 mA, V_{CCIO} = 3V	V_{CCIO} – 0.2V	-	V
V_{OL}	Low level output voltage	I_{OL} = 8 mA, V_{CCIO} = 3V	-	0.4	V
		I_{OL} = 0.1 mA, V_{CCIO} = 3V	-	0.2	V
I_{IL}	Input leakage current	V_{IN} = 0V or V_{CCIO} to 3.9V	–10	10	µA
I_{IH}	I/O High-Z leakage	V_{IN} = 0V or V_{CCIO} to 3.9V	–10	10	µA

LVCMOS 2.5V DC Voltage Specifications

Symbol	Parameter	Test Conditions	Min.	Max.	Units
V_{CCIO}	Input source voltage		2.3	2.7	V
V_{IH}	High level input voltage		1.7	3.9	V
V_{IL}	Low level input voltage		–0.3	0.7	V
V_{OH}	High level output voltage	I_{OH} = –8 mA, V_{CCIO} = 2.3V	V_{CCIO} – 0.4V	-	V
		I_{OH} = –0.1 mA, V_{CCIO} = 2.3V	V_{CCIO} – 0.2V	-	V
V_{OL}	Low level output voltage	I_{OL} = 8 mA, V_{CCIO} = 2.3V	-	0.4	V
		I_{OL} = 0.1 mA, V_{CCIO} = 2.3V	-	0.2	V
I_{IL}	Input leakage current	V_{IN} = 0V or V_{CCIO} to 3.9V	–10	10	µA
I_{IH}	I/O High-Z leakage	V_{IN} = 0V or V_{CCIO} to 3.9V	–10	10	µA

LVCMOS 1.8V DC Voltage Specifications

Symbol	Parameter	Test Conditions	Min.	Max.	Units
V_{CCIO}	Input source voltage		1.7	1.9	V
V_{IH}	High level input voltage		0.65 x V_{CCIO}	3.9	V
V_{IL}	Low level input voltage		–0.3	0.35 x V_{CCIO}	V
V_{OH}	High level output voltage	I_{OH} = –8 mA, V_{CCIO} = 1.7V	V_{CCIO} – 0.45	-	V
		I_{OH} = –0.1 mA, V_{CCIO} = 1.7V	V_{CCIO} – 0.2	-	V
V_{OL}	Low level output voltage	I_{OL} = 8 mA, V_{CCIO} = 1.7V	-	0.45	V
		I_{OL} = 0.1 mA, V_{CCIO} = 1.7V	-	0.2	V
I_{IL}	Input leakage current	V_{IN} = 0 or V_{CCIO} to 3.9V	–10	10	µA
I_{IH}	I/O High-Z leakage	V_{IN} = 0 or V_{CCIO} to 3.9V	–10	10	µA

1.5V DC Voltage Specifications(1)

Symbol	Parameter	Test Conditions	Min.	Max.	Units
V_{CCIO}	Input source voltage		1.4	1.6	V
V_{T+}	Input hysteresis threshold voltage		0.5 x V_{CCIO}	0.8 x V_{CCIO}	V
V_{T-}			0.2 x V_{CCIO}	0.5 x V_{CCIO}	V
V_{OH}	High level output voltage	I_{OH} = –8 mA, V_{CCIO} = 1.4V	V_{CCIO} – 0.45	-	V
		I_{OH} = –0.1 mA, V_{CCIO} = 1.4V	V_{CCIO} – 0.2	-	V
V_{OL}	Low level output voltage	I_{OL} = 8 mA, V_{CCIO} = 1.4V	-	0.4	V
		I_{OL} = 0.1 mA, V_{CCIO} = 1.4V	-	0.2	V
I_{IL}	Input leakage current	V_{IN} = 0 or V_{CCIO} to 3.9V	–10	10	µA
I_{IH}	I/O High-Z leakage	V_{IN} = 0 or V_{CCIO} to 3.9V	–10	10	µA

Notes:
1. Hysteresis used on 1.5V inputs.

SSTL2-1 DC Voltage Specifications

Symbol	Parameter	Test Conditions	Min.	Typ	Max.	Units
V_{CCIO}	Input source voltage		2.3	2.5	2.7	V
V_{REF}(1)	Input reference voltage		1.15	1.25	1.35	V
V_{TT}(2)	Termination voltage		V_{REF} – 0.04	1.25	V_{REF} + 0.04	V
V_{IH}	High level input voltage		V_{REF} + 0.18	-	3.9	V
V_{IL}	Low level input voltage		–0.3	-	V_{REF} – 0.18	V
V_{OH}	High level output voltage	I_{OH} = –8 mA, V_{CCIO} = 2.3V	V_{CCIO} – 0.62	-	-	V
V_{OL}	Low level output voltage	I_{OL} = 8 mA, V_{CCIO} = 2.3V	-	-	0.54	V
I_{IL}	Input leakage current	V_{IN} = 0V or V_{CCIO} to 3.9V	–10	-	10	µA
I_{IH}	I/O High-Z leakage	V_{IN} = 0V or V_{CCIO} to 3.9V	–10	-	10	µA

Notes:
1. V_{REF} should track the variations in V_{CCIO}, also peak to peak AC noise on V_{REF} may not exceed +/- 2% V_{REF}.
2. V_{TT} of transmitting device must track V_{REF} of receiving devices.

SSTL3-1 DC Voltage Specifications

Symbol	Parameter	Test Conditions	Min.	Typ	Max.	Units
V_{CCIO}	Input source voltage		3.0	3.3	3.6	V
V_{REF}(1)	Input reference voltage		1.3	1.5	1.7	V
V_{TT}(2)	Termination voltage		V_{REF} – 0.05	1.5	V_{REF} + 0.05	V
V_{IH}	High level input voltage		V_{REF} + 0.2	-	V_{CCIO} + 0.3	V
V_{IL}	Low level input voltage		–0.3	-	V_{REF} – 0.2	V
V_{OH}	High level output voltage	I_{OH} = –8 mA, V_{CCIO} = 3V	V_{CCIO} – 1.1	-	-	V
V_{OL}	Low level output voltage	I_{OL} = 8 mA, V_{CCIO} = 3V	-	-	0.7	V
I_{IL}	Input leakage current	V_{IN} = 0V or V_{CCIO} to 3.9V	–10	-	10	µA
I_{IH}	I/O High-Z leakage	V_{IN} = 0V or V_{CCIO} to 3.9V	–10	-	10	µA

Notes:
1. V_{REF} should track the variations in V_{CCIO}, also peak to peak AC noise on V_{REF} may not exceed +/- 2% V_{REF}.
2. V_{TT} of transmitting device must track V_{REF} of receiving devices.

HSTL1 DC Voltage Specifications

Symbol	Parameter	Test Conditions	Min.	Typ	Max.	Units
V_{CCIO}	Input source voltage	-	1.4	1.5	1.6	V
V_{REF}(1)	Input reference voltage	-	0.68	0.75	0.90	V
V_{TT}(2)	Termination voltage	-	-	V_{CCIO} x 0.5	-	V
V_{IH}	High level input voltage	-	V_{REF} + 0.1	-	1.9	V
V_{IL}	Low level input voltage	-	–0.3	-	V_{REF} – 0.1	V
V_{OH}	High level output voltage	I_{OH} = –8 mA, V_{CCIO} = 1.4V	V_{CCIO} – 0.4	-	-	V
V_{OL}	Low level output voltage	I_{OL} = 8 mA, V_{CCIO} = 1.4V	-	-	0.4	V
I_{IL}	Input leakage current	V_{IN} = 0 or V_{CCIO} to 3.9V	–10	-	10	μA
I_{IH}	I/O High-Z leakage	V_{IN} = 0 or V_{CCIO} to 3.9V	–10	-	10	μA

Notes:
1. V_{REF} should track the variations in V_{CCIO}, also peak to peak AC noise on V_{REF} may not exceed +/- 2% V_{REF}.
2. V_{TT} of transmitting device must track V_{REF} of receiving devices.

AC Electrical Characteristics (Over Recommended Operating Conditions)

Symbol	Parameter	-4		-6		-7		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
T_{PD1}	Propagation delay single p-term	-	4.2	-	5.6	-	6.7	ns
T_{PD2}	Propagation delay OR array	-	4.5	-	6.0	-	7.5	ns
T_{SUD}	Direct input register set-up time	1.7	-	2.0	-	2.3	-	ns
T_{SU1}	Setup time fast (single p-term)	1.8	-	2.4	-	2.5	-	ns
T_{SU2}	Setup time (OR array)	2.1	-	2.8	-	3.3	-	ns
T_{HF}	Fast input register hold time	0	-	0	-	0	-	ns
T_H	Hold time (Or array or p-term)	0	-	0	-	0	-	ns
T_{CO}	Clock to output	-	3.4	-	4.5	-	6.0	ns
F_{TOGGLE}(1)	Internal toggle rate(1)	-	416	-	250	-	192	MHz
$F_{SYSTEM1}$(2)	Maximum system frequency(2)	-	263	-	213	-	159	MHz
$F_{SYSTEM2}$(2)	Maximum system frequency(2)	-	244	-	196	-	141	MHz
F_{EXT1}(3)	Maximum external frequency(3)	-	192	-	145	-	118	MHz
F_{EXT2}(3)	Maximum external frequency(3)	-	182	-	137	-	108	MHz
T_{PSUD}	Direct input register p-term clock setup time	1.0	-	0.9	-	1.5	-	ns
T_{PSU1}	P-term clock setup time (single p-term)	1.1	-	1.3	-	1.7	-	ns
T_{PSU2}	P-term clock setup time (OR array)	1.4	-	1.7	-	2.5	-	ns
T_{PHF}	Fast input register p-term clock hold time	0.4	-	0.9	-	1.0	-	ns
T_{PH}	P-term clock hold	0.3	-	0.5	-	0.8	-	ns
T_{PCO}	P-term clock to output	-	4.1	-	5.6	-	6.8	ns
T_{OE}/T_{OD}	Global OE to output enable/disable	-	4.3	-	5.6	-	7.0	ns
T_{POE}/T_{POD}	P-term OE to output enable/disable	-	4.8	-	6.4	-	7.3	ns

AC Electrical Characteristics (Over Recommended Operating Conditions)

Symbol	Parameter	-4		-6		-7		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
T_{MOE}/T_{MOD}	Macrocell driven OE to output enable/disable	-	5.5	-	7.2	-	9.2	ns
T_{PAO}	P-term set/reset to output valid	-	5.9	-	7.4	-	9.1	ns
T_{AO}	Global set/reset to output valid	-	6.0	-	7.3	-	9.3	ns
T_{SUEC}	Register clock enable setup time	1.9	-	2.5	-	2.6	-	ns
T_{HEC}	Register clock enable hold time	0	-	0	-	0	-	ns
T_{CW}	Global clock pulse width High or Low	1.2	-	2.0	-	2.6	-	ns
T_{PCW}	P-term pulse width High or Low	4.5	-	6.0	-	7.5	-	ns
T_{DGSU}	Set-up before DataGATE latch assertion	5.0	-	7.0	-	9.0	-	ns
T_{DGHO}	Hold to DataGATE latch assertion	5.0	-	7.0	-	9.0	-	ns
T_{DGR}	DataGATE recovery to new data	-	5.0	-	7.0	-	9.0	ns
T_{DGW}	DataGATE high pulse width	2.0	-	2.5	-	4.0	-	ns
T_{CDRSU}	CDRST setup time before falling edge GCLK2	0.8	-	1.3	-	2.0	-	ns
T_{CDRHO}	Hold time CDRST after falling edge GCLK2	0.0	-	0.0	-	0.0	-	ns
$T_{CONFIG(4)}$	Configuration time							µs

Notes:
1. F_{TOGGLE} (1/2*T_{CW}) is the maximum frequency of a T flip-flop with output enabled
2. $F_{SYSTEM1}$ (1/T_{CYCLE}) is the internal operating frequency for a device with 16-bit resettable binary counter through one p-term per macrocell while $F_{SYSTEM2}$ is through the OR array (one counter per function block)
3. F_{EXT1} (1/T_{SU1}+T_{CO}) is the maximum external frequency using one p-term while F_{EXT2} is through the OR array
4. Typical configuration current during configuration

Internal Timing Parameters

Symbol	Parameter[1]	-4		-6		-7		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
Buffer Delays								
T_{IN}	Input buffer delay	-	1.6	-	2.3	-	2.4	ns
T_{FIN}	Fast data register input delay	-	1.9	-	2.4	-	3.0	ns
T_{GCK}	Global Clock buffer delay	-	1.4	-	1.8	-	2.5	ns
T_{GSR}	Global set/reset buffer delay	-	2.2	-	2.8	-	3.5	ns
T_{GTS}	Global 3-state buffer delay	-	1.6	-	2.1	-	3.0	ns
T_{OUT}	Output buffer delay	-	1.8	-	2.3	-	2.8	ns
T_{EN}	Output buffer enable/disable delay	-	2.7	-	3.5	-	4.0	ns
P-term Delays								
T_{CT}	Control term delay	-	0.5	-	0.6	-	0.9	ns
T_{LOGI1}	Single P-term delay adder	-	0.4	-	0.5	-	0.8	ns
T_{LOGI2}	Multiple P-term delay adder	-	0.3	-	0.4	-	0.8	ns
Macrocell Delay								
T_{PDI}	Input to output valid	-	0.4	-	0.5	-	0.7	ns
T_{SUI}	Setup before clock	1.2	-	1.4	-	1.8	-	ns
T_{HI}	Hold after clock	0	-	0	-	0	-	ns
T_{ECSU}	Enable clock setup time	1.2	-	1.4	-	1.8	-	ns
T_{ECHO}	Enable clock hold time	0	-	0	-	0	-	ns
T_{COI}	Clock to output valid	-	0.2	-	0.4	-	0.7	ns
T_{AOI}	Set/reset to output valid	-	2.0	-	2.2	-	3.0	ns
T_{CDBL}	Clock doubler delay	-	0	-	0	-	0	ns
Feedback Delays								
T_{F}	Feedback delay	-	2.0	-	2.4	-	3.0	ns
T_{OEM}	Macrocell to global OE delay	-	1.2	-	1.5	-	2.0	ns
I/O Standard Time Adder Delays 1.5V CMOS								
T_{HYS15}	Hysteresis input adder	-	2.0	-	3.0	-	4.0	ns
T_{OUT15}	Output adder	-	0.5	-	0.8	-	1.0	ns
T_{SLEW15}	Output slew rate adder	-	2.0	-	3.0	-	4.0	ns
I/O Standard Time Adder Delays 1.8V CMOS								
T_{IN18}	Standard input adder	-	0	-	0	-	0	ns
T_{HYS18}	Hysteresis input adder	-	2.0	-	3.0	-	4.0	ns
T_{OUT18}	Output adder	-	0	-	0	-	0	ns
T_{SLEW}	Output slew rate adder	-	2.0	-	3.0	-	4.0	ns

Internal Timing Parameters *(Continued)*

Symbol	Parameter[1]	-4		-6		-7		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
I/O Standard Time Adder Delays 2.5V CMOS								
T_{IN25}	Standard input adder	-	0.5	-	0.8	-	1.0	ns
T_{HYS25}	Hysteresis input adder	-	1.5	-	2.5	-	3.0	ns
T_{OUT25}	Output adder	-	1.5	-	2.5	-	3.0	ns
T_{SLEW25}	Output slew rate adder	-	2.0	-	3.0	-	4.0	ns
I/O Standard Time Adder Delays 3.3V CMOS/TTL								
T_{IN33}	Standard input adder	-	0.7	-	1.0	-	2.0	ns
T_{HYS33}	Hysteresis input adder	-	1.0	-	2.0	-	3.0	ns
T_{OUT33}	Output adder	-	1.0	-	2.0	-	3.0	ns
T_{SLEW33}	Output slew rate adder	-	2.0	-	3.0	-	4.0	ns
I/O Standard Time Adder Delays HSTL, SSTL								
SSTL2-1	Input adder to TIN, TFIN, TGCK, TGSR, TGTS	-	1.5	-	1.8	-	2.5	ns
	Output adder to TOUT	-	0	-	0	-	0	ns
SSTL3-1	Input adder to TIN, TFIN, TGCK, TGSR, TGTS	-	1.5	-	1.8	-	2.5	ns
	Output adder to TOUT	-	0	-	0	-	0	ns
HSTL-1	Input adder to TIN, TFIN, TGCK, TGSR, TGTS	-	1.5	-	1.8	-	2.5	ns
	Output adder to TOUT	-	0	-	0	-	0	ns

Notes:

1. 1.5 ns input pin signal rise/fall.

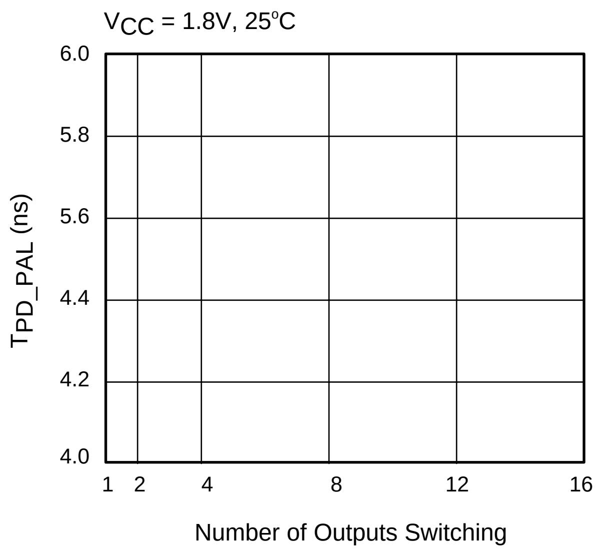
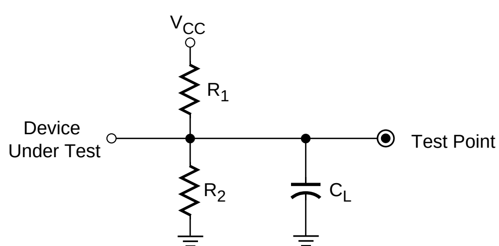


Figure 2: **Switching Characteristics**



Output Type	R_1	R_2	C_L
LVTTL33	268Ω	235Ω	35 pF
LVCMOS33	275Ω	275Ω	35 pF
LVCMOS25	188Ω	188Ω	35pF
LVCMOS18	112.5Ω	112.5Ω	35pF
LVCMOS15	150Ω	150Ω	35pF

C_L includes test fixtures and probe capacitance.
1.5 nsec maximum rise/fall times on inputs.

DS_ACT_08_14_02

Figure 3: **Switching Test Conditions**

Pin Descriptions

Function Block	Macro-cell	VQ100	CP132	TQ144	I/O Bank
1	1	13	G1	17	2
1	2	-	F1	16	2
1	3	12	F2	15	2
1	4	11	F3	14	2
1	5	10	E1	13	2
1	6	9	E2	12	2
1	7	-	-	-	-
1	8	-	-	-	-
1	9	-	-	-	-
1	10	-	-	-	-
1	11	8	E3	11	2
1	12	7	D1	10	2
1	13	6	D2	9	2
1	14	-	C1	7	2
1(GTS1)	15	4	C2	6	2
1(GTS0)	16	3	C3	5	2
2	1	-	G2	19	1
2	2	14	G3	21	1
2	3	15	H1	22	1
2	4	16	H2	23	1
2	5	17	H3	24	1
2	6	18	J1	25	1
2	7	-	-	-	-
2	8	-	-	-	-
2	9	-	-	-	-
2	10	-	-	-	-
2	11	19	J2	26	1
2	12	-	K1	28	1
2(GCK0)	13	22	K3	30	1
2(GCK1)	14	23	L2	32	1
2(CDRST)	15	24	M2	35	1
2(GCK2)	16	27	N2	38	1

Pin Descriptions *(Continued)*

Function Block	Macro-cell	VQ100	CP132	TQ144	I/O Bank
3	1	-	B1	4	2
3(GTS3)	2	2	B2	3	2
3(GTS2)	3	1	A1	2	2
3(GSR)	4	99	A3	143	2
3	5	97	B4	140	2
3	6	96	A4	138	2
3	7	95	C5	136	2
3	8	-	-	-	-
3	9	-	-	-	-
3	10	-	-	-	-
3	11	94	B5	134	2
3	12		A5	133	2
3	13	93	C6	132	2
3	14	92	B6	131	2
3	15	91	A6	130	2
3	16	90	C7	129	2
4(DGE)	1	28	P2	39	1
4	2	-	M3	40	1
4	3	-	N3	41	1
4	4	29	P3	43	1
4	5	30	M4	45	1
4	6	32	M5	49	1
4	7	33	N5	50	1
4	8	-	-	-	-
4	9	-	-	-	-
4	10	-	-	-	-
4	11	34	P5	51	1
4	12	35	M6	52	1
4	13	36	N6	53	1
4	14	37	P6	54	1
4	15	39	N7	56	1
4	16	40	M7	57	1

Pin Descriptions *(Continued)*

Function Block	Macro-cell	VQ100	CP132	TQ144	I/O Bank
5	1	65	G13	94	2
5	2	66	G12	95	2
5	3	67	F14	96	2
5	4	-	F13	97	2
5	5	68	F12	98	2
5	6	-	E13	100	2
5	7	70	E12	101	2
5	8	-	-	-	-
5	9	-	-	-	-
5	10	-	-	-	-
5	11	71	D14	102	2
5	12	72	D13	103	2
5	13	73	D12	104	2
5	14	74	C14	105	2
5	15	76	B13	110	2
5	16	-	A13	111	2
6	1	64	H12	92	1
6	2	63	H13	91	1
6	3	61	J13	88	1
6	4	60	J12	87	1
6	5	59	K14	86	1
6	6	58	K13	85	1
6	7	-	-	-	-
6	8	-	-	-	-
6	9	-	-	-	-
6	10	-	-	-	-
6	11	-	L14	83	1
6	12	56	L13	82	1
6	13	-	L12	81	1
6	14	55	M14	80	1
6	15	-	M13	79	1
6	16	54	M12	78	1

Pin Descriptions *(Continued)*

Function Block	Macro-cell	VQ100	CP132	TQ144	I/O Bank
7	1	77	C12	112	2
7	2	78	B12	113	2
7	3	-	A12	115	2
7	4	79	C11	116	2
7	5	80	B11	117	2
7	6	81	A11	118	2
7	7	-	C10	119	2
7	8	-	-	-	-
7	9	-	-	-	-
7	10	-	-	-	-
7	11	82	A10	120	2
7	12	-	C9	121	2
7	13	85	A8	124	2
7	14	86	B8	125	2
7	15	87	C8	126	2
7	16	89	B7	128	2

Pin Descriptions *(Continued)*

Function Block	Macro-cell	VQ100	CP132	TQ144	I/O Bank
8	1	-	N14	77	1
8	2	53	N13	76	1
8	3	52	P14	74	1
8	4	50	P12	71	1
8	5	-	M11	70	1
8	6	49	N11	69	1
8	7	-	-	-	-
8	8	-	-	-	-
8	9	-	-	-	-
8	10	-	-	-	-
8	11	-	P11	68	1
8	12	46	P10	64	1
8	13	44	P9	61	1
8	14	43	M8	60	1
8	15	42	N8	59	1
8	16	41	P8	58	1

Notes:

1. GTS = global output enable, GSR = global reset/set, GCK = global clock, CDRST = clock divide reset, DGE = DataGATE enable.

XC2C128 JTAG, Power/Ground, No Connect Pins and Total User I/O

Pin Type	VQ100	CP132	TQ144
TCK	48	M10	67
TDI	45	M9	63
TDO	83	B9	122
TMS	47	N10	65
V_{AUX} (JTAG supply voltage)	5	D3	8
Power internal (V_{CC})	26, 57	P1, K12, A2	1, 37, 84
Power Bank 1 I/O (V_{CCIO1})	20, 38, 51	J3, P7, G14, P13	27, 55, 73, 93
Power Bank 2 I/O (V_{CCIO2})	88, 98	A14, C4, A7	109, 127, 141
Ground	21, 25, 31, 62, 69, 75, 84, 100	K2, N1, P4, N9, N12, J14, H14, E14, B14, A9, B3	29, 36, 47, 62, 72, 89, 90, 99, 108, 123, 144
No connects	-	L1, L3, M1, N4, C13, B10	18, 20, 31, 33, 34, 42, 44, 46, 48, 66, 75, 106, 107, 114, 135, 137, 139, 142
Total user I/O (including dual function pins)	80	100	100

Ordering Information

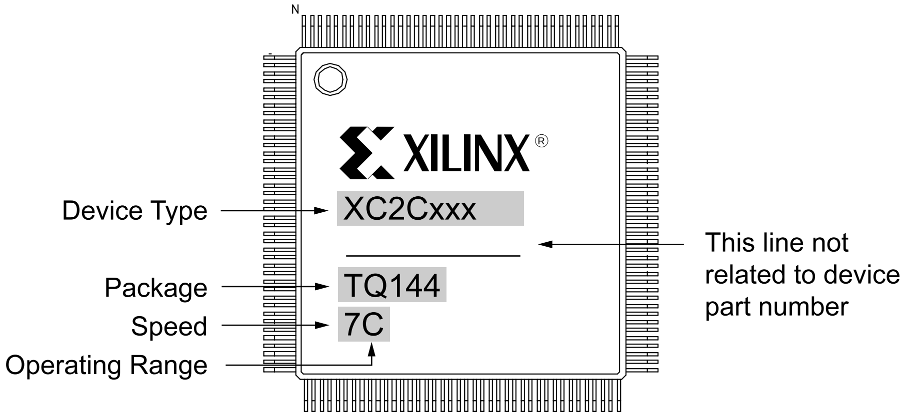


Figure 4: **Sample Package with Part Marking**

Part Number	Pin/Ball Spacing	θ_{JA} (C/Watt)	θ_{JC} (C/Watt)	Package Type	Package Dimensions	I/O	Commercial (C)(1) Industrial (I)(2)
XC2C128-4VQ100C	0.5mm	47.5	12.5	Very Thin Quad Flat Pack	14mm x 14mm	80	C
XC2C128-6VQ100C	0.5mm	47.5	12.5	Very Thin Quad Flat Pack	14mm x 14mm	80	C
XC2C128-7VQ100C	0.5mm	47.5	12.5	Very Thin Quad Flat Pack	14mm x 14mm	80	C
XC2C128-4CP132C	0.5mm	72.4	15.7	Chip Scale Package	8mm x 8mm	100	C
XC2C128-6CP132C	0.5mm	72.4	15.7	Chip Scale Package	8mm x 8mm	100	C
XC2C128-7CP132C	0.5mm	72.4	15.7	Chip Scale Package	8mm x 8mm	100	C
XC2C128-4TQ144C	0.5mm	46.1	7.9	Thin Quad Flat Pack	20mm x 20mm	100	C
XC2C128-6TQ144C	0.5mm	46.1	7.9	Thin Quad Flat Pack	20mm x 20mm	100	C
XC2C128-7TQ144C	0.5mm	46.1	7.9	Thin Quad Flat Pack	20mm x 20mm	100	C
XC2C128-7VQ100I	0.5mm	47.5	12.5	Very Thin Quad Flat Pack	14mm x 14mm	80	I
XC2C128-7CP132I	0.5mm	72.4	15.7	Chip Scale Package	8mm x 8mm	100	I
XC2C128-7TQ144I	0.5mm	46.1	7.9	Thin Quad Flat Pack	20mm x 20mm	100	I

Notes:
1. C = Commercial (T_A = 0°C to +70°C)
2. I = Industrial (T_A = –40°C to +85°C)

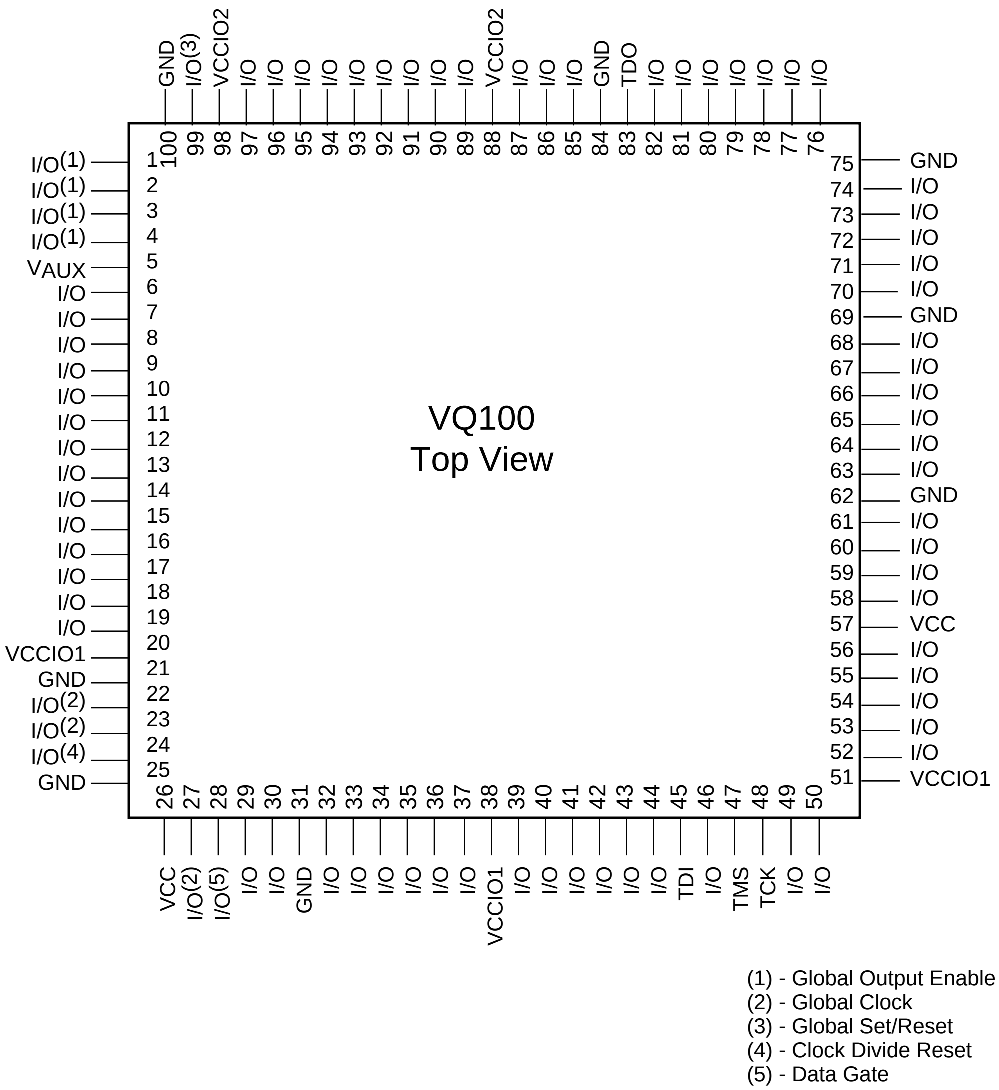


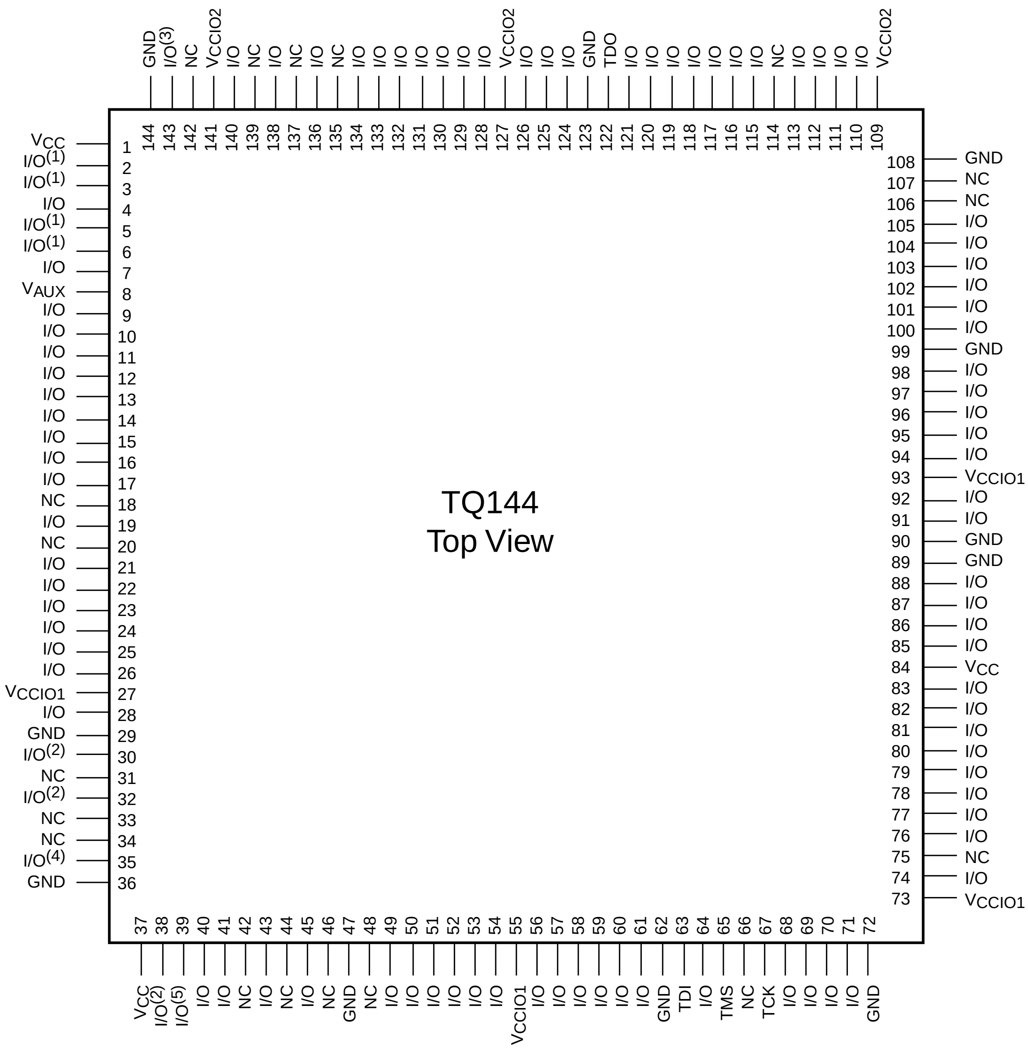
Figure 5: **VQ100 Very Thin Quad Flat Pack**

CP132
Bottom View

	1	2	3	4	5	6	7	8	9	10	11	12	13	14
P	VCC	I/O(5)	I/O	GND	I/O	I/O	VCCIO1	I/O	I/O	I/O	I/O	I/O	VCCIO1	I/O
N	GND	I/O(2)	I/O	NC	I/O	I/O	I/O	I/O	GND	TMS	I/O	GND	I/O	I/O
M	NC	I/O(4)	I/O	I/O	I/O	I/O	I/O	I/O	TDI	TCK	I/O	I/O	I/O	I/O
L	NC	I/O(2)	NC									I/O	I/O	I/O
K	I/O	GND	I/O(2)									VCC	I/O	I/O
J	I/O	I/O	VCCIO1									I/O	I/O	GND
H	I/O	I/O	I/O									I/O	I/O	GND
G	I/O	I/O	I/O									I/O	I/O	VCCIO1
F	I/O	I/O	I/O									I/O	I/O	I/O
E	I/O	I/O	I/O									I/O	I/O	GND
D	I/O	I/O	VAUX									I/O	I/O	I/O
C	I/O	I/O(1)	I/O(1)	VCCIO2	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	NC	I/O
B	I/O	I/O(1)	GND	I/O	I/O	I/O	I/O	I/O	TDO	NC	I/O	I/O	I/O	GND
A	I/O(1)	VCC	I/O(3)	I/O	I/O	I/O	VCCIO2	I/O	GND	I/O	I/O	I/O	I/O	VCCIO2

(1) - Global Output Enable
(2) - Global Clock
(3) - Global Set/Reset
(4) - Clock Divide Reset
(5) - DataGATE Enable

Figure 6: **CP132 Chip Scale Package**



(1) - Global Output Enable
(2) - Global Clock
(3) - Global Set/Reset
(4) - Clock Divide Reset
(5) - DataGATE Enable

Figure 7: **TQ144 Thin Quad Flat Pack**

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
9/01/02	1.0	Initial Xilinx release.