XC2C384 CoolRunner-II CPLD

DS095 (v1.1) September 23, 2002 **Advance Product Specification**

Features

- Optimized for 1.8V systems
  - As fast as 6.0 ns pin-to-pin delays
  - As low as 27 µA quiescent current
- Industry's best 0.18 micron CMOS CPLD
  - Optimized architecture for effective logic synthesis
  - Multi-voltage I/O operation — 1.5V to 3.3V
- Available in multiple package options
  - 144-pin TQFP with 118 user I/O
  - 208-pin PQFP with 173 user I/O
  - 256-ball FT (1.0mm) BGA with 212 user I/O
  - 324-ball FG (1.2mm) BGA with 240 user I/O
- Advanced system features
  - Fastest in system programming
    - 1.8V ISP using IEEE 1532 (JTAG) interface
  - IEEE1149.1 JTAG Boundary Scan Test
  - Optional Schmitt-trigger input (per pin)
  - Unsurpassed low power management
  - Four seperate output banks
  - Fast Zero Power™ (FZP) 100% CMOS product term generation
  - DataGATE enable (DGE) signal control
  - Flexible clocking modes
    - Optional DualEDGE triggered registers
    - Clock divider (divide by 2,4,6,8,10,12,14,16)
    - CoolCLOCK
  - Global signal options with macrocell control
    - Multiple global clocks with phase selection per macrocell
    - Multiple global output enables
    - Global set/reset
  - Advanced design security
  - Open-drain output option for Wired-OR and LED drive
  - Optional bus-hold, 3-state or weak pullup on selected I/O pins
  - Optional configurable grounds on unused I/Os
  - Mixed I/O voltages compatible with 1.5V, 1.8V, 2.5V, and 3.3V logic levels
    - SSTL2-1, SSTL3-1, and HSTL-1 I/O compatibility
  - Hot pluggable

Refer to the CoolRunner™-II family data sheet for architecture description.

Description

The CoolRunner-II 384-macrocell device is designed for both high performance and low power applications. This lends power savings to high-end communication equipment and high speed to battery operated devices. Due to the low power stand-by and dynamic operation, overall system reliability is improved

This device consists of twenty four Function Blocks inter-connected by a low power Advanced Interconnect Matrix (AIM). The AIM feeds 40 true and complement inputs to each Function Block. The Function Blocks consist of a 40 by 56 P-term PLA and 16 macrocells which contain numerous configuration bits that allow for combinational or registered modes of operation.

Additionally, these registers can be globally reset or preset and configured as a D or T flip-flop or as a D latch. There are also multiple clock signals, both global and local product term types, configured on a per macrocell basis. Output pin configurations include slew rate limit, bus hold, pull-up, open drain and programmable grounds. A Schmitt-trigger input is available on a per input pin basis. In addition to storing macrocell output states, the macrocell registers may be configured as direct input registers to store signals directly from input pins.

Clocking is available on a global or Function Block basis. Three global clocks are available for all Function Blocks as a synchronous clock source. Macrocell registers can be individually configured to power up to the zero or one state. A global set/reset control line is also available to asynchronously set or reset selected registers during operation. Additional local clock, synchronous clock-enable, asynchonous set/reset and output enable signals can be formed using product terms on a per-macrocell or per-Function Block basis.

A DualEDGE flip-flop feature is also available on a per macrocell basis. This feature allows high performance synchronous operation based on lower frequency clocking to help reduce the total power consumption of the device.

Circuitry has also been included to divide one externally supplied global clock (GCK2) by eight different selections. This yields divide by even and odd clock frequencies.

The use of the clock divide (division by 2) and DualEDGE flip-flop gives the resultant CoolCLOCK feature.

DataGATE is a method to selectively disable inputs of the CPLD that are not of interest during certain points in time.

By mapping a signal to the DataGATE function, lower power can be achieved due to reduction in signal switching.

Another feature that eases voltage translation is output banking. Four output banks are available on the CoolRunner-II 384 macrocell device that permits easy interfacing to 3.3V, 2.5V, 1.8V, and 1.5V devices.

The CoolRunner-II 384 macrocell CPLD is I/O compatible with various I/O standards (see Table 1). This device is also 1.5V I/O compatible with the use of Schmitt-trigger inputs.

Fast Zero Power Design Technology

Xilinx CoolRunner-II CPLDs are fabricated on a 0.18 micron process technology which is derived from leading edge FPGA product development. CoolRunner-II CPLDs employ Fast Zero Power™ (FZP), a design technique that makes use of CMOS technology in both the fabrication and design methodology. FZP design technology employs a cascade of CMOS gates to implement sum of products instead of traditional sense amplifier methodology. Due to this technology, Xilinx CoolRunner-II CPLDs achieve both high-performance and low power operation.

Supported I/O Standards

The CoolRunner-II 384 macrocell features LVCMOS, LVTTL, SSTL and HSTL I/O implementations. See Table 1 for I/O standard voltages. The LVTTL I/O standard is a general purpose EIA/JEDEC standard for 3.3V applications that use an LVTTL input buffer and Push-Pull output buffer. The LVCMOS standard is used in 3.3V, 2.5V, 1.8V applications. Both HSTL and SSTL I/O standards make use of a V_{REF} pin for JEDEC compliance. CoolRunner-II CPLDs are also 1.5V I/O compatible with the use of Schmitt-trigger inputs.

Table 1: **I/O Standards for XC2C384**

I/O Types	Output V_{CCIO}	Input V_{CCIO}	Input V_{REF}	Board Termination Voltage V_{TT}
LVTTL	3.3	3.3	N/A	N/A
LVCMOS33	3.3	3.3	N/A	N/A
LVCMOS25	2.5	2.5	N/A	N/A
LVCMOS18	1.8	1.8	N/A	N/A
1.5V I/O	1.5	1.5	N/A	N/A
HSTL-1	1.5	1.5	0.75	0.75
SSTL2-1	2.5	2.5	1.25	1.25
SSTL3-1	3.3	3.3	1.5	1.5

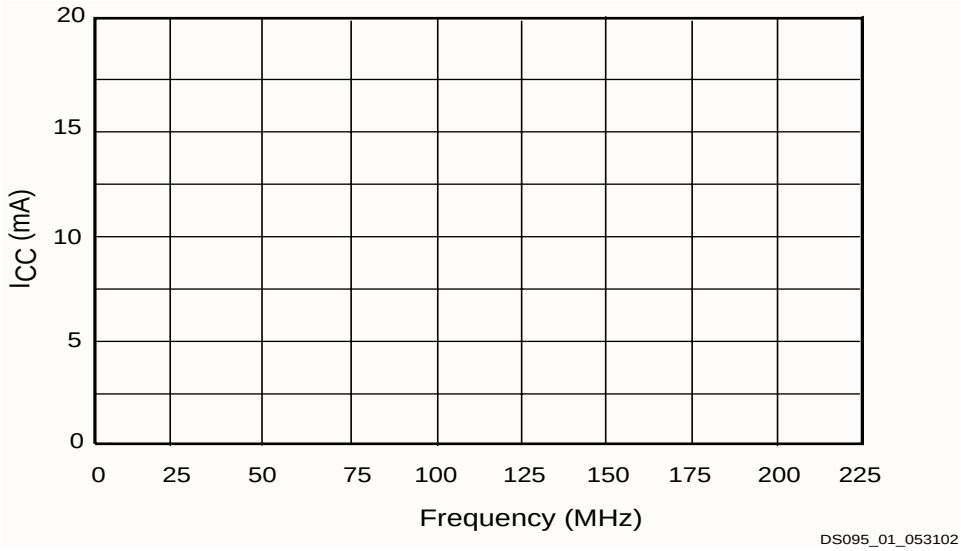


Figure 1: **I_{CC} vs Frequency**

Table 2: **I_{CC} vs Frequency (LVCMOS 1.8V T_A = 25°C)(1)**

	Frequency (MHz)									
	0	25	50	75	100	125	150	175	200	225
Typical -7, -10 I_{CC} (mA)										
Typical -6 I_{CC} (mA)										

Notes:
1. 16-bit up/down, resettable binary counter (one counter per function block).

Absolute Maximum Ratings

Symbol	Description	Value	Units
V_{CC}	Supply voltage relative to ground	–0.5 to 2.0	V
V_{CCIO}	Supply voltage for output drivers	–0.5 to 4.0	V
V_{JTAG}	JTAG input voltage limits	–0.5 to 4.0	V
V_{AUX}	JTAG input supply voltage	–0.5 to 4.0	V
V_{IN}	Input voltage relative to ground(1)	–0.5 to 4.0	V
V_{TS}	Voltage applied to 3-state output(1)	–0.5 to 4.0	V
T_{STG}	Storage Temperature (ambient)	–65 to +150	°C
T_{SOL}	Maximum Soldering temperature (10s @ 1/16in. = 1.5mm)	+260	°C
T_J	Junction Temperature	+150	°C

Notes:
1. Maximum DC undershoot below GND must be limited to either 0.5V or 10 mA, whichever is easiest to achieve. During transitions, the device pins may undershoot to –2.0v or overshoot to +4.5V, provided this over or undershoot lasts less than 10 ns and with the forcing current being limited to 200 mA.

Recommended Operating Conditions

Symbol	Parameter		Min	Max	Units
V_{CC}	Supply voltage for internal logic and input buffers	Commercial T_A = 0°C to +70°C	1.7	1.9	V
		Industrial T_A = –40°C to +85°C	1.7	1.9	V
V_{CCIO}	Supply voltage for output drivers @ 3.3V operation		3.0	3.6	V
	Supply voltage for output drivers @ 2.5V operation		2.3	2.7	V
	Supply voltage for output drivers @ 1.8V operation		1.7	1.9	V
	Supply voltage for output drivers @ 1.5V operation		1.4	1.6	V
V_{AUX}	JTAG programming		1.7	3.6	V

DC Electrical Characteristics (Over Recommended Operating Conditions)

Symbol	Parameter	Test Conditions	Min.	Max.	Units
I_{CCSB}	Standby current (-7, -10)	V_{CC} = 1.9V, V_{CCIO} = 3.6V	-	100	µA
I_{CCSB}	Standby current (-6)	V_{CC} = 1.9V, V_{CCIO} = 3.6V			mA
I_{CC} (1)	Dynamic current (-7, -10)	f = 1 MHz			mA
		f = 50 MHz			mA
I_{CC} (1)	Dynamic current (-6)	f = 1 MHz			mA
		f = 50 MHz			mA
C_{JTAG}	JTAG input capacitance	f = 1 MHz	-	10	pF
C_{CLK}	Global clock input capacitance	f = 1 MHz	-	12	pF
C_{IO}	I/O capacitance	f = 1 MHz	-	10	pF

Notes:
1. 16-bit up/down, resettable binary counter (one counter per function block).

LVCMOS and LVTTL 3.3V DC Voltage Specifications

Symbol	Parameter	Test Conditions	Min.	Max.	Units
V_{CCIO}	Input source voltage		3.0	3.6	V
V_{IH}	High level input voltage		2	3.9	V
V_{IL}	Low level input voltage		–0.3	0.8	V
V_{OH}	High level output voltage	I_{OH} = –8 mA, V_{CCIO} = 3V	V_{CCIO} – 0.4V	-	V
		I_{OH} = –0.1 mA, V_{CCIO} = 3V	V_{CCIO} – 0.2V	-	V
V_{OL}	Low level output voltage	I_{OL} = 8 mA, V_{CCIO} = 3V	-	0.4	V
		I_{OL} = 0.1 mA, V_{CCIO} = 3V	-	0.2	V
I_{IL}	Input leakage current	V_{IN} = 0V or V_{CCIO} to 3.9V	–1	1	µA
I_{IH}	I/O High-Z leakage	V_{IN} = 0V or V_{CCIO} to 3.9V	–1	1	µA

LVCMOS 2.5V DC Voltage Specifications

Symbol	Parameter	Test Conditions	Min.	Max.	Units
V_{CCIO}	Input source voltage		2.3	2.7	V
V_{IH}	High level input voltage		1.7	3.9	V
V_{IL}	Low level input voltage		–0.3	0.7	V
V_{OH}	High level output voltage	I_{OH} = –8 mA, V_{CCIO} = 2.3V	V_{CCIO} – 0.4V	-	V
		I_{OH} = –0.1 mA, V_{CCIO} = 2.3V	V_{CCIO} – 0.2V	-	V
V_{OL}	Low level output voltage	I_{OL} = 8 mA, V_{CCIO} = 2.3V	-	0.4	V
		I_{OL} = 0.1 mA, V_{CCIO} = 2.3V	-	0.2	V
I_{IL}	Input leakage current	V_{IN} = 0V or V_{CCIO} to 3.9V	–1	1	µA
I_{IH}	I/O High-Z leakage	V_{IN} = 0V or V_{CCIO} to 3.9V	–1	1	µA

LVCMOS 1.8V DC Voltage Specifications

Symbol	Parameter	Test Conditions	Min.	Max.	Units
V_{CCIO}	Input source voltage		1.7	1.9	V
V_{IH}	High level input voltage		0.65 * V_{CCIO}	3.9	V
V_{IL}	Low level input voltage		–0.3	0.35 * V_{CCIO}	V
V_{OH}	High level output voltage	I_{OH} = –8 mA, V_{CCIO} = 1.7V	V_{CCIO} – 0.45	-	V
		I_{OH} = –0.1 mA, V_{CCIO} = 1.7V	V_{CCIO} – 0.2	-	V
V_{OL}	Low level output voltage	I_{OL} = 8 mA, V_{CCIO} = 1.7V	-	0.45	V
		I_{OL} = 0.1 mA, V_{CCIO} = 1.7V	-	0.2	V
I_{IL}	Input leakage current	V_{IN} = 0 or V_{CCIO} to 3.9V	–1	1	µA
I_{IH}	I/O High-Z leakage	V_{IN} = 0 or V_{CCIO} to 3.9V	–1	1	µA

1.5V DC Voltage Specifications(1)

Symbol	Parameter	Test Conditions	Min.	Max.	Units
V_{CCIO}	Input source voltage		1.4	1.6	V
V_{T+}	Input hysteresis threshold voltage		0.5 * V_{CCIO}	0.8 * V_{CCIO}	V
V_{T-}			0.2 * V_{CCIO}	0.5 * V_{CCIO}	V
V_{OH}	High level output voltage	I_{OH} = –8 mA, V_{CCIO} = 1.4V	V_{CCIO} – 0.45	-	V
		I_{OH} = –0.1 mA, V_{CCIO} = 1.4V	V_{CCIO} – 0.2	-	V
V_{OL}	Low level output voltage	I_{OL} = 8 mA, V_{CCIO} = 1.4V	-	0.4	V
		I_{OL} = 0.1 mA, V_{CCIO} = 1.4V	-	0.2	V
I_{IL}	Input leakage current	V_{IN} = 0 or V_{CCIO} to 3.9V	–1	1	µA
I_{IH}	I/O High-Z leakage	V_{IN} = 0 or V_{CCIO} to 3.9V	–1	1	µA

Notes:
1. Hysteresis used on 1.5V inputs.

SSTL2-1 DC Voltage Specifications

Symbol	Parameter	Test Conditions	Min.	Typ	Max.	Units
V_{CCIO}	Input source voltage		2.3	2.5	2.7	V
$V_{REF(1)}$	Input reference voltage		1.15	1.25	1.35	V
$V_{TT(2)}$	Termination voltage		V_{REF} – 0.04	1.25	V_{REF} + 0.04	V
V_{IH}	High level input voltage		V_{REF} + 0.18	-	3.9	V
V_{IL}	Low level input voltage		–0.3	-	V_{REF} – 0.18	V
V_{OH}	High level output voltage	I_{OH} = –8 mA, V_{CCIO} = 2.3V	V_{CCIO} – 0.62	-	-	V
V_{OL}	Low level output voltage	I_{OL} = 8 mA, V_{CCIO} = 2.3V	-	-	0.54	V
I_{IL}	Input leakage current	V_{IN} = 0V or V_{CCIO} to 3.9V	–1	-	1	µA
I_{IH}	I/O High-Z leakage	V_{IN} = 0V or V_{CCIO} to 3.9V	–1	-	1	µA

Notes:
1. V_{REF} should track the variations in V_{CCIO}, also peak to peak ac noise win V_{REF} may not exceed ±2% V_{REF}
2. V_{TT} of transmitting device must track V_{REF} of receiving devices

SSTL3-1 DC Voltage Specifications

Symbol	Parameter	Test Conditions	Min.	Typ	Max.	Units
V_{CCIO}	Input source voltage		3.0	3.3	3.6	V
$V_{REF(1)}$	Input reference voltage		1.3	1.5	1.7	V
$V_{TT(2)}$	Termination voltage		V_{REF} – 0.05	1.5	V_{REF} + 0.05	V
V_{IH}	High level input voltage		V_{REF} + 0.2	-	V_{CCIO} + 0.3	V
V_{IL}	Low level input voltage		–0.3	-	V_{REF} – 0.2	V
V_{OH}	High level output voltage	I_{OH} = –8 mA, V_{CCIO} = 3V	V_{CCIO} – 1.1	-	-	V
V_{OL}	Low level output voltage	I_{OL} = 8 mA, V_{CCIO} = 3V	-	-	0.7	V
I_{IL}	Input leakage current	V_{IN} = 0V or V_{CCIO} to 3.9V	–1	-	1	µA
I_{IH}	I/O High-Z leakage	V_{IN} = 0V or V_{CCIO} to 3.9V	–1	-	1	µA

Notes:
1. V_{REF} should track the variations in V_{CCIO}, also peak to peak ac noise win V_{REF} may not exceed ±2% V_{REF}
2. V_{TT} of transmitting device must track V_{REF} of receiving devices

HSTL1 DC Voltage Specifications

Symbol	Parameter	Test Conditions	Min.	Typ	Max.	Units
V_{CCIO}	Input source voltage		1.4	1.5	1.6	V
$V_{REF(1)}$	Input reference voltage		0.68	0.75	0.90	V
$V_{TT(2)}$	Termination voltage		-	V_{CCIO} * 0.5	-	V
V_{IH}	High level input voltage		V_{REF} + 0.1	-	1.9	V
V_{IL}	Low level input voltage		–0.3	-	V_{REF} – 0.1	V
V_{OH}	High level output voltage	I_{OH} = –8 mA, V_{CCIO} = 1.7V	V_{CCIO} – 0.4	-	-	V
V_{OL}	Low level output voltage	I_{OL} = 8 mA, V_{CCIO} = 1.7V	-	-	0.4	V
I_{IL}	Input leakage current	V_{IN} = 0 or V_{CCIO} to 3.9V	–10	-	10	µA
I_{IH}	I/O High-Z leakage	V_{IN} = 0 or V_{CCIO} to 3.9V	–10	-	10	µA

Notes:
1. V_{REF} should track the variations in V_{CCIO}, also peak to peak ac noise win V_{REF} may not exceed ±2% V_{REF}
2. V_{TT} of transmitting device must track V_{REF} of receiving devices

AC Electrical Characteristics Over Recommended Operating Conditions

Symbol	Parameter	-6		-7		-10		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
T_{PD1}	Propagation delay single p-term	-	5.7	-	7.1	-	9.2	ns
T_{PD2}	Propagation delay OR array	-	6.0	-	7.5	-	10.0	ns
T_{SUF}	Fast input register set-up time	2.2	-	2.4	-	2.7	-	ns
T_{SU1}	Setup time fast (single p-term)	2.3	-	2.6	-	3.1	-	ns
T_{SU2}	Setup time (OR array)	2.6	-	3.0	-	3.9	-	ns
T_{HF}	Fast input register hold time	0	-	0	-	0	-	ns
T_{H}	Hold time (OR array or p-term)	0	-	0	-	0	-	ns
T_{CO}	Clock to output	-	4.4	-	5.8	-	7.9	ns
F_{TOGGLE}	Internal toggle rate(1)	-	416	-	250	-	166	MHz
$F_{SYSTEM1}$	Maximum system frequency(2)	-	217	-	179	-	128	MHz
$F_{SYSTEM2}$	Maximum system frequency(2)	-	204	-	167	-	116	MHz
F_{EXT1}	Maximum external frequency(3)	-	149	-	119	-	91	MHz
F_{EXT2}	Maximum external frequency(3)	-	143	-	114	-	85	MHz
T_{PSUF}	Fast input register p-term clock setup time	1.0	-	1.1	-	1.3	-	ns
T_{PSU1}	P-term clock setup time (single p-term)	1.1	-	1.3	-	1.7	-	ns
T_{PSU2}	P-term clock setup time (OR array)	1.4	-	1.7	-	2.5	-	ns
T_{PHF}	Fast input register p-term clock hold time	0.5	-	0.9	-	1.3	-	ns
T_{PH}	P-term clock hold	0.4	-	0.7	-	0.9	-	ns
T_{PCO}	P-term clock to output	-	5.6	-	7.1	-	9.3	ns
T_{OE}/T_{OD}	Global OE to output enable/disable	-	5.5	-	7.0	-	9.2	ns
T_{POE}/T_{POD}	P-term OE to output enable/disable	-	6.5	-	8.0	-	10.2	ns
T_{MOE}/T_{MOD}	Macrocell driven OE to output enable/disable	-	7.1	-	9.1	-	12.5	ns
T_{PAO}	P-term set/reset to output valid	-	7.4	-	8.9	-	11.6	ns
T_{AO}	Global set/reset to output valid	-	7.2	-	9.0	-	11.5	ns
T_{SUEC}	Register clock enable setup time	2.4	-	2.7	-	3.2	-	ns
T_{HEC}	Register clock enable hold time	0	-	0	-	0	-	ns
T_{CW}	Global clock pulse width High or Low	1.2	-	2.0	-	3.0	-	ns
T_{PCW}	P-term pulse width High or Low	6.0	-	7.5	-	10.0	-	ns
T_{DGSU}	Set-up before DataGATE latch assertion	7.0		9.0		10.0		ns
T_{DGHO}	Hold to DataGATE latch assertion	7.0		9.0		10.0		ns
T_{DGR}	DataGATE recovery to new data		7.0		9.0		11.0	ns
T_{DGW}	DataGATE high pulse width	2.5		3.0		5.0		ns
T_{CDRSU}	CDRST setup time before falling edge GCLK2	1.2		1.7		2.5		ns
T_{CDRHO}	Hold time CDRST after falling edge GCLK2	0		0		0		ns
T_{CONFIG}	Configuration time							µs

Notes:

1. F_{TOGGLE} ($1/2*T_{CW}$) is the maximum frequency of a T flip-flop with output enabled
2. $F_{SYSTEM1}$ ($1/T_{CYCLE}$) is the internal operating frequency for a device with 16-bit resettable binary counter through one p-term per macrocell while $F_{SYSTEM2}$ is through the OR array (one counter per function block)
3. $F_{EXT1}(1/T_{SU1}+T_{CO})$ is the maximum external frequency using one p-term while F_{EXT2} is through the OR array

Internal Timing Parameters

Symbol	Parameter[1]	-6		-7		-10		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
Buffer Delays								
T_{IN}	Input buffer delay	-	2.5	-	3.1	-	3.8	ns
T_{FIN}	Fast data register input delay	-	2.8	-	3.4	-	4.2	ns
T_{GCK}	Global Clock buffer delay	-	1.8	-	2.4	-	3.3	ns
T_{GSR}	Global set/reset buffer delay	-	2.8	-	3.8	-	4.6	ns
T_{GTS}	Global 3-state buffer delay	-	2.0	-	2.7	-	3.7	ns
T_{OUT}	Output buffer delay	-	2.4	-	3.0	-	3.9	ns
T_{EN}	Output buffer enable/disable delay	-	3.5	-	4.3	-	5.5	ns
P-term Delays								
T_{CT}	Control term delay	-	0.5	-	0.6	-	0.9	ns
T_{LOGI1}	Single P-term delay adder	-	0.4	-	0.5	-	0.8	ns
T_{LOGI2}	Multiple P-term delay adder	-	0.3	-	0.4	-	0.8	ns
Macrocell Delay								
T_{PDI}	Input to output valid	-	0.4	-	0.5	-	0.7	ns
T_{SUI}	Setup before clock	1.2	-	1.4	-	1.8	-	ns
T_{HI}	Hold after clock	0	-	0	-	0	-	ns
T_{ECSU}	Enable clock setup time	1.2	-	1.4	-	1.8	-	ns
T_{ECHO}	Enable clock hold time	0	-	0	-	0	-	ns
T_{COI}	Clock to output valid	-	0.2	-	0.4	-	0.7	ns
T_{AOI}	Set/reset to output valid	-	2.0	-	2.2	-	3.0	ns
T_{CDBL}	Clock doubler delay	-	0	-	0	-	0	ns
Feedback Delays								
T_{F}	Feedback delay	-	2.8	-	3.3	-	4.5	ns
T_{OEM}	Macrocell to global OE delay	-	1.6	-	2.0	-	3.0	ns
I/O Standard Time Adder Delays 1.5V CMOS								
T_{HYS15}	Hysteresis input adder	-	2.0	-	3.0	-	4.0	ns
T_{OUT15}	Output adder	-	0.5	-	0.8	-	1.0	ns
T_{SLEW15}	Output slew rate adder	-	2.0	-	3.0	-	4.0	ns
I/O Standard Time Adder Delays 1.8V CMOS								
T_{IN18}	Standard input adder	-	0	-	0	-	0	ns
T_{HYS18}	Hysteresis input adder	-	2.0	-	3.0	-	4.0	ns
T_{OUT18}	Output adder	-	0	-	0	-	0	ns
T_{SLEW}	Output slew rate adder	-	2.0	-	3.0	-	4.0	ns
I/O Standard Time Adder Delays 2.5V CMOS								
T_{IN25}	Standard input adder	-	0.5	-	0.8	-	1.0	ns
T_{HYS25}	Hysteresis input adder	-	1.5	-	2.5	-	3.0	ns
T_{OUT25}	Output adder	-	1.5	-	2.5	-	3.0	ns
T_{SLEW25}	Output slew rate adder	-	2.0	-	3.0	-	4.0	ns

Internal Timing Parameters *(Continued)*

Symbol	Parameter[1]	-6		-7		-10		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
I/O Standard Time Adder Delays 3.3V CMOS/TTL								
T_{IN33}	Standard input adder	-	0.7	-	1.0	-	2.0	ns
T_{HYS33}	Hysteresis input adder	-	1.0	-	2.0	-	3.0	ns
T_{OUT33}	Output adder	-	1.0	-	2.0	-	3.0	ns
T_{SLEW33}	Output slew rate adder	-	2.0	-	3.0	-	4.0	ns
I/O Standard Time Adder Delays HSTL, SSTL								
SSTL2-1	Input adder to TIN, TFIN, TGCK, TGSR,TGTS	-	1.5	-	1.8	-	2.5	ns
	Output adder to TOUT	-	0	-	0	-	0	ns
SSTL3-1	Input adder to TIN, TFIN, TGCK, TGSR,TGTS	-	1.5	-	1.8	-	2.5	ns
	Output adder to TOUT	-	0	-	0	-	0	ns
HSTL-1	Input adder to TIN, TFIN, TGCK, TGSR,TGTS	-	1.5	-	1.8	-	2.5	ns
	Output adder to TOUT	-	0	-	0	-	0	ns

Notes:
1. 1.5 ns input pin signal rise/fall.

Switching Characteristics

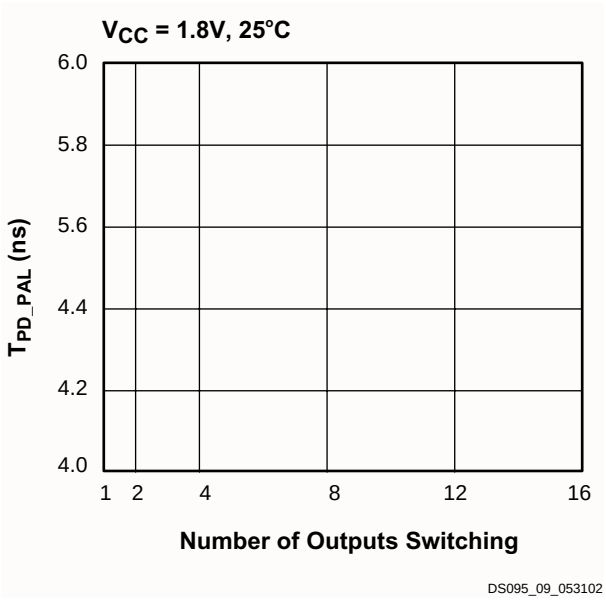
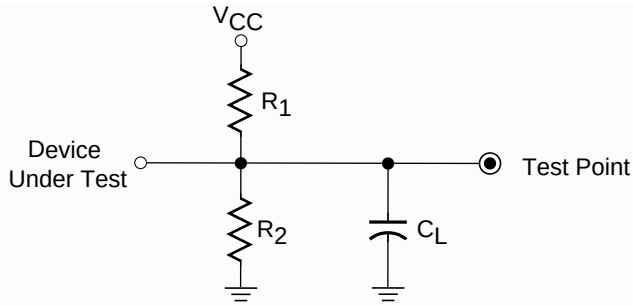


Figure 2: **Typical I/V Curve for XC2C384**

Switching Test Conditions



Output Type	R_1	R_2	C_L
LVTTL33	268Ω	235Ω	35 pF
LVCMOS33	275Ω	275Ω	35 pF
LVCMOS25	188Ω	188Ω	35 pF
LVCMOS18	112.5Ω	112.5Ω	35 pF
LVCMOS15	150Ω	150Ω	35 pF

Notes:
1. C_L includes test fixtures and probe capacitance.
2. 1.5 nsec maximum rise/fall times on inputs.

DS092_03_092302

Figure 3: **AC Load Circuit**

Pin Descriptions

Function Block	Macro-cell	TQ144	PQ208	FT256	FG324	I/O Bank
1	1	-	2	B3	C3	2
1	2	-	208	B4	A1	2
1(GSR)	3	143	206	C4	A2	2
1	4	142	205	A2	B3	2
1	5	-	-	-	C4	2
1	6	-	-	-	-	-
1	7	-	-	-	-	-
1	8	-	-	-	-	-
1	9	-	-	-	-	-
1	10	-	-	-	-	-
1	11	-	-	-	-	-
1	12	140	203	C5	B4	2
1	13	139	202	A3	C5	2
1	14	-	201	-	B5	2
1	15	-	200	E7	A3	2
1	16	-	199	-	A4	2
2(GTS2)	1	2	3	D3	D3	2
2	2	-	4	C3	B2	2
2(GTS3)	3	3	5	E3	B1	2
2	4	4	6	B2	C2	2
2(GTS0)	5	5	7	D4	C1	2
2	6	-	-	-	-	-
2	7	-	-	-	-	-
2	8	-	-	-	-	-
2	9	-	-	-	-	-
2	10	-	-	-	-	-
2	11	-	-	-	-	-
2	12	-	-	A1	D2	2
2	13	-	8	D2	F4	2
2	14	-	-	C2	E2	2
2(GTS1)	15	6	9	E5	E1	2
2	16	7	10	B1	F2	2

Pin Descriptions *(Continued)*

Function Block	Macro-cell	TQ144	PQ208	FT256	FG324	I/O Bank
3	1	-	198	A4	D6	2
3	2	-	197	-	A5	2
3	3	138	196	C6	C6	2
3	4	137	195	B5	B6	2
3	5	136	194	D6	A6	2
3	6	-	-	-	-	-
3	7	-	-	-	-	-
3	8	-	-	-	-	-
3	9	-	-	-	-	-
3	10	-	-	-	-	-
3	11	-	-	-	-	-
3	12	135	193	A5	D7	2
3	13	-	192	E8	C7	2
3	14	-	-	B6	B7	2
3	15	-	191	C7	A7	2
3	16	134	-	A6	D8	2
4	1	9	12	E4	G4	2
4	2	10	-	C1	G3	2
4	3	11	14	E2	G2	2
4	4	12	15	F2	G1	2
4	5	-	16	E6	H4	2
4	6	-	-	-	-	-
4	7	-	-	-	-	-
4	8	-	-	-	-	-
4	9	-	-	-	-	-
4	10	-	-	-	-	-
4	11	-	-	-	-	-
4	12	-	17	F3	H3	2
4	13	-	18	D1	H2	2
4	14	-	19	G4	H1	2
4	15	-	20	E1	J3	2
4	16	-	21	G3	J2	2

Pin Descriptions *(Continued)*

Function Block	Macro-cell	TQ144	PQ208	FT256	FG324	I/O Bank
5	1	-	-	D7	C8	2
5	2	133	-	B7	B8	2
5	3	132	-	E9	A8	2
5	4	-	189	A7	D9	2
5	5	-	188	D8	C9	2
5	6	-	-	-	-	-
5	7	-	-	-	-	-
5	8	-	-	-	-	-
5	9	-	-	-	-	-
5	10	-	-	-	-	-
5	11	-	-	-	-	-
5	12	-	187	B8	B9	2
5	13	131	186	C8	A9	2
5	14	-	185	A8	D10	2
5	15	130	184	E11	C10	2
5	16	129	183	E10	B10	2
6	1	-	22	G2	J1	2
6	2	13	-	F5	K3	2
6	3	14	23	F1	K2	2
6	4	15	-	G5	K1	2
6	5	-	-	H2	L1	2
6	6	-	-	-	-	-
6	7	-	-	-	-	-
6	8	-	-	-	-	-
6	9	-	-	-	-	-
6	10	-	-	-	-	-
6	11	-	-	-	-	-
6	12	-	-	H4	L3	2
6	13	16	-	G1	L2	2
6	14	17	-	H3	M1	2
6	15	-	-	H1	M2	2
6	16	18	25	H5	M3	2

Pin Descriptions *(Continued)*

Function Block	Macro-cell	TQ144	PQ208	FT256	FG324	I/O Bank
7(CDRST)	1	35	51	P2	AB2	1
7	2	-	50	N3	AA2	1
7	3	-	49	R1	AA1	1
7	4	34	48	N4	W4	1
7	5	33	47	N2	Y2	1
7	6	-	-	-	-	-
7	7	-	-	-	-	-
7	8	-	-	-	-	-
7	9	-	-	-	-	-
7	10	-	-	-	-	-
7	11	-	-	-	-	-
7(GCK1)	12	32	46	M3	Y1	1
7	13	-	-	P1	W2	1
7	14	31	45	M4	W1	1
7(GCK0)	15	30	44	M2	V3	1
7	16	-	43	L3	U4	1
8	1	-	54	P4	Y4	1
8(GCK2)	2	38	55	P5	AB3	1
8	3	-	56	R2	AA4	1
8	4	-	57	T1	Y5	1
8(DGE)	5	39	58	T2	AA5	1
8	6	-	-	-	-	-
8	7	-	-	-	-	-
8	8	-	-	-	-	-
8	9	-	-	-	-	-
8	10	-	-	-	-	-
8	11	-	-	-	-	-
8	12	-	-	-	AB4	1
8	13	40	60	N5	W6	1
8	14	41	-	-	AB5	1
8	15	42	61	R4	Y6	1
8	16	43	-	M5	AA6	1

Pin Descriptions *(Continued)*

Function Block	Macro-cell	TQ144	PQ208	FT256	FG324	I/O Bank
9	1	-	41	N1	V2	1
9	2	28	40	L4	V1	1
9	3	-	39	M1	U3	1
9	4	-	38	L5	U2	1
9	5	-	37	K4	U1	1
9	6	-	-	-	-	-
9	7	-	-	-	-	-
9	8	-	-	-	-	-
9	9	-	-	-	-	-
9	10	-	-	-	-	-
9	11	--	-	-	-	-
9	12	-	36	L2	T4	1
9	13	-	35	K3	T3	1
9	14	-	34	L1	T2	1
9	15	26	32	-	T1	1
9	16	25	-	-	R4	1
10	1	44	62	-	AB6	1
10	2	45	63	R5	W7	1
10	3	-	-	-	Y7	1
10	4	46	64	R6	AA7	1
10	5	-	65	N6	AB7	1
10	6	-	-	-	-	-
10	7	-	-	-	-	-
10	8	-	-	-	-	-
10	9	-	-	-	-	-
10	10	-	-	-	-	-
10	11	-	-	-	-	-
10	12	-	66	R3	W8	1
10	13	-	67	M6	Y8	1
10	14	48	69	-	AA8	1
10	15	49	70	T3	AB8	1
10	16	50	71	P6	Y9	1

Pin Descriptions *(Continued)*

Function Block	Macro-cell	TQ144	PQ208	FT256	FG324	I/O Bank
11	1	24	31	K5	R3	1
11	2	23	-	K2	R2	1
11	3	22	30	J4	R1	1
11	4	21	29	K1	P4	1
11	5	20	28	J3	P3	1
11	6	-	-	-	-	-
11	7	-	-	-	-	-
11	8	-	-	-	-	-
11	9	-	-	-	-	-
11	10	-	-	-	-	-
11	11	-	-	-	-	-
11	12	19	27	J2	P2	1
11	13	-	-	J5	P1	1
11	14	-	-	J1	N3	1
11	15	-	-	-	N2	1
11	16	-	-	-	N1	1
12	1	51	72	T4	AA9	1
12	2	52	73	P7	AB9	1
12	3	53	74	T5	W10	1
12	4	-	75	N7	Y10	1
12	5	54	76	R7	AA10	1
12	6	-	-	-	-	-
12	7	-	-	-	-	-
12	8	-	-	-	-	-
12	9	-	-	-	-	-
12	10	-	-	-	-	-
12	11	-	-	-	-	-
12	12	-	77	M7	AB10	1
12	13	-	-	-	AB11	1
12	14	-	-	-	W11	1
12	15	-	-	-	AA11	1
12	16	-	78	T6	Y11	1

Pin Descriptions *(Continued)*

Function Block	Macro-cell	TQ144	PQ208	FT256	FG324	I/O Bank
13	1	-	-	B16	C21	4
13	2	-	-	G11	C20	4
13	3	112	160	C14	B22	4
13	4	113	161	B15	B21	4
13	5	-	-	A16	A22	4
13	6	-	-	-	-	-
13	7	-	-	-	-	-
13	8	-	-	-	-	-
13	9	-	-	-	-	-
13	10	-	-	-	-	-
13	11	-	-	-	-	-
13	12	114	162	B13	A21	4
13	13	115	163	B14	B20	4
13	14	-	-	C13	C19	4
13	15	-	-	A15	B19	4
13	16	-	164	C12	C18	4
14	1	111	159	D14	D19	4
14	2	110	158	C15	D20	4
14	3	107	155	G12	C22	4
14	4	106	154	D15	D21	4
14	5	105	153	E14	D22	4
14	6	-	-	-	-	-
14	7	-	-	-	-	-
14	8	-	-	-	-	-
14	9	-	-	-	-	-
14	10	-	-	-	-	-
14	11	-	-	-	-	-
14	12	-	-	C16	E20	4
14	13	104	152	F14	F19	4
14	14	-	151	D16	E21	4
14	15	-	-	F13	E22	4
14	16	-	150	E15	F20	4

Pin Descriptions *(Continued)*

Function Block	Macro-cell	TQ144	PQ208	FT256	FG324	I/O Bank
15	1	-	-	B12	B18	4
15	2	116	165	D13	A19	4
15	3	-	166	A14	D17	4
15	4	-	-	E13	A18	4
15	5	117	167	A13	C17	4
15	6	-	-	-	-	-
15	7	-	-	-	-	-
15	8	-	-	-	-	-
15	9	-	-	-	-	-
15	10	-	-	-	-	-
15	11	-	-	-	-	-
15	12	-	168	C11	B17	4
15	13	118	169	A12	D16	4
15	14	-	-	B11	C16	4
15	15	119	170	D11	B16	4
15	16	120	171	A11	D15	4
16	1	103	149	G13	F21	4
16	2	-	148	F15	F22	4
16	3	102	147	G14	G19	4
16	4	-	146	E16	G20	4
16	5	-	-	H12	G21	4
16	6	-	-	-	-	-
16	7	-	-	-	-	-
16	8	-	-	-	-	-
16	9	-	-	-	-	-
16	10	-	-	-	-	-
16	11	-	-	-	-	-
16	12	-	145	F16	G22	4
16	13	-	-	H16	H19	4
16	14	101	144	-	H21	4
16	15	-	-	-	H22	4
16	16	100	143	-	J19	4

Pin Descriptions *(Continued)*

Function Block	Macro-cell	TQ144	PQ208	FT256	FG324	I/O Bank
17	1	-	173	D10	C15	4
17	2	121	174	B10	B15	4
17	3	-	175	E12	D14	4
17	4	-	-	-	B14	4
17	5	-	-	F12	C13	4
17	6	-	-	-	-	-
17	7	-	-	-	-	-
17	8	-	-	-	-	-
17	9	-	-	-	-	-
17	10	-	-	-	-	-
17	11	-	-	-	-	-
17	12	124	178	B9	A13	4
17	13	125	179	C9	D12	4
17	14	126	180	C10	C12	4
17	15	-	-	A9	B11	4
17	16	128	182	D9	A10	4
18	1	-	-	G15	J20	4
18	2	-	142	-	J21	4
18	3	98	140	-	J22	4
18	4	97	139	H13	K19	4
18	5	96	138	G16	K20	4
18	6	-	-	-	-	-
18	7	-	-	-	-	-
18	8	-	-	-	-	-
18	9	-	-	-	-	-
18	10	-	-	-	-	-
18	11	-	-	-	-	-
18	12	95	137	H14	K21	4
18	13	94	136	H15	K22	4
18	14	-	135	J12	L19	4
18	15	-	134	K12	L20	4
18	16	-	-	J16	L21	4

Pin Descriptions *(Continued)*

Function Block	Macro-cell	TQ144	PQ208	FT256	FG324	I/O Bank
19	1	-	103	P13	AA22	3
19	2	-	-	P14	Y20	3
19	3	74	106	P15	Y21	3
19	4	75	107	R15	W20	3
19	5	76	108	T16	W21	3
19	6	-	-	-	-	-
19	7	-	-	-	-	-
19	8	-	-	-	-	-
19	9	-	-	-	-	-
19	10	-	-	-	-	-
19	11	-	-	-	-	-
19	12	77	109	N14	Y22	3
19	13	78	110	R16	W22	3
19	14	79	111	N15	V20	3
19	15	-	112	M15	V21	3
19	16	-	113	M13	U19	3
20	1	71	102	R13	AB22	3
20	2	70	101	N13	AA21	3
20	3	69	100	R14	AB21	3
20	4	68	99	T15	W19	3
20	5	66	97	R12	AA20	3
20	6	-	-	-	-	-
20	7	-	-	-	-	-
20	8	-	-	-	-	-
20	9	-	-	-	-	-
20	10	-	-	-	-	-
20	11	-	-	-	-	-
20	12	-	-	T14	Y18	3
20	13	64	95	N11	AA19	3
20	14	-	-	P11	Y17	3
20	15	-	-	M11	AA18	3
20	16	-	-	T13	AB18	3

Pin Descriptions *(Continued)*

Function Block	Macro-cell	TQ144	PQ208	FT256	FG324	I/O Bank
21	1	80	114	P16	V22	3
21	2	-	115	N16	U20	3
21	3	81	116	L14	U21	3
21	4	-	117	M14	U22	3
21	5	-	118	L15	T19	3
21	6	-	-	-	-	-
21	7	-	-	-	-	-
21	8	-	-	-	-	-
21	9	-	-	-	-	-
21	10	-	-	-	-	-
21	11	-	-	-	-	-
21	12	82	119	L13	T20	3
21	13	-	120	M12	T21	3
21	14	-	121	M16	T22	3
21	15	83	122	K14	R21	3
21	16	-	123	-	R22	3
22	1	-	-	N10	AA17	3
22	2	61	91	T12	AB17	3
22	3	-	90	P10	Y16	3
22	4	-	89	T11	AA16	3
22	5	-	-	R10	AB16	3
22	6	-	-	-	-	-
22	7	-	-	-	-	-
22	8	-	-	-	-	-
22	9	-	-	-	-	-
22	10	-	-	-	-	-
22	11	-	-	-	-	-
22	12	60	88	M10	W15	3
22	13	-	87	T10	Y15	3
22	14	59	86	M9	AA15	3
22	15	-	85	R9	AB15	3
22	16	-	-	P9	W14	3

Pin Descriptions *(Continued)*

Function Block	Macro-cell	TQ144	PQ208	FT256	FG324	I/O Bank
23	1	-	-	L16	P20	3
23	2	-	125	K15	P21	3
23	3	85	126	L12	N19	3
23	4	86	127	-	N21	3
23	5	87	-	K16	N22	3
23	6	-	-	-	-	-
23	7	-	-	-	-	-
23	8	-	-	-	-	-
23	9	-	-	-	-	-
23	10	-	-	-	-	-
23	11	-	-	-	-	-
23	12	88	128	J14	M22	3
23	13	91	-	J15	M19	3
23	14	92	131	J13	M20	3
23	15	-	-	-	M21	3
23	16	-	-	-	L22	3
24	1	-	-	N9	Y14	3
24	2	58	84	T9	AA14	3
24	3	-	-	-	AB14	3
24	4	-	83	-	Y13	3
24	5	-	82	M8	AA13	3
24	6	-	-	-	-	-
24	7	-	-	-	-	-
24	8	-	-	-	-	-
24	9	-	-	-	-	-
24	10	-	-	-	-	-
24	11	-	-	-	-	-
24	12	57	-	T8	AB13	3
24	13	-	-	P8	W12	3
24	14	56	80	R8	Y12	3
24	15	-	-	T7	AA12	3
24	16	-	-	N8	AB12	3

Notes:

1. GTS = global output enable, GSR = global reset/set, GCK = global clock, CDRST = clock divide reset, DGE = DataGATE enable.

XC2C384 JTAG, Power/Ground, No Connect Pins and Total User I/O

Pin Type	TQ144	PQ208	FT256	FG324
TCK	67	98	P12	Y19
TDI	63	94	R11	AB19
TDO	122	176	A10	C14
TMS	65	96	N12	AB20
V_{AUX} (JTAG supply voltage)	8	11	F4	F1
Power internal (V_{CC})	1, 37, 84	1, 53, 124	P3, K13, D12, D5	AA3, N20, A20, D4, E3
Power Bank 1 I/O (V_{CCIO1})	27, 55	33, 59, 79	J6, K6, L7, L8	M9, N9, P10, P11
Power Bank 2 I/O (V_{CCIO2})	141	26, 204	F7, F8, G6, H6	J10, J11, K9, L9
Power Bank 3 I/O (V_{CCIO3})	73, 93	92, 105, 132	J11, K11, L10, L9	M14, N14, P12, P13
Power Bank 4 I/O (V_{CCIO4})	109, 127	133, 157, 172, 181	F10, F9, H11	J12, J13, K14, L14
Ground	29, 36, 47, 62, 72, 89, 90, 99, 108, 123, 144	13, 24, 42, 52, 68, 81, 93, 104, 129, 130, 141, 156, 177, 190, 207	F11, F6, G10, G7, G8, G9, H10, H7, H8, H9, J10, J7, J8, J9, K10, K7, K8, K9, L11, L6	D5, D18, E4, E19, J9, J14, K10, K11, K12, K13, L10, L11, L12, L13, M10, M11, M12, M13, N10, N11, N12, N13, P9, P14, V4, V19, W5, W18
No connects	-	-		A11, A12, A14, A15, A16, A17, B12, B13, C11, D1, D11, D13, F3, H20, J4, K4, L4, M4, N4, P19, P22, R19, R20, W3, W9, W13, W16, W17, Y3, AB1
Total user I/O (includes dual function pins)	118	173	212	240

Ordering Information

Part Number	Pin/Ball Spacing	θ_{JA} (C/Watt)	θ_{JC} (C/Watt)	Package Type	Package Dimensions	I/O	Commercial (C) Industrial (I)
XC2C384-6TQ144C	0.5mm	34.1	6.5	Thin Quad Flat Pack	20mm x 20mm	118	C
XC2C384-7TQ144C	0.5mm	34.1	6.5	Thin Quad Flat Pack	20mm x 20mm	118	C
XC2C384-10TQ144C	0.5mm	34.1	6.5	Thin Quad Flat Pack	20mm x 20mm	118	C
XC2C384-6PQ208C	0.5mm	36.1	8.4	Plastic Quad Flat Pack	28mm x 28mm	173	C
XC2C384-7PQ208C	0.5mm	36.1	8.4	Plastic Quad Flat Pack	28mm x 28mm	173	C
XC2C384-10PQ208C	0.5mm	36.1	8.4	Plastic Quad Flat Pack	28mm x 28mm	173	C
XC2C384-6FT256C	1.0mm	33.5	5.5	Fine Pitch Thin BGA	17mm x 17mm	212	C
XC2C384-7FT256C	1.0mm	33.5	5.5	Fine Pitch Thin BGA	17mm x 17mm	212	C
XC2C384-10FT256C	1.0mm	33.5	5.5	Fine Pitch Thin BGA	17mm x 17mm	212	C
XC2C384-6FG324C	1.0mm	39.3	5.3	Fine Pitch BGA	23mm x 23mm	240	C
XC2C384-7FG324C	1.0mm	39.3	5.3	Fine Pitch BGA	23mm x 23mm	240	C
XC2C384-10FG324C	1.0mm	39.3	5.3	Fine Pitch BGA	23mm x 23mm	240	C
XC2C384-10TQ144I	0.5mm	34.1	6.5	Plastic Quad Flat Pack	28mm x 28mm	118	I
XC2C384-10PQ208I	0.5mm	36.1	8.4	Plastic Quad Flat Pack	28mm x 28mm	173	I
XC2C384-10FT256I	1.0mm	33.5	5.5	Fine Pitch Thin BGA	17mm x 17mm	212	I
XC2C384-10FG324I	1.0mm	39.3	5.3	Fine Pitch BGA	23mm x 23mm	240	I

Notes: Note:

1. C = Commercial (T_A = 0°C to +70°C); I = Industrial (T_A = –40°C to +85°C).

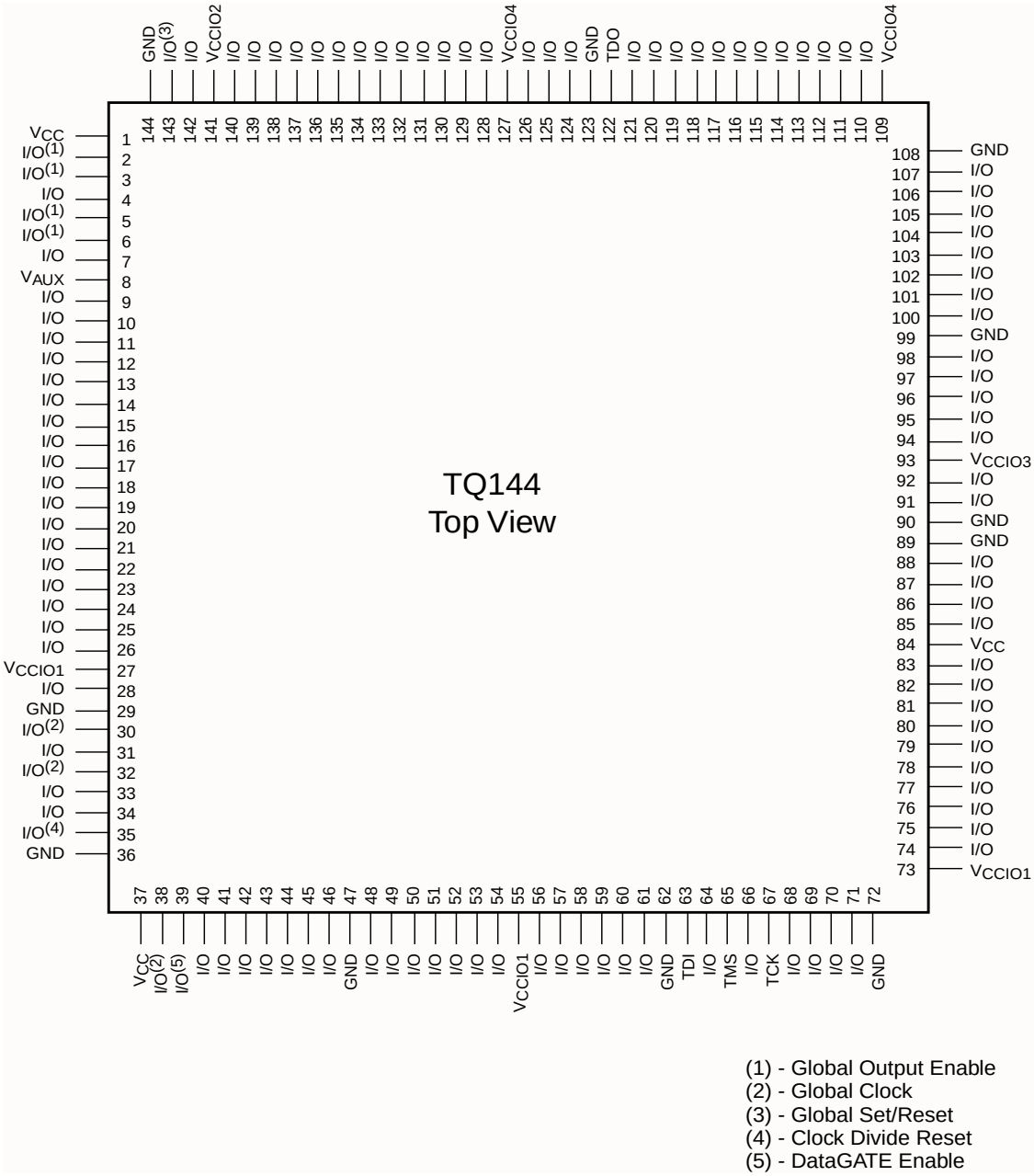


Figure 4: **TQ144 Thin Quad Flat Pack**

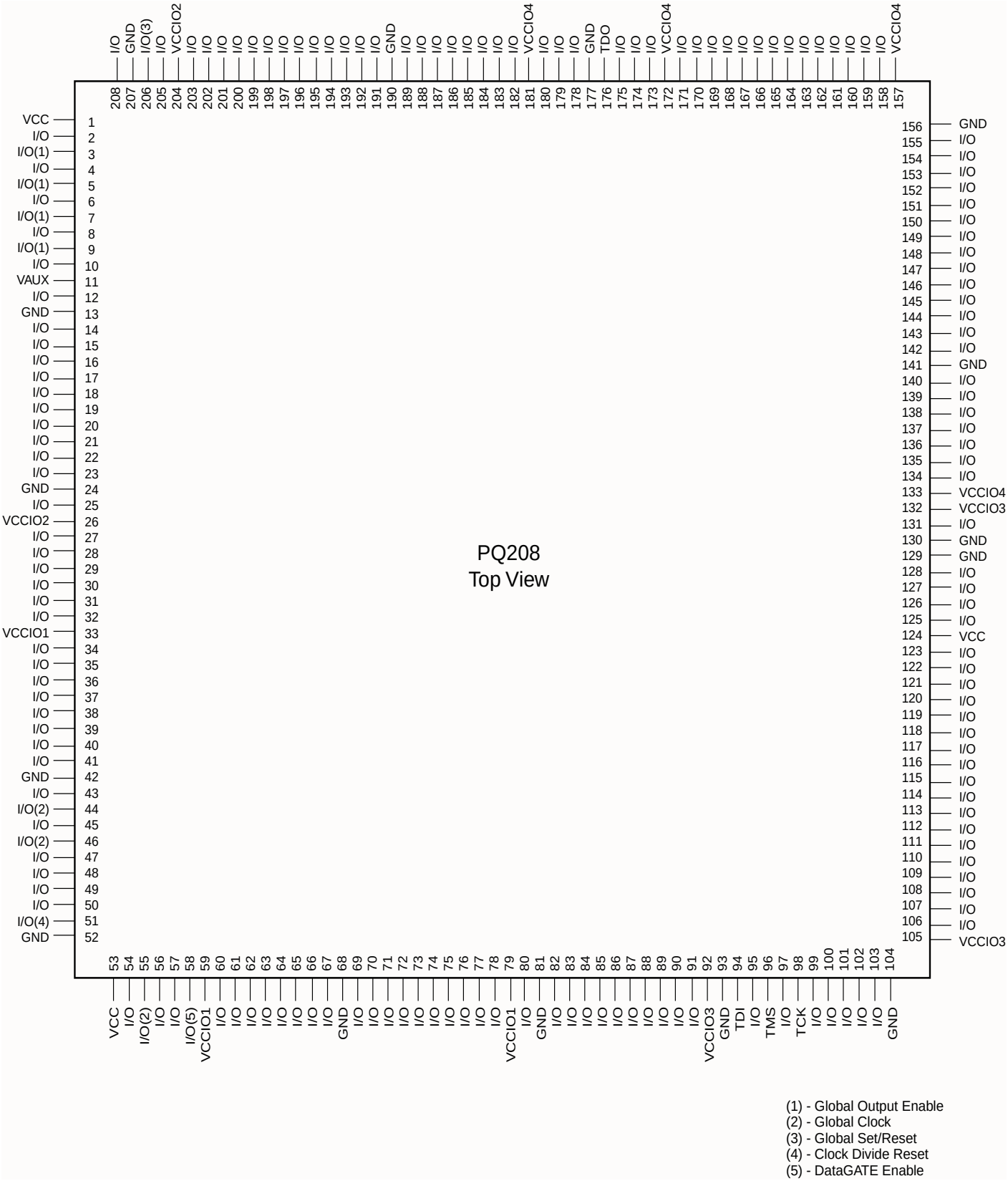
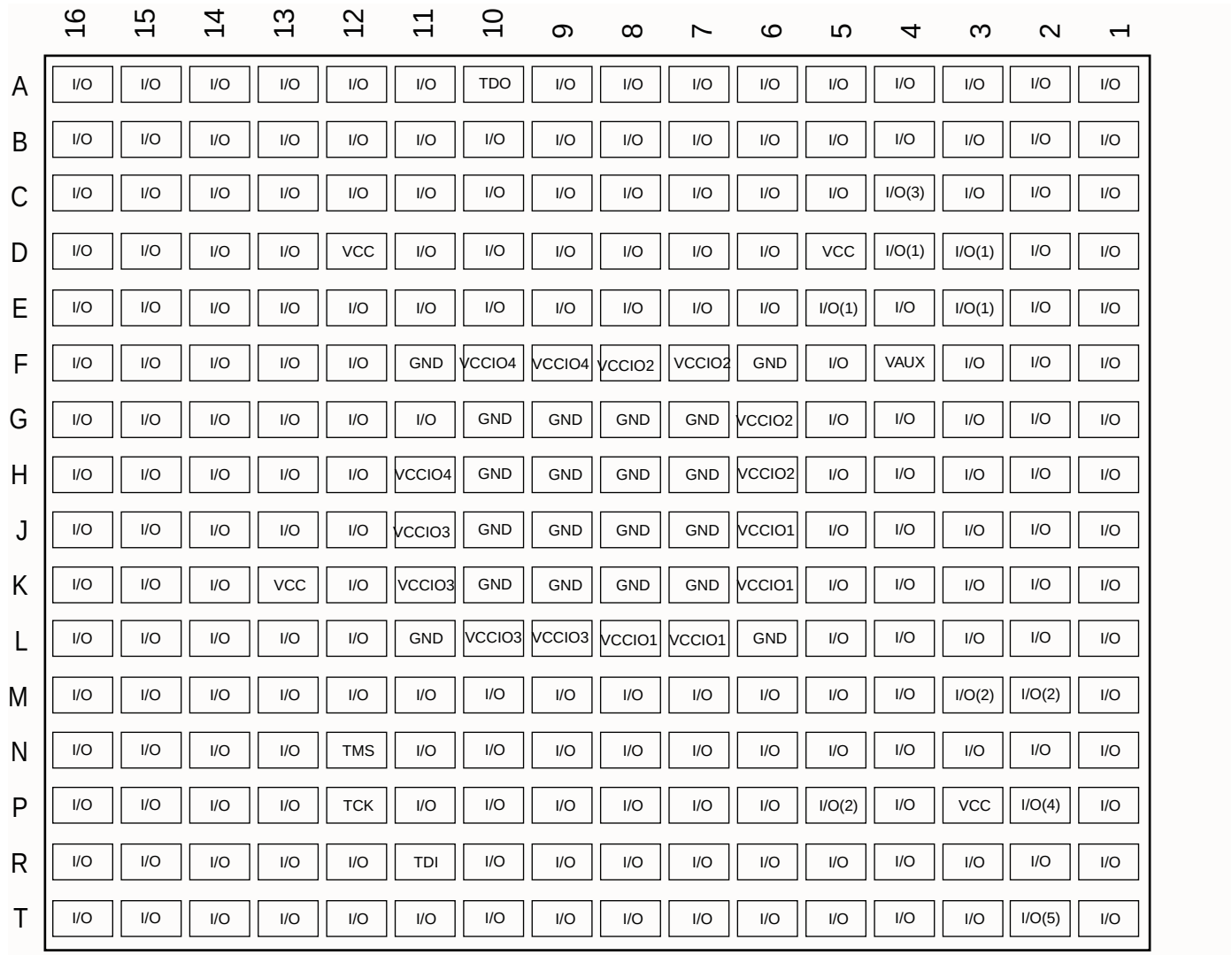


Figure 5: **PQ208 Plastic Quad Flat Package**

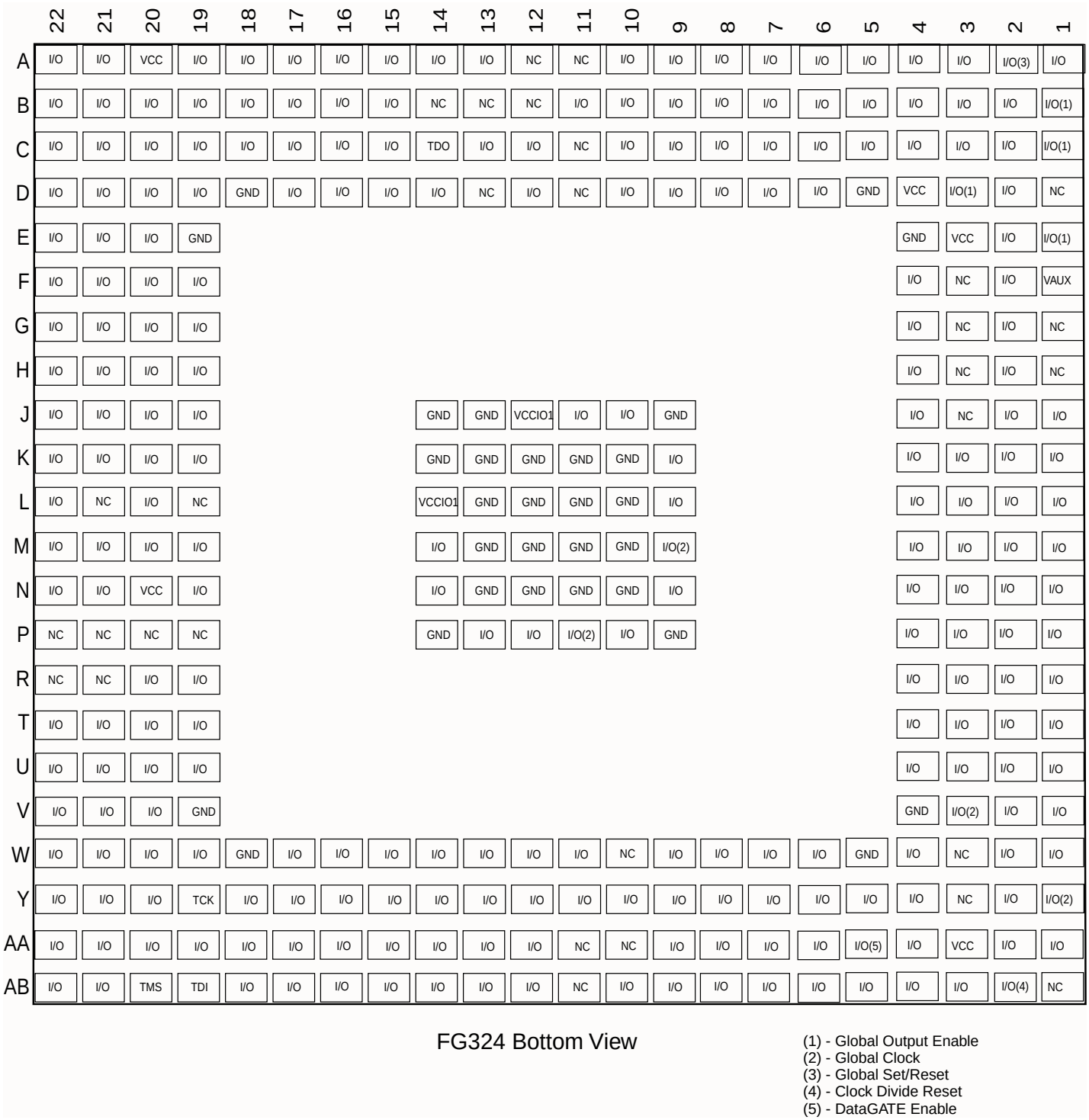


	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
A	I/O	I/O	I/O	I/O	I/O	I/O	TDO	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O
B	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O
C	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O(3)	I/O	I/O	I/O
D	I/O	I/O	I/O	I/O	VCC	I/O	I/O	I/O	I/O	I/O	I/O	VCC	I/O(1)	I/O(1)	I/O	I/O
E	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O(1)	I/O	I/O(1)	I/O	I/O
F	I/O	I/O	I/O	I/O	I/O	GND	VCCIO4	VCCIO4	VCCIO2	VCCIO2	GND	I/O	VAUX	I/O	I/O	I/O
G	I/O	I/O	I/O	I/O	I/O	I/O	GND	GND	GND	GND	VCCIO2	I/O	I/O	I/O	I/O	I/O
H	I/O	I/O	I/O	I/O	I/O	VCCIO4	GND	GND	GND	GND	VCCIO2	I/O	I/O	I/O	I/O	I/O
J	I/O	I/O	I/O	I/O	I/O	VCCIO3	GND	GND	GND	GND	VCCIO1	I/O	I/O	I/O	I/O	I/O
K	I/O	I/O	I/O	VCC	I/O	VCCIO3	GND	GND	GND	GND	VCCIO1	I/O	I/O	I/O	I/O	I/O
L	I/O	I/O	I/O	I/O	I/O	GND	VCCIO3	VCCIO3	VCCIO1	VCCIO1	GND	I/O	I/O	I/O	I/O	I/O
M	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O(2)	I/O(2)	I/O
N	I/O	I/O	I/O	I/O	TMS	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O
P	I/O	I/O	I/O	I/O	TCK	I/O	I/O	I/O	I/O	I/O	I/O	I/O(2)	I/O	VCC	I/O(4)	I/O
R	I/O	I/O	I/O	I/O	I/O	TDI	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O
T	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O(5)	I/O

FT256 Bottom View

(1) - Global Output Enable
(2) - Global Clock
(3) - Global Set/Reset
(4) - Clock Divide Reset
(5) - DataGATE Enable

Figure 6: **FT256 Fine Pitch Thin BGA**



FG324 Bottom View

(1) - Global Output Enable
(2) - Global Clock
(3) - Global Set/Reset
(4) - Clock Divide Reset
(5) - DataGATE Enable

Figure 7: **FG324 Fine Pitch BGA**

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
05/31/02	1.0	Initial Xilinx release.
09/23/02	1.1	Updated FT256 and TQ144 pinouts.