Spartan-IIE 1.8V FPGA Automotive IQ Product Family: Introduction and Ordering

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Advance Product Specification

Introduction

The Spartan™-IIE 1.8V Field-Programmable Gate Array (FPGA) Automotive IQ product family gives users high performance, abundant logic resources, and a rich feature set. The five-member family offers densities ranging from 50,000 to 600,000 system gates, as shown in Table 1.

Spartan-IIE devices deliver more gates, I/Os, and features per Dollar/Euro than other FPGAs by combining advanced process technology with a streamlined architecture based on the proven Virtex™-E platform. Features include block RAM (to 288K bits), distributed RAM (to 216K bits), 19 selectable I/O standards, and four DLLs (Delay-Locked Loops). Fast, predictable interconnect means that successive design iterations continue to meet timing requirements.

The Spartan-IIE family is a superior alternative to mask-programmed ASICs. The FPGA avoids the initial cost, lengthy development cycles, and inherent risk of conventional ASICs. Also, FPGA programmability permits design upgrades in the field with no hardware replacement necessary (impossible with ASICs).

Features

- Guaranteed to meet full electrical specifications over T_J = –40°C to +125°C
- Second generation ASIC replacement technology
  - Densities as high as 15,552 logic cells with up to 600,000 system gates
  - Streamlined features based on Virtex-E architecture
  - Unlimited in-system reprogrammability
- System level features
  - SelectRAM+™ hierarchical memory:
    - 16 bits/LUT distributed RAM to enable larger FIFOs, cache tag memory, and buffers
    - Configurable 4K-bit true dual-port block RAM to enable larger FIFOs, cache tag
    - Fast interfaces to external RAM such as SDRAM and ZBTRAM
  - Low-power segmented routing architecture
  - Full readback ability for verification/observability
  - Dedicated carry logic for high-speed arithmetic
  - Efficient multiplier support
  - Cascade chain for wide-input functions
  - Abundant registers/latches with enable, set, reset
  - Four dedicated DLLs for advanced clock control such as de-skewing clocks, clock generation (multiply/divide), and board level de-skew
  - Four primary low-skew global clock distribution nets
  - IEEE 1149.1 compatible boundary scan logic
- Versatile I/O and packaging
  - Family footprint compatibility in common packages
  - 19 high-performance interface standards, including LVDS and LVPECL — ideal for level shifting, interfacing, and translation (chip-to-chip, chip-to-memory, and chip-to-backplane)
  - Up to 205 differential I/O pairs that can be input, output, or bidirectional
  - Zero hold time simplifies system timing
- Fully supported by powerful Xilinx ISE development system
  - Fully automatic mapping, placement, and routing
  - Integrated with design entry and verification tools

Table 1: **Spartan-IIE FPGA Family Members**

Device	Logic Cells	Typical System Gate Range (Logic and RAM)	CLB Array (R x C)	Total CLBs	Maximum Available User I/O	Maximum Differential I/O Pairs	Distributed RAM Bits	Block RAM Bits
XC2S50E	1,728	23,000 - 50,000	16 x 24	384	182	83	24,576	32K
XC2S100E	2,700	37,000 - 100,000	20 x 30	600	182	83	38,400	40K
XC2S150E	3,888	52,000 - 150,000	24 x 36	864	182	83	55,296	48K
XC2S200E	5,292	71,000 - 200,000	28 x 42	1,176	182	83	75,264	56K
XC2S300E	6,912	93,000 - 300,000	32 x 48	1,536	329	120	98,304	64K
XC2S400E	10,800	145,000 - 400,000	40 x 60	2,400	410	172	153,600	160K
XC2S600E	15,552	210,000 - 600,000	48 x 72	3,456	514	205	221,184	288K

DC Specifications

Absolute Maximum Ratings(1)

Symbol	Description	Min	Max	Units
V_{CCINT}	Supply voltage relative to GND	–0.5	2.0	V
V_{CCO}	Supply voltage relative to GND	–0.5	4.0	V
V_{REF}	Input reference voltage	–0.5	4.0	V
V_{IN}	Input voltage relative to GND(2,3)	–0.5	4.05	V
V_{TS}	Voltage applied to 3-state output (3)	–0.5	4.0	V
T_{STG}	Storage temperature (ambient)	–65	+150	°C
T_J	Junction temperature	-	+135	°C

Notes:
1. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.
2. V_{IN} should not exceed V_{CCO} by more than 3.6V over extended periods of time (e.g., longer than a day).
3. Maximum DC overshoot must be limited to either V_{CCO} + 0.5V or 10 mA, and undershoot must be limited to –0.5V or 10 mA, whichever is easier to achieve. The Maximum AC conditions are as follows: The device pins may undershoot to –2.0V or overshoot to V_{CCO} + 2.0V, provided this over/undershoot lasts no more than 11 ns with a forcing current no greater than 100 mA.
4. For soldering guidelines, see the Packaging Information on the Xilinx website.

Recommended Operating Conditions

Symbol	Description	Min	Max	Units
T_J	Junction temperature	–40	125	°C
V_{CCINT}	Supply voltage relative to GND(1)	1.8 – 5%	1.8 + 5%	V
V_{CCO}	Supply voltage relative to GND(2)	1.2	3.6	V
T_{IN}	Input signal transition time(3)	-	250	ns

Notes:
1. Functional operation is guaranteed down to a minimum V_{CCINT} of 1.62V (Nominal V_{CCINT} –10%). For every 50 mV reduction in V_{CCINT} below 1.71V (nominal V_{CCINT} –5%), all delay parameters increase by 3%.
2. Minimum and maximum values for V_{CCO} vary according to the I/O standard selected.
3. Input and output measurement threshold is ~50% of V_{CCO}.

Spartan-IIE Product Availability

Table 2 shows the package and speed grades available for Spartan-IIE family devices. Table 3 shows the maximum user I/Os available on the device and the number of user I/Os available for each device/package combination.

Table 2: **Spartan-IIE Package and Speed Grade Availability**

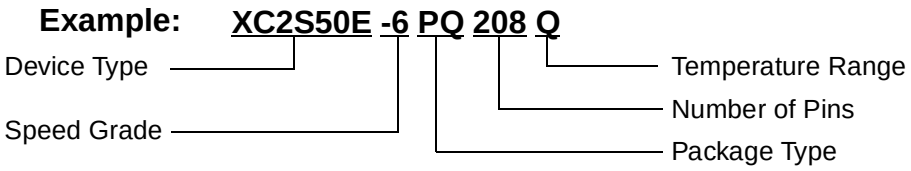
	Pins	144	208	256	456	676
	Type	Plastic TQFP	Plastic PQFP	Fine Pitch BGA	Fine Pitch BGA	Fine Pitch BGA
Device	Code	TQ144	PQ208	FT256	FG456	FG676
XC2S50E	-6	Q	Q	Q	-	-
XC2S100E	-6	Q	Q	Q	-	-
XC2S150E	-6	-	Q	Q	-	-
XC2S200E	-6	-	Q	Q	-	-
XC2S300E	-6	-	Q	-	Q	-
XC2S400E	-6	-	-	-	Q	Q
XC2S600E	-6	-	-	-	Q	Q

Notes:
1. Q = Automotive IQ, T_J = –40°C to +125°C

Table 3: **Spartan-IIE User I/O Chart**

Device	Maximum User I/O	Available User I/O According to Package Type				
		TQ144	PQ208	FT256	FG456	FG676
XC2S50E	182	102	146	182	-	-
XC2S100E	182	102	146	182	-	-
XC2S150E	182	-	146	182	-	-
XC2S200E	182	-	146	182	-	-
XC2S300E	329	-	146	-	329	-
XC2S400E	410	-	-	-	329	410
XC2S600E	514	-	-	-	329	514

Ordering Information



Device Ordering Options

Device
XC2S50E
XC2S100E
XC2S150E
XC2S200E
XC2S300E
XC2S400E
XC2S600E

Speed Grade	
-6	Standard Performance

Package Type / Number of Pins	
TQ144	144-pin Plastic Thin QFP
PQ208	208-pin Plastic QFP
FT256	256-ball Fine Pitch BGA
FG456	456-ball Fine Pitch BGA
FG676	676-ball Fine Pitch BGA

Temperature Range (T_J)	
Q = Automotive IQ	–40°C to +125°C

Revision History

Version No.	Date	Description
1.0	07/17/02	Initial Xilinx release.
1.1	11/18/02	Added XC2S400-E and XC2S600-E devices. Added FG676 to package list.
1.2	11/26/02	Updated Max User I/O and Differential I/O Pairs in Table 1 and Max User I/O in Table 3. Updated notes for Recommended Operating Conditions.

For more details about the Spartan-IIE Automotive IQ device, refer to specification:

DS106, *Spartan-IIE 1.8V FPGA Automotive IQ Family*