XCR3256XL 256 Macrocell Automotive IQ CPLD

DS119-3 (v1.0) February 14, 2003

Advance Product Specification

Features

- Guaranteed to meet full electrical specifications over T_A = –40°C to +125°C
- Technology: 0.35 µm EEPROM process
- Full Boundary Scan Test (IEEE 1149.1) for flexible in-system device and system testing
- Fast programming times in production saves time and money
  - Increases system reliability through reduced device handling
- High-speed pin-to-pin delays of 12 ns (88 MHz)
- Slew rate control per output to reduce EMI
- 100% routable which enables all device resources to be utilized
- Refer to XPLA3 Family data sheet (DS012) for architecture description
- Refer to XCR3256XL data sheet (DS013) for pin descriptions

Description

The CoolRunner™ XCR3256XL-Q CPLD Automotive IQ product is targeted for low power systems that include portable, handheld, automotive, and power sensitive applications. This device includes Fast Zero Power™ (FZP) design technology that combines low power and high speed. With this design technique, the XCR3256XL-Q delivers low standby current without the need for "turbo bits" or other power down schemes. By replacing conventional sense amplifier methods for implementing product terms (a technique that has been used in PLDs since the bipolar era) with a cascaded chain of pure CMOS gates, the dynamic power is also substantially lower than any other CPLD. CoolRunner devices are the only TotalCMOS PLDs, as they use both a CMOS process technology and the patented full CMOS FZP design technique.

The CoolRunner XCR3256XL-Q employs a full PLA structure for logic allocation within a functon block. The PLA provides maximum flexibility and logic density, with superior pin locking capability, while maintaining deterministic timing.

The CoolRunner XCR3256XL-Q is supported by WebPACK™ and WebFITTER™ from Xilinx and industry standard CAE tools (Cadence/OrCAD, Exemplar Logic, Mentor, Synopsys, ViewLogic, and Synplicity), using text (ABEL, VHDL, Verilog) and schematic capture design entry. Design verification uses industry standard simulators for functional and timing simulation. Development is supported on personal computer, Sparc, and HP platforms.

The XCR3256XL-Q features also include industry-standard, IEEE 1149.1, JTAG interface through which boundary-scan testing and In-System Programming (ISP) and reprogramming of the device can occur. This device is electrically reprogrammable using industry standard device programmers.

Table 1: **CoolRunner XCR3256XL-Q**

	XCR3256XL-Q
Macrocells	256
Usable Gates	6,000
Registers	256
F_{SYSTEM} (MHz)	88
User I/O (208-pin PQFP)	164

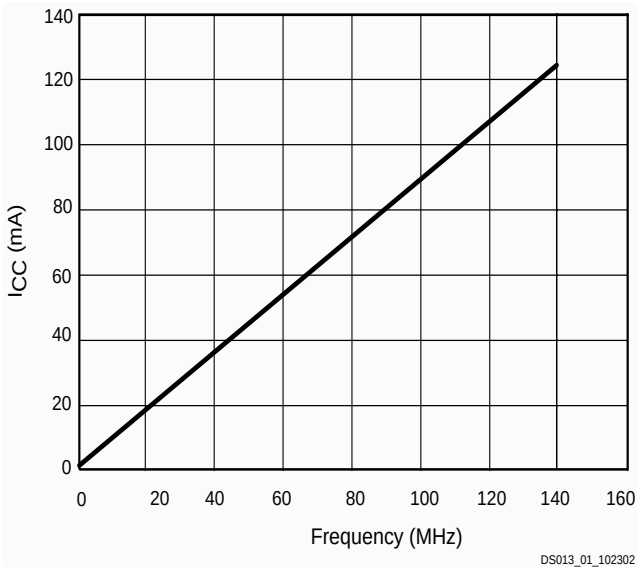


Figure 1: **XCR3256XL Typical I_{CC} vs. Frequency at V_{CC} = 3.3V, 25°C**

Table 2: **Typical I_{CC} vs. Frequency at V_{CC} = 3.3V, 25°C**

Frequency (MHz)	0	1	10	20	40	60	80	100	120	140
Typical I_{CC} (mA)	0.02	0.98	9.69	19.3	38.1	56.2	73.7	90.8	107.3	123.9

Absolute Maximum Ratings(1)

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply voltage(2) relative to GND	–0.5	4.0	V
V_I	Input voltage(3) relative to GND	–0.5	5.5(4)	V
I_{OUT}	Output current, per pin	–100	100	mA
T_J	Maximum junction temperature	–40	150	°C
T_{STR}	Storage temperature	–65	150	°C

Notes:

1. Stresses above those listed may cause malfunction or permanent damage to the device. This is a stress rating only. Functional operation at these or any other condition above those indicated in the operational and programming specification is not implied.
2. The chip supply voltage must rise monotonically.
3. Maximum DC undershoot below GND must be limited to either 0.5V or 10 mA, whichever is easier to achieve. During transitions, the device pins may undershoot to –2.0V or overshoot to 7.0V, provided this over- or undershoot lasts less than 10 ns and with the forcing current being limited to 200 mA.
4. External I/O voltage may not exceed V_{CC} by 4.0V.

Recommended Operating Conditions

Symbol	Parameter	Min.	Max.	Unit
T_A	Ambient temperature	–40	+125	°C
V_{CC}	Supply voltage	3.0	3.6	V
V_{IL}	Low-level input voltage	0	0.8	V
V_{IH}	High-level input voltage	2.0	5.5	V
V_O	Output voltage	0	V_{CC}	V
T_R	Input rise time	-	20	ns
T_F	Input fall time	-	20	ns

Quality and Reliability Characteristics

Symbol	Parameter	Min	Max	Units
T_{DR}	Data retention	20	-	Years
N_{PE}	Program/erase cycles (Endurance) @ T_A = 70°C	10,000	-	Cycles

DC Electrical Characteristics Over Recommended Operating Conditions

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
V_{OH}[1]	Output High voltage	I_{OH} = –500 µA	90%V_{CC}[2]	-	V
		V_{CC} = 3.0V, I_{OH} = –8 mA	2.4	-	V
V_{OL}	Output Low voltage	I_{OL} = 8 mA	-	0.4	V
I_{IL}[3]	Input leakage current	V_{IN} = GND or V_{CC}	–10	10	µA
I_{IH}[3]	I/O High-Z leakage current	V_{IN} = GND or V_{CC}	–10	10	µA
I_{CCSB}	Standby current	V_{CC} = 3.6V	-	5.0	mA
I_{CC}	Dynamic current[4]	f = 1 MHz	-	10	mA
		f = 50 MHz	-	75	mA
C_{IN}	Input pin capacitance[5]	f = 1 MHz	-	8	pF
C_{CLK}	Clock input capacitance[5]	f = 1 MHz	-	12	pF
$C_{I/O}$	I/O pin capacitance[5]	f = 1 MHz	-	10	pF

Notes:

1. See Figure 2 for output drive characteristics of the XPLA3 family.
2. This parameter guaranteed by design and characterization, not by testing.
3. Typical leakage current is less than 1 µA.
4. This parameter measured with a 16-bit, resetable up/down counter loaded into every function block, with all outputs disabled and unloaded. Inputs are tied to V_{CC} or ground. This parameter guaranteed by design and characterization, not testing.
5. Typical values, not tested.

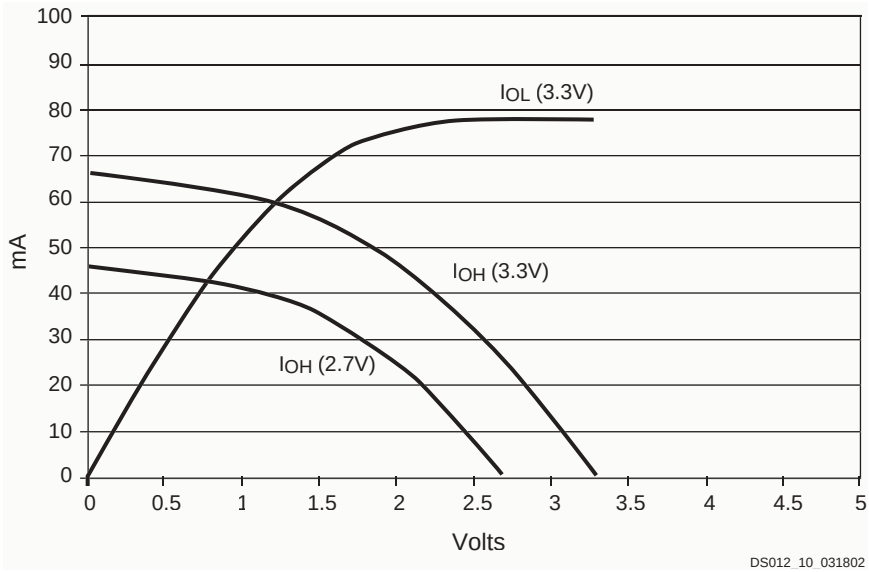


Figure 2: **Typical I/V Curve for the XPLA3 Family, 3.3V, 25°C**

AC Electrical Characteristics Over Recommended Operating Conditions(1)

Symbol	Parameter	-12		Unit
		Min.	Max.	
T_{PD1}	Propagation delay time (single p-term)	-	10.8	ns
T_{PD2}	Propagation delay time (OR array)	-	12.0	ns
T_{CO}	Clock to output (global synchronous pin clock)	-	6.9	ns
T_{SUF}	Setup time (fast input register)	3.0	-	ns
T_{SU1}(2)	Setup time (single p-term)	6.7	-	ns
T_{SU2}	Setup time (OR array)	7.9	-	ns
T_{H}(2)	Hold time	0.0	-	ns
T_{WLH}(2)	Global Clock pulse width (High or Low)	5.0	-	ns
T_{PLH}(2)	P-term clock pulse width	7.5	-	ns
T_{R}(2)	Input rise time	-	20.0	ns
T_{L}(2)	Input fall time	-	20.0	ns
f_{SYSTEM}(2)	Maximum system frequency	-	88	MHz
T_{CONFIG}(2)	Configuration time(3)	-	200	µs
T_{INIT}	ISP initialization time	-	200	µs
T_{POE}(2)	P-term OE to output enabled	-	13.0	ns
T_{POD}(2)	P-term OE to output disabled(4)	-	13.0	ns
T_{PCO}(2)	P-term clock to output	-	12.4	ns
T_{PAO}(2)	P-term set/reset to output valid	-	13.0	ns

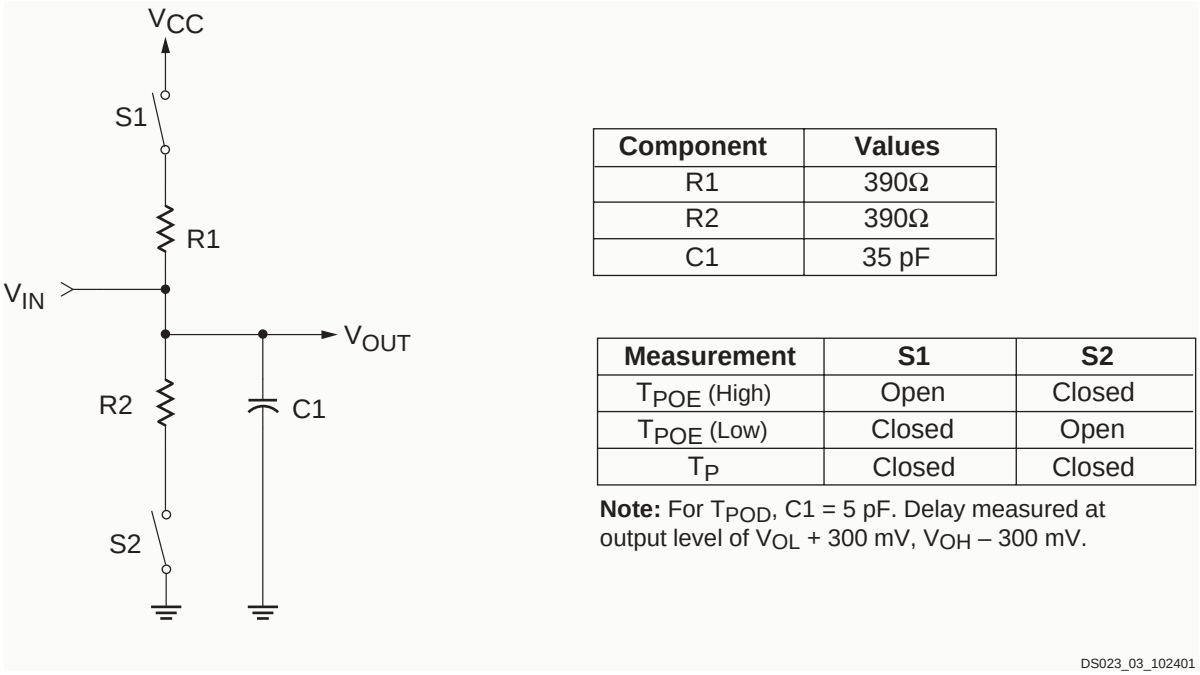
Notes:
1. Specifications measured with one output switching.
2. These parameters guaranteed by design and/or characterization, not testing.
3. Typical current draw during configuration is 3 mA at 3.6V.
4. Output C_L = 5 pF.

Internal Timing Parameters(1)

Symbol	Parameter	-12		Unit
		Min.	Max.	
Buffer Delays				
T_{IN}	Input buffer delay	-	4.0	ns
T_{FIN}	Fast Input buffer delay	-	3.3	ns
T_{GCK}	Global Clock buffer delay	-	1.5	ns
T_{OUT}	Output buffer delay	-	3.8	ns
T_{EN}	Output buffer enable/disable delay	-	6.0	ns
Internal Register, Product Term, and Combinatorial Delays				
T_{LDI}	Latch transparent delay	-	2.0	ns
T_{SUI}	Register setup time	1.2	-	ns
T_{HI}	Register hold time	0.7	-	ns
T_{ECSU}	Register clock enable setup time	3.0	-	ns
T_{ECHO}	Register clock enable hold time	5.5	-	ns
T_{COI}	Register clock to output delay	-	1.6	ns
T_{AOI}	Register async. S/R to output delay	-	2.2	ns
T_{RAI}	Register async. recovery	-	8.0	ns
T_{PTCK}	Product term clock delay	-	3.0	ns
T_{LOGI1}	Internal logic delay (single p-term)	-	3.0	ns
T_{LOGI2}	Internal logic delay (PLA OR term)	-	4.2	ns
Feedback Delays				
T_{F}	ZIA delay	-	4.4	ns
Time Adders				
T_{LOGI3}	Fold-back NAND delay	-	3.0	ns
T_{UDA}	Universal delay	-	3.0	ns
T_{SLEW}	Slew rate limited delay	-	6.0	ns

Notes:
1. These parameters guaranteed by design and characterization, not testing.

Switching Characteristics

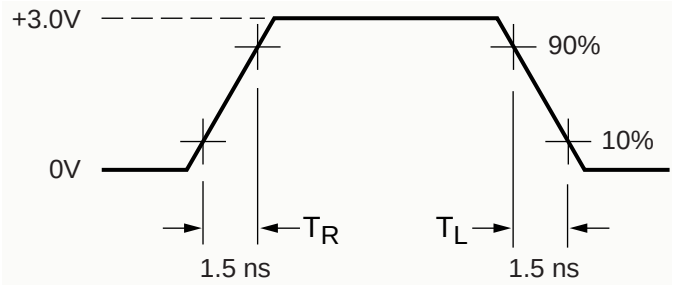


Component	Values
R1	390Ω
R2	390Ω
C1	35 pF

Measurement	S1	S2
T_{POE} (High)	Open	Closed
T_{POE} (Low)	Closed	Open
T_P	Closed	Closed

Note: For T_{POD}, C1 = 5 pF. Delay measured at output level of V_{OL} + 300 mV, V_{OH} – 300 mV.

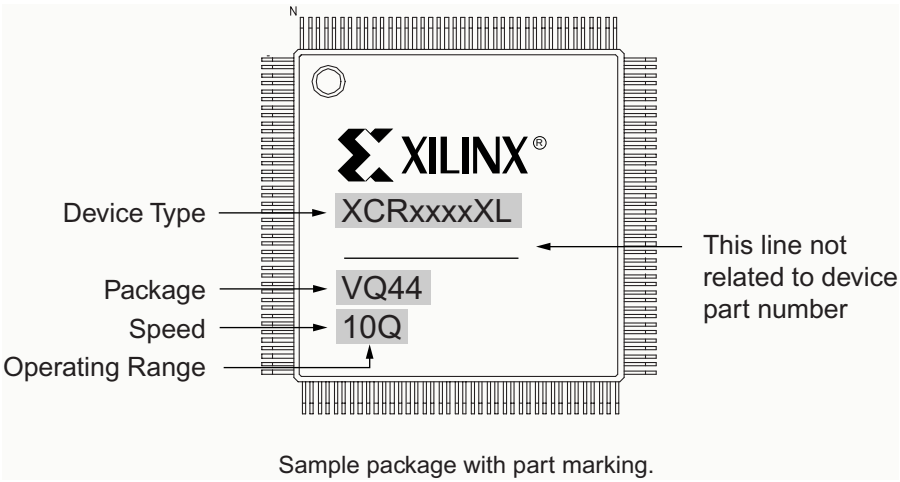
Figure 3: **Typical AC Load Circuit**



Measurements:
All circuit delays are measured at the +1.5V level of inputs and outputs, unless otherwise specified.

Figure 4: **Typical Voltage Waveform**

Device Part Marking



Sample package with part marking.

Ordering Combination Information

Device Ordering and Part Marking Number	Speed (pin-to-pin delay)	Pkg. Symbol	No. of Pins	Package Type	Operating Range(1)
XCR3256XL-12PQ208Q	12 ns	PQ208	208-pin	Plastic Quad Flat Pack (PQFP)	Q

Notes:
1. Q = Automotive: T_A = –40° to +125°C

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
02/14/03	1.0	Initial Xilinx release.