



Spartan Families

High volume package solutions guide

Spartan™ families provide the low-cost, high-volume ASIC packages for applications that need low power, small form factors and high reliability. The Chip Scale Package (CSP) and the Fine Pitch BGA package (FG) provide higher I/O count in significantly less board space with the smallest form factor thus reducing the board space, and are ideal for high-volume and cost-sensitive designs. The plastic packages (QFP) provide the high-volume, low-cost packages. All of the Spartan packages provide low power and high reliability. This package solutions guide will allow you to quickly compare the board space requirements for the Chip Scale (CSP), Plastic Chip Carrier (PC), Plastic Quad Flat Pack (PQFP, TQFP, VQFP), Ball Grid Array (BG), and Fine-Pitch Ball Grid Array (FG) packages. It also shows the board layout guidelines for the CSP, BG, and FG packages.



Actual size shown

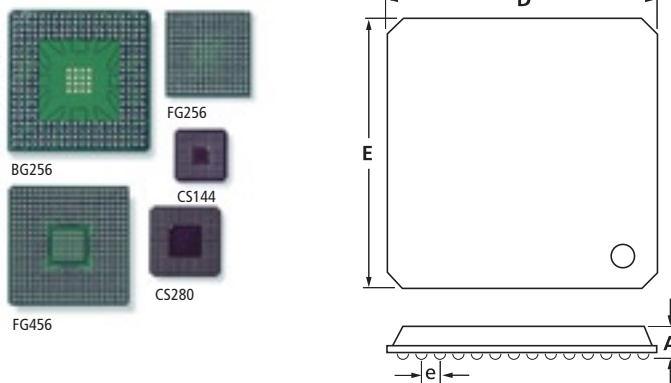
Packages by device

	PC	CSP		1.0 mm FG		1.27 mm BG	TQ/VQ/PQFP			
Leads/balls	84	144	280	256	456	256	100	144	208	240
Spartan-XL										
XCS05/XL	X						X			
XCS10/XL	X	X ¹					X	X		
XCS20/XL		X ¹					X	X	X	
XCS30/XL			X ¹			X	X	X	X	X
XCS40/XL			X ¹			X			X	X
Spartan-II										
XC2S15		X					X	X		
XC2S30		X					X	X	X	
XC2S50				X				X	X	
XC2S100				X	X			X	X	
XC2S150				X	X				X	

Notes:

1. Only Spartan-XL device is offered in this package. For more information, see the Spartan/XL data sheet at <http://www.xilinx.com/partinfo/spartan.pdf>

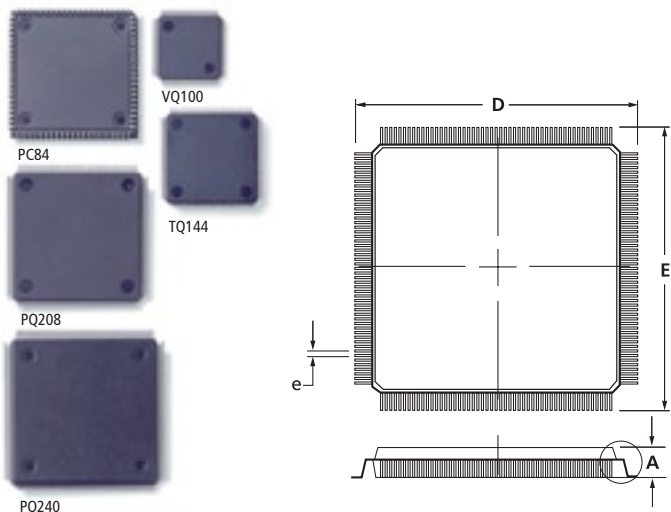
Chip Scale and Ball Grid Array



Chip Scale and Ball Array Packaging (CS/FG/BG)

Package Leads	Chip Scale (CS)		1.0mm BGA (FG)		1.27mm BGA (BG)
(All in mm)	CS144	CS280	FG256	FG456	BG256
Ball spacing (e)	0.8	0.8	1	1	1.27
Height (A)	1.2	1.2	1.7	2.2	2.3
Width/length (D/E)	12	16	17	23	27
Theta JA still air C/W	35	30	23-25	17-19	24-32

Plastic Quad Flatpack



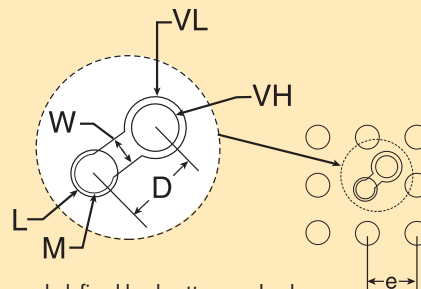
Plastic Leaded Chip Carrier (PC) and Plastic Quad Flat Pack Packaging (PQ/TQ/VQ)

Package Leads	PC	PQ	TQ	VQ	
(All in mm)	PC84	PQ208	PQ240	TQ144	VQ100
Lead spacing (e)	1.27	0.5	0.5	0.5	0.5
Height (A)	5.08	4.1	4.1	1.6	1.2
Width/length (D/E)	30.3	30.6	34.6	22	16
Theta JA still air C/W	41	26-35	19-28	30-35	32-47

For detailed package information, see the Xilinx web site at: <http://www.xilinx.com/partinfo/databook.htm#Packages>

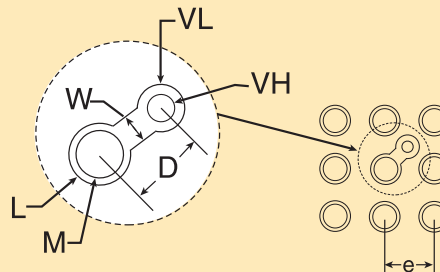
Recommended PCB Design Rules

Mask Opening Outside of Land



Non solder mask defined land patterns or land defined land patterns are recommended for CS.

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	CSP		1.0mm FG	
	CS144	CS280	FG256	FG456
Solder land (L) diameter	0.33	0.33	0.54	0.54
Opening in solder mask (M) diameter	0.44	0.44	0.45	0.45
Solder (ball) land pitch (e)	0.8	0.8	1	1
Line width between via and land (W)	0.25	0.25	0.3	0.3
Distance between via and land (D)	0.56	0.56	0.7	0.7
Via Land (VL) diameter	0.51	0.51	0.56	0.56
Through Hole (VH), plated diameter	0.25	0.25	0.3	0.3
Pad Array	Periphery	Periphery	Full	Periphery
Matrix or external row	13 x 13	19 x 19	16 x 16	22 x 22
Periphery Rows	4	5	4	7*

Notes:

1. Dimensions in millimeters
2. 3 x 3 matrix for illustration only, one land pad shown with via connection to land pad
3. Reference J-STD-013, use 'dog-bone' design via connection to land pad
4. *FG has more solder balls in the center periphery rows of balls
5. Non Solder Mask Defined (NSMD) lands are recommended for CS packages

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