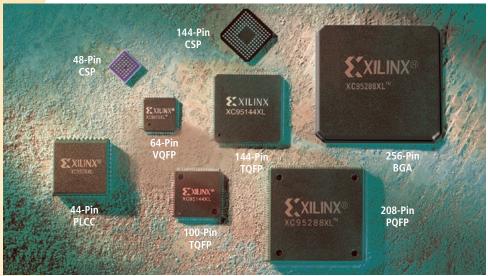# XC9500XL/XV™ CPLD Families

The XC9500XL and XC9500XV CPLD families from Xilinx combine an advanced architecture with efficient manufacturing processes to give you system flexibility, high performance, faster time-to-market, and lower overall costs. Targeted for leading-edge systems that require rapid design development, these CPLDs provide unparalleled performance and longer system life, along with robust field upgrade capability, the highest programming reliability, and ease of use. In addition, XC9500XL/XV CPLDs easily complement our higher density FPGAs, giving you a total, seamless logic solution.

- 48-Pin CSP
- 144-Pin CSP
- 64-Pin VQFP
- 144-Pin TQFP
- 256-Pin BGA
- 44-Pin PLCC
- 100-Pin TQFP
- 208-Pin PQFP

Family Overview:
- 36 to 288 macrocells
- Up to 4.0 ns pin-to-pin speeds with 250 MHz system frequency
- Fast in-system programming and erase times
- Superior pin-locking for reliable field upgrade capability
- Most extensive 1149.1 (JTAG) ISP programming capability
- The XC9500XL operates at 3.3V core voltage; interfaces with 5V, 3.3V, and 2.5V
- The XC9500XV operates at 2.5V core voltage; interfaces with 3.3V, 2.5V, and 1.8V

Ideal Applications:
- DRAM controller
- Microprocessor interface
- Video clock generator
- Display driver
- Gate array patch
- Bus transceiver
- PAL/GAL consolidation
- Discrete logic replacement
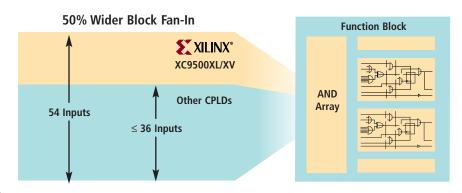
XC9500XL/XV Families

	XC9536XL/XV	XC9572XL/XV	XC95144XL/XV	XC95288XL/XV
Macrocells	36	72	144	288
Usable Gates	800	1,600	3,200	6,400
Registers	36	72	144	288
t_{PD} (ns)				
XC9500XL	5	5	5	6
XC9500XV	4	4	4	5
f_{system} (MHz)				
XC9500XL	222	222	222	208
XC9500XV	250	250	250	222
Packages (Max User I/O)	PC44 (34) VQ44 (34) VQ64* (34) CS48 (36)	PC44 (34) VQ44 (34) VQ64* (34) CS48 (38) TQ100 (72)	TQ100 (81) CS144 (117) TQ144 (117)	TQ144 (117) PQ208 (168) FG256 (192) BG256* (192) CS280 (192)

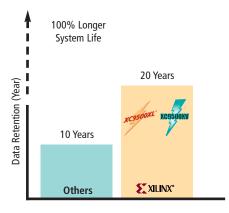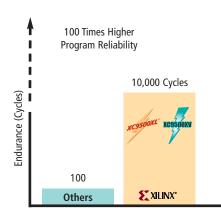* available in XC9500XL only

XILINX®

Advanced Architecture

- Ultra-wide 54 input function blocks for fast, wide logic
- Oversized 18 macrocell blocks for look ahead logic
- 90 possible product-terms per macrocell
- Three global clocks and product-term clock, with inversion at the macrocell
- Global and individual OE per output, with inversion at the output
- Bus-hold circuitry on all user I/O pins
- Input hysteresis on all user and JTAG inputs
- Multiple I/O banks in the XC9500XV for easy device interfacing

50% Wider Block Fan-In

XILINX®
XC9500XL/XV

54 Inputs

Other CPLDs

≤ 36 Inputs

Function Block

AND Array

Highest Device Reliability

Data Retention (Year)

100% Longer System Life

20 Years

XC9500XL XC9500XV

10 Years

Others

XILINX®

Endurance (Cycles)

100 Times Higher Program Reliability

10,000 Cycles

XC9500XL XC9500XV

100

Others

XILINX®

Solid Reliability

- Endurance rating of 10,000 program/ erase cycles
  - Virtually eliminates programming failures
- Data retention rating of 20 years
  - Supports longer system life
- Immune from "ISP Lock-Out" failure mode
- Allows arbitrary mixed power sequencing ("hot plugging")

Free CPLD Design Tools:

XC9500XL/XV devices are supported in all versions of the Xilinx Integrated Software Environment (ISE) including the free ISE WebPACK™ and WebFITTER.™ ISE WebPACK is a complete downloadable desktop solution that contains synthesis support, design verification and iMPACT programming support for all Xilinx devices. WebFITTER is an intuitive, online design tool that allows you to easily submit your designs to find out what a Xilinx CPLD can do for you.

A Compelling CPLD Solution

- 4.0 ns/250 MHz performance
- Flexible pin-locking architecture for simplified design changes
- Small and low-cost packaging
- Robust 5V, 3.3V, 2.5V and 1.8V interfacing
- A single software environment for your CPLD and FPGA designs

Contact Us

For more information contact your local Xilinx sales representative or visit us at **www.xilinx.com/products/cpldsolutions** to download your free software.

XILINX®
The Programmable Logic Company℠