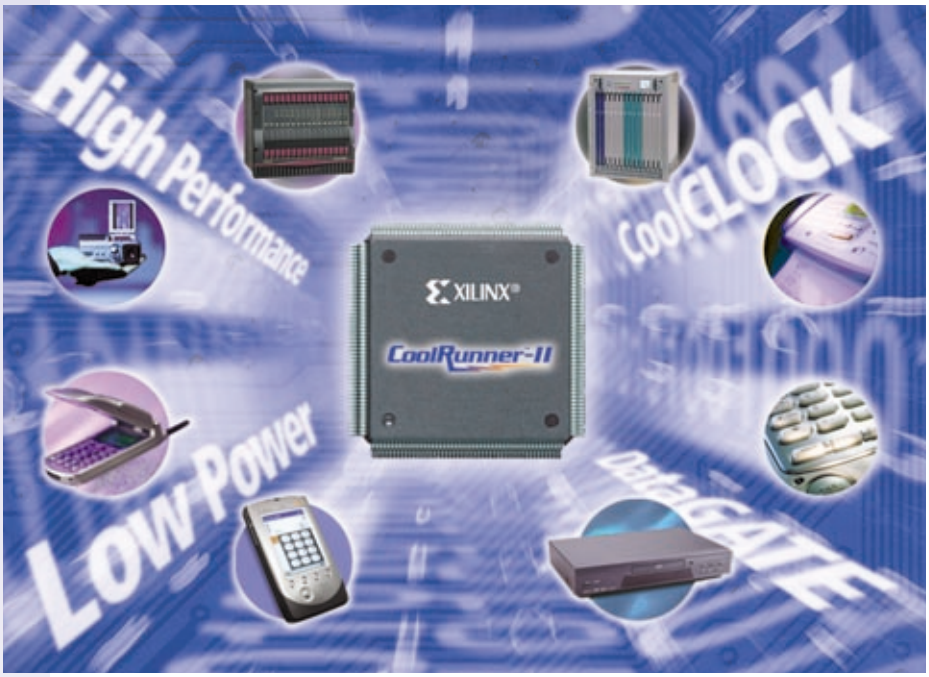
CoolRunner™-II

Xilinx CoolRunner-II: RealDigital CPLDs

High performance and ultra low power consumption with no compromises.

Designing today's advanced systems is a significant challenge. In the past, your only option was to choose a CPLD with either high performance or low power. Now, you can get the best of both worlds: high performance and ultra low power consumption in a single device with no compromises.

The new CoolRunner-II CPLD family uses our advanced second generation Fast Zero Power™ (FZP) scalable design technology to give you the best performance with the lowest possible power consumption, and no price premium now or in the future. Featuring a 100% digital core, advanced system features, up to 303 MHz performance, and less than 100 µA of standby current, CoolRunner-II CPLDs are the perfect solution for any new system.



A Complete Programmable Solution

There are many reasons to choose CoolRunner CPLDs, including:

- **Up to 303 MHz performance** — High performance for all leading-edge applications. Up to 400 MHz toggle rate with clock doubler.
- **Less than 100 µA standby current** — The industry's lowest power consumption.
- **1.8 Volt device operation** — I/O voltages compatible with 1.5V, 1.8V, 2.5V, and 3.3V logic levels to simplify multi-voltage system design.
- **A wide range of densities** — From 32 to 512 macrocells, to suit a broad range of applications.
- **Advanced system features** — Multiple I/O standards, clock management, and increased design security simplify your design.
- **Complete software support** — All Xilinx ISE software packages provide complete support for CoolRunner-II devices.
- **Advanced packaging** — Choose from Chip Scale (CSP), TQFP, PQFP, VQFP, PLCC, and fine line BGA packages for PC board space savings, cost optimization, and high performance.
- **Easy In System Programming (ISP)** — Support for IEEE 1532 In System Programming and IEEE 1149.1 JTAG Boundary Scan testing.
- **Superior pin-locking** — Implement design updates without changing pinouts, minimizing PC board layout changes and enabling field upgradeability.

XILINX®

Advanced System Features

Advanced I/O Support

- **LVTTL and LVCMOS** for standard chip-to-chip interfacing.
- **SSTL and HSTL** for standard chip-to-memory interfacing.
- **DataGATE** disables pins that are not being used and reduces power.
- **Bus Hold** keeps outputs in their last stable state, for further power reduction.
- **Input hysteresis (400mv)** conditions noisy and slow analog signals.

Superior Clock Management

- **Clock Doubler:** Enhances performance by doubling input clock switching frequency.
- **Clock Divider:** Improves power savings by dividing externally supplied global clocks by standard values.
- **CoolCLOCK:** Provides the ability to combine a clock divider and doubler to divide an incoming clock by two (reducing clocking power). It then doubles the clock at the macrocell.

Unparalleled Design Security

- **Four levels of design security** prevent accidental overwriting and pattern theft.

Software Tools

CoolRunner-II CPLDs are supported in all versions of the Xilinx Integrated Software Environment (ISE) which include ISE WebPACK™, WebFITTER™, and ISE Foundation™.

- **ISE WebPACK™** is a free, downloadable desktop solution that offers HDL and ABEL synthesis and simulation, JTAG and third-party EDA support, and device support for all Xilinx CPLD families (as well as Spartan-II, Spartan-IIE, Virtex-II, and Virtex-E FPGA families up to 300K gates).

DOWNLOAD NOW

- **WebFITTER™** is a Web-based, CPLD design fitting tool that allows you to evaluate your designs using CoolRunner-II and all other Xilinx CPLD families. WebFITTER accepts VHDL, Verilog, ABEL, and standard netlist inputs. You can convert existing designs from other CPLD manufacturers into the appropriate Xilinx CPLD.
- **ISE Foundation** is the full featured software environment that supports all of our current CPLD and FPGA families.

Contact Us!

For additional information, please visit our website at:
www.xilinx.com/cr2.

CoolRunner-II Family at a Glance

	XC2C32	XC2C64	XC2C128	XC2C256	XC2C384	XC2C512
I/O Standards	LVTTL,LVCMOS 15,18,25,33	LVTTL,LVCMOS 15,18,25,33	LVTTL,LVCMOS 15,18,25,33 SSTL 2-1,3-1 HSTL1	LVTTL,LVCMOS 15,18,25,33 SSTL 2-1,3-1 HSTL1	LVTTL,LVCMOS 15,18,25,33 SSTL 2-1,3-1 HSTL1	LVTTL,LVCMOS 15,18,25,33 SSTL 2-1,3-1 HSTL1
Max I/O	33	64	100	184	240	270
T_{PD}(ns)	3.5*	4.0*	4.5*	5.0*	6.0*	6.0*
I/O Banks	1	1	2	2	4	4
Clock double	Yes	Yes	Yes	Yes	Yes	Yes
Input Hysteresis	Yes	Yes	Yes	Yes	Yes	Yes
DataGATE & Clock divide			Yes	Yes	Yes	Yes
Packages	VQ44 PC44 CP56	VQ44 PC44 CP56 VQ100	VQ100 CP132 TQ144	VQ100 CP132 TQ144 PQ208 FT256	TQ144 PQ208 FT256 FG324	PQ208 FT256 FG324

* Note: T_{PD} speeds are estimates

Corporate Headquarters
Xilinx, Inc.
2100 Logic Drive
San Jose, CA 95124
Tel: (408) 559-7778
Fax: (408) 559-7114
Web: www.xilinx.com

Europe
Xilinx, Ltd.
Benchmark House
203 Brooklands Road
Weybridge
Surrey KT13 ORH
United Kingdom
Tel: 44-870-7350-600
Fax: 44-870-7350-601
Web: www.xilinx.com

Japan
Xilinx, K.K.
Shinjuku Square Tower 18F
6-22-1 Nishi-Shinjuku
Shinjuku-ku, Tokyo
163-1118, Japan
Tel: 81-3-5321-7711
Fax: 81-3-5321-7765
Web: www.xilinx.co.jp

Asia Pacific
Xilinx, Asia Pacific
Unit 1201, Tower 6, Gateway
9 Canton Road
Tsimshatsui, Kowloon,
Hong Kong
Tel: 852-2-424-5200
Fax: 852-2-494-7159
E-mail: hongkong@xilinx.com

XILINX®
The Programmable Logic Company℠

FORTUNE 2001
100 BEST COMPANIES TO WORK FOR

Printed in the U.S.A.

PN 0010619